



October 18, 2002

ERRATA TO JEDEC STANDARD

JESD8-9B, - ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)

REASON FOR ERRATA: Days after publication of this standard in May 2002, it was brought to the attention of the sponsor that there were errors in Table 4. After further investigation by the sponsor it was noted that during the transfer of numbers from the worksheet to FrameMaker a couple of typo's had been introduced. These typo's had gone unnoticed through the complete ballot process. The sponsor presented the corrected numbers to the committee at it's September 2002 meeting and Table 4 as corrected was approved.

HARD COPY: All recipients of this errata are asked to replace page 7 with the corrected page included in this errata.

ELECTRONIC: If you have downloaded the file prior to date of errata please reprint page 7. The sheet has been corrected in the downloadable file on the JEDEC website as of October 18, 2002.

The standard in question can be downloaded at no charge from the JEDEC web site at www.jedec.org.

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JEDEC STANDARD

Stub Series Terminated Logic for 2.5 V (SSTL_2)

JESD8-9B

(Revision of JESD8-9A)

MAY 2002

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)
A 2.5 V Supply Voltage Based Interface Standard for Digital Integrated Circuits

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STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)

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Foreword

The following changes are included in this revision: Reduction of V_{IH}/V_{IL} (AC) from 350 mV to 310 mV and of V_{IL}/V_{IH} (DC) from 180 mV to 150 mV (single ended applications); increase of driver current from 15.4 mA (7.6 mA) to 16.2 mA (8.1 mA); reduction of V_{IH}/V_{IL} (AC) from 700 mV to 620 mV and of V_{IH}/V_{IL} (DC) from 360 mV to 300 mV (differential applications.); recalculation of Table 4.

STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)

A 2.5 V Supply Voltage Based Interface Standard for Digital Integrated Circuits

(From JEDEC Board Ballots JCB-97-80 and JCB-98-80 (section 5), and JCB-01-87, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages. In many cases V_{DD} and V_{DDQ} will have the same voltage level. The V_{DD} value is not specified in this standard other than that V_{DDQ} value may not exceed that of V_{DD} .

1.1 Standard structure

The standard is defined in three clauses:

The first clause defines pertinent supply voltage requirements common to all compliant ICs.

The second clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The third clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments. The output specifications are divided into two classes, Class I and Class II, which are distinguished by drive requirements and application.

A given IC need not be equipped with both classes of output drivers, but each must support at least one to claim SSTL_2 output compliance.

The full input reference level (V_{REF}) range specified is required on each IC in order to allow any SSTL_2 IC to receive signals from any SSTL_2 output driver.

1.2 Rationale and assumptions

This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage.