

JEDEC STANDARD

Definition of the SSTVN16859 2.5-2.6 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM Applications

JESD82-13A.01

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**STANDARD FOR DEFINITION OF THE SSTVN16859 2.5–2.6 V 13-BIT TO 26-BIT SSTL_2
REGISTERED BUFFER FOR DDR DIMM APPLICATIONS**

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STANDARD FOR DEFINITION OF THE SSTVN16859 2.5–2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-74 and JCB-05-11, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTVN16859 13-bit to 26-bit SSTL_2 registered buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM applications. The SSTVN16859 is a speed upgrade of the SSTV16859 (JESD82-4) for use in PC3200 DDR DIMMs. It is fully backward compatible with SSTV16859 for all speed grades.

The purpose is to provide a standard for the SSTVN16859 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTVN16859 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 13-bit to 26-bit registered buffer is designed for 2.3 V to 2.7 V V_{DD} (PC1600, PC2100, PC2700) and 2.5 V to 2.7 V V_{DD} (PC3200) operation.

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SSTVN16859 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain low.