JEDEC STANDARD

Definition of the SSTUB32868 1.8 V Configurable Registered Buffer with Parity for DDR2 RDIMM Applications

JESD82-14A

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DEFINITION OF THE SSTUB32868 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-06-33, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications. SSTU32S2868 denotes a single-die implementation and SSTU32D868 denotes a dual-die implementation.

The purpose is to provide a standard for the SSTUB32868 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32868 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{DD} operation.

All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{\text{RESET}}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for un-terminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{\text{QERR}}$) output.

The SSTUB32868 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and un-driven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and C inputs always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully

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2 Device standard (cont'd)

2.1 Description (cont'd)

enabled, the design of the SSTUB32868 must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding $\overline{\text{QERR}}$ output signal for the data inputs is generated two clock cycles after the data, to which the $\overline{\text{QERR}}$ signal applies, is registered.

The SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when C = 0; or D1-D12, D17-D20, D22, D24-D28 when C = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power (LPM) and the $\overline{\text{QERR}}$ output is driven low, then it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hard-wired to a valid low or high level to configure the register in the desired mode.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high. If CSGEN, $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. Also, if both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs are high, the device will gate the $\overline{\text{QERR}}$ output from changing states. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ is low, the $\overline{\text{QERR}}$ output will function normally. The RESET input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and when driven low will force the Qn outputs low, and the $\overline{\text{QERR}}$ output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ only, then the CSGEN input should be pulled up to V_{DD} through a pull-up resistor.

The two V_{REF} pins (A1 and V1) are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

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2 Device standard (cont'd)

Package options include 176-ball TFBGA (MO-246 version B).

2.2 176-ball TFBGA (MO-246, Variation TBD)

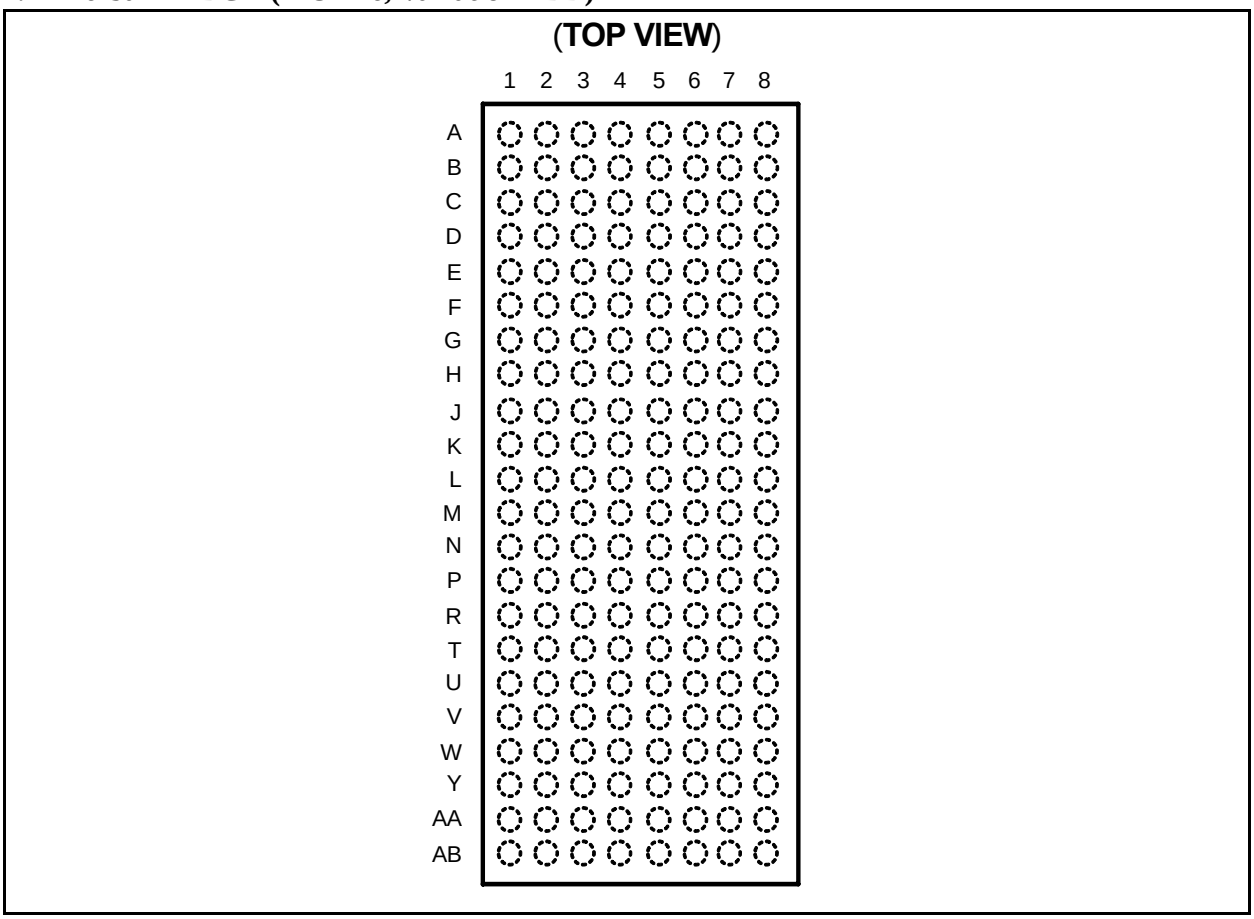

Figure 1 — Pinout configuration

NOTE 1 8 x 22 array, 6.0 x 15.0-mm body size, 0.65-mm pitch. Diagram is for reference only. See MO-246 for detailed package specification.

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2 Device standard (cont'd)

2.3 Pinout top view for 176-ball TFBGA

A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A QCKE0A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B (QCKE0B)
J	$\overline{DCS1}$	$\overline{QCS1A}$	GND	GND	GND	GND	Q10B	Q9B
K	$\overline{DCS0}$	$\overline{QCS0A}$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{QCS0B}$)	Q13B ($\overline{QCS1B}$)
M	$\overline{CK}$	$\overline{RESET}$	$\overline{QERR}$	V_{DD}	V_{DD}	V_{DD}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (Q0DT1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B
	1	2	3	4	5	6	7	8

Figure 2 — 1:2 Register A (C=0)

NC denotes no internal connection.

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2 Device standard (cont'd)

2.3 Pinout top view for 176-ball TFBGA (cont'd)

A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{CK}$	$\overline{RESET}$	$\overline{QERR}$	V_{DD}	V_{DD}	V_{DD}	Q15B ($\overline{QCS0B}$)	Q16B ($\overline{QCS1B}$)
N	D15 ($\overline{DCS0}$)	Q15A ($\overline{QCS0A}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{DCS1}$)	Q16A ($\overline{QCS1A}$)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B
	1	2	3	4	5	6	7	8

Figure 3 — 1:2 Register B (C=1)

NC denotes no internal connection.

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2 Device standard (cont'd)

2.4 Terminal functions

Table 1 — Terminal functions

Terminal name	Description	Electrical characteristics
GND	Ground	Ground input
V_{DD}	Power supply voltage	1.8-V nominal
V_{REF}	Input reference voltage	0.9-V nominal
CK	Positive master clock input	Differential input
$\overline{CK}$	Negative master clock input	Differential input
C	Configuration control inputs - Register A or Register B	LVCMOS inputs
$\overline{RESET}$	Asynchronous reset input – resets registers and disables V_{REF} data and clock differential-input receivers	LVCMOS input
CSGEN	Chip select gate enable – When high, D1-D28† inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1-D28† inputs will be latched and re-driven on every rising edge of the clock.	LVCMOS input
D1–D28	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL_18 input
$\overline{DCS0}$, $\overline{DCS1}$	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to re-drive all D inputs (CSGEN high) only when at least one chip select input is low. If CSGEN, $\overline{DCS0}$, and $\overline{DCS1}$ inputs are high, D1–D28† inputs will be disabled.	SSTL_18 input
DODT0, DODT1	The outputs of this register bit will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	SSTL_18 input
DCKE0, DCKE1	The outputs of this register bit will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	SSTL_18 input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input.	SSTL_18 input
Q1–Q28‡	Data outputs that are suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8-V CMOS outputs
$\overline{QCS0}$, $\overline{QCS1}$	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8-V CMOS output
QODT0, QODT1	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8-V CMOS output
QCKE0, QCKE1	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8-V CMOS output
$\overline{QERR}$	Output error bit - generated one clock cycle after the corresponding data output	Open-drain output
NC	No internal connection	

† Data inputs = D1-D5, D7, D9-D12, D17-D28 when C=0

Data inputs = D1-D12, D17-D20, D22, D24-D28 when C=1

‡ Data outputs = Q1-Q5, Q7, Q9-Q12, Q17-Q28 when C=0

Data outputs = Q1-Q12, Q17-Q20, Q22, Q24-Q28 when C=1

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