

JEDEC STANDARD

Definition of the SSTUA32866 1.8 V Configurable Registered Buffer with Parity Test for DDR2 RDIMM Applications

JESD82-16A

(Revision of JESD82-16, November 2005)

MAY 2007

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7559 or www.jedec.org.

Published by

©JEDEC Solid State Technology Association 2007
2500 Wilson Boulevard
Arlington, VA 22201-3834

This document may be downloaded free of charge, however JEDEC retains the copyright on this material.
By downloading this file the individual agrees not to charge for or resell the resulting material.

**Price: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications at www.jedec.org**

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by the JEDEC Solid State Technology Association
and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

DEFINITION OF THE SSTUA32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-05-101 and JCB-07-10, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32866 registered buffer with parity test for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTUA32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUA32866 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset ($\overline{\text{RESET}}$) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications. The error ($\overline{\text{QERR}}$) output is 1.8 V open-drain driver.

The SSTUA32866 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The SSTUA32866 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0; D2–D3, D5–D6, D8–D14 when C0 = 0 and C1=1; or D1–D6, D8–D13 when C0 = 1 and C1=1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. Two cycles after the data are registered, the corresponding partial-parity-out (PPO) and $\overline{\text{QERR}}$ signals are generated.

2 Device standard (cont'd)

2.1 Description (cont'd)

When used in pairs, the C0 input of the first register is tied low and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the $\overline{\text{PAR\_IN}}$ input of the first device. Two clock cycles after the data are registered the corresponding PPO and $\overline{\text{QERR}}$ signals are produced on the second device. The PPO output of the first register is cascaded to the $\overline{\text{PAR\_IN}}$ of the second register. The $\overline{\text{QERR}}$ output of the first register is left floating and the valid error information is latched on the $\overline{\text{QERR}}$ output of the second register.

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched as low for a clock duration equal to the parity-error duration or until $\overline{\text{RESET}}$ is driven low. For the case where a parity error occurs just before the device enters the low-power mode (LPM), see Table 4, Figure 18, Figure 19, and Figure 20. The DIMM-dependent signals ($\overline{\text{DCKE}}$, $\overline{\text{DCS}}$, $\overline{\text{DODT}}$, and $\overline{\text{CSR}}$) are not included in the parity check computation. The parity error output $\overline{\text{QERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS}}$ and/or $\overline{\text{CSR}}$ are asserted low.

The C0 input controls the pinout configuration for the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUA32866 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held high, $\overline{\text{DODT}}$ and $\overline{\text{DCKE}}$ must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$, C0, and C1 inputs must always be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn and PPO outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and when driven low will force the Qn and PPO outputs low, and the $\overline{\text{QERR}}$ output high. If the $\overline{\text{DCS}}$ control functionality is not desired, then the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS}}$ only, then the $\overline{\text{CSR}}$ input should be pulled

2 Device standard (cont'd)

up to V_{DD} through a pullup resistor.

Package options include 96-ball LFBGA (MO-205CC).

2.2 96-ball LFBGA (MO-205CC)

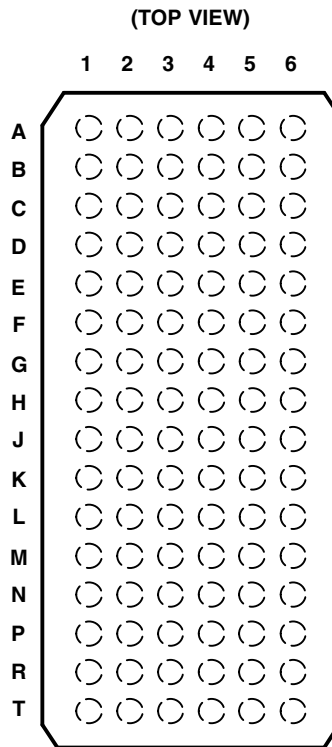


Figure 1 — Pinout configuration

2 Device standard (cont'd)**2.3 Pinout top view for 96-ball LFBGA**

A	DCKE	PPO	V _{REF}	V _{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{DD}	V _{DD}	Q3	Q16
D	DODT	$\overline{QERR}$	GND	GND	QODT	DNU
E	D5	D17	V _{DD}	V _{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{RESET}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCS}$	DNU
J	$\overline{CK}$	$\overline{CSR}$	V _{DD}	V _{DD}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{DD}	V _{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{DD}	V _{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{DD}	V _{DD}	Q13	Q24
T	D14	D25	V _{REF}	V _{DD}	Q14	Q25
	1	2	3	4	5	6

Figure 2 — 1:1 Register (C0=0, C1=0)

A	DCKE	PPO	V _{REF}	V _{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	DODT	$\overline{QERR}$	GND	GND	QODTA	QODTB
E	D5	NC	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V _{DD}	V _{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{DD}	V _{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{DD}	Q14A	Q14B
	1	2	3	4	5	6

Figure 3 — 1:2 Register A (C0=0, C1=1)

2 Device standard (cont'd)

2.3 Pinout top view for 96-ball LFBGA (cont'd)

A	D1	PPO	V _{REF}	V _{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	D4	$\overline{QERR}$	GND	GND	Q4A	Q4B
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	CSR	V _{DD}	V _{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V _{DD}	V _{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	DCKE	DNU	V _{REF}	V _{DD}	QCKEA	QCKEB
	1	2	3	4	5	6

Figure 4 — 1:2 Register B (C0=1, C1=1)

DNU denotes do not use. NC denotes no internal connection.

2 Device standard (cont'd)

2.4 Terminal functions

Table 1 — Terminal functions

Terminal name	Description	Electrical characteristics
GND	Ground	Ground input
V _{DD}	Power supply voltage	1.8-V nominal
V _{REF}	Input reference voltage	0.9-V nominal
CK	Positive master clock input	Differential input
$\overline{\text{CK}}$	Negative master clock input	Differential input
C0, C1	Configuration control inputs - Register A or Register B and 1:1 mode or 1:2 mode select	LVC MOS inputs
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables V _{REF} data and clock differential-input receivers. When $\overline{\text{RESET}}$ is low all Q outputs are forced low and $\overline{\text{QERR}}$ output is forced high.	LVC MOS input
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	Chip select inputs – disables D1-D24 [†] outputs switching when both inputs are high	SSTL ₁₈ input
D1–D25	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$	SSTL ₁₈ input
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL ₁₈ input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL ₁₈ input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input.	SSTL ₁₈ input
Q1–Q25*	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS outputs
PPO	Partial parity out - indicates odd parity of inputs D1 - D25 [†]	1.8-V CMOS output
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
$\overline{\text{QERR}}$	Output error bit - Timing is determined by the device mode.	Open-drain output
NC	No internal connection	
DNU	Do not use - inputs are in standby-equivalent mode and outputs are driven low.	

[†] Data inputs = D2, D3, D5, D6, D8-D25 when C0=0 and C1=0

Data inputs = D2, D3, D5, D6, D8-D14 when C0=0 and C1=1

Data inputs = D1-D6, D8-D10, D12, D13 when C0=1 and C1=1

* Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0=0 and C1=0

Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0=0 and C1=1

Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0=1 and C1=1

2 Device standard (cont'd)

2.5 Function table

Table 2 — Function table (each flip flop)

Inputs						Outputs		
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS}}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	H	↑	↓	L	Q ₀	H	L
H	H	H	↑	↓	H	Q ₀	H	H
H	H	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

2 Device standard (cont'd)

2.5 Function table (cont'd)

Table 3 — Parity and standby function table

Inputs							Outputs	
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Σ of inputs = H (D1-D25) [†]	PAR_IN*	PPO	$\overline{\text{QERR}}$ **
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	H	L	↑	↓	Even	L	L	H
H	H	L	↑	↓	Odd	L	H	L
H	H	L	↑	↓	Even	H	H	L
H	H	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	PPO ₀	$\overline{\text{QERR}}_0$
H	X	X	L or H	L or H	X	X	PPO ₀	$\overline{\text{QERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	H

[†] Data inputs = D2, D3, D5, D6, D8-D25 when C0=0 and C1=0

Data inputs = D2, D3, D5, D6, D8-D14 when C0=0 and C1=1

Data inputs = D1-D6, D8-D10, D12, D13 when C0=1 and C1=1

* PAR_IN arrives one clock cycle (C0=0), or two clock cycles (C0=1), after the data to which it applies

** This transition assumes $\overline{\text{QERR}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{QERR}}$ is low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity duration or until RESET is driven low.

Table 4 — Parity Error Detect in Low-Power Mode[‡]

Input-Data Error Occurrence [¥]	1:1 Mode (C0=0, C1=0)		1:2 Register-A Mode (C0=0, C1=1)		1:2 Register-B Mode (C0=1, C1=1)	
	PPO Duration [€] ^ß	$\overline{\text{QERR}}$ Duration [€]	PPO Duration [€]	$\overline{\text{QERR}}$ Duration [€] ^ß	PPO Duration [€] ^ß	$\overline{\text{QERR}}$ Duration [€]
n-2	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n-1	2 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted	1 Cycles after LPM is de-asserted	1 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted
n	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected

[‡] If a parity error occurs before the device enters the low-power mode (LPM), the behavior of PPO and $\overline{\text{QERR}}$ is dependent on the mode of the device and the position of the parity error occurrence. This table illustrates the low-power-mode effect on parity detect. The low-power mode is activated on the n clock cycle when DCS and CSR go high.

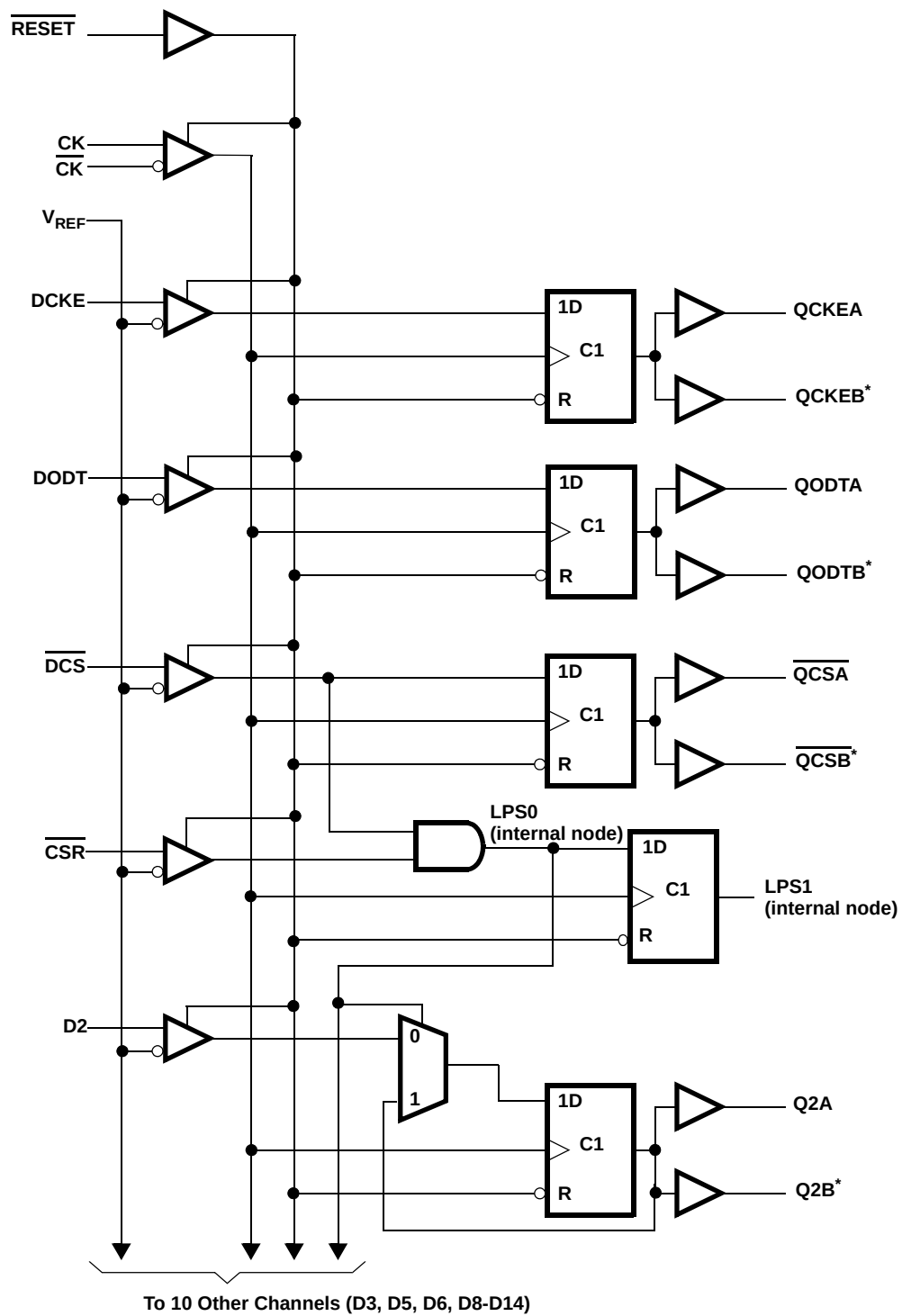
[¥] The clock-edge position of a one-cycle data-input error relative to the clock-edge (n) which initiates LPM at the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs.

[€] If an error occurs, the PPO output may be driven high and the $\overline{\text{QERR}}$ output driven low. These columns show the clock duration for which the PPO signal will be held high or the $\overline{\text{QERR}}$ signal will be held low.

^ß Not used.

2 Device standard (cont'd)

2.6 Logic diagram



* Disabled in 1:1 configuration

Figure 5 — Logic diagram 1:2 register-A configuration with C0=0 and C1=1 (positive logic)

2 Device standard (cont'd)

2.6 Logic diagram (cont'd)

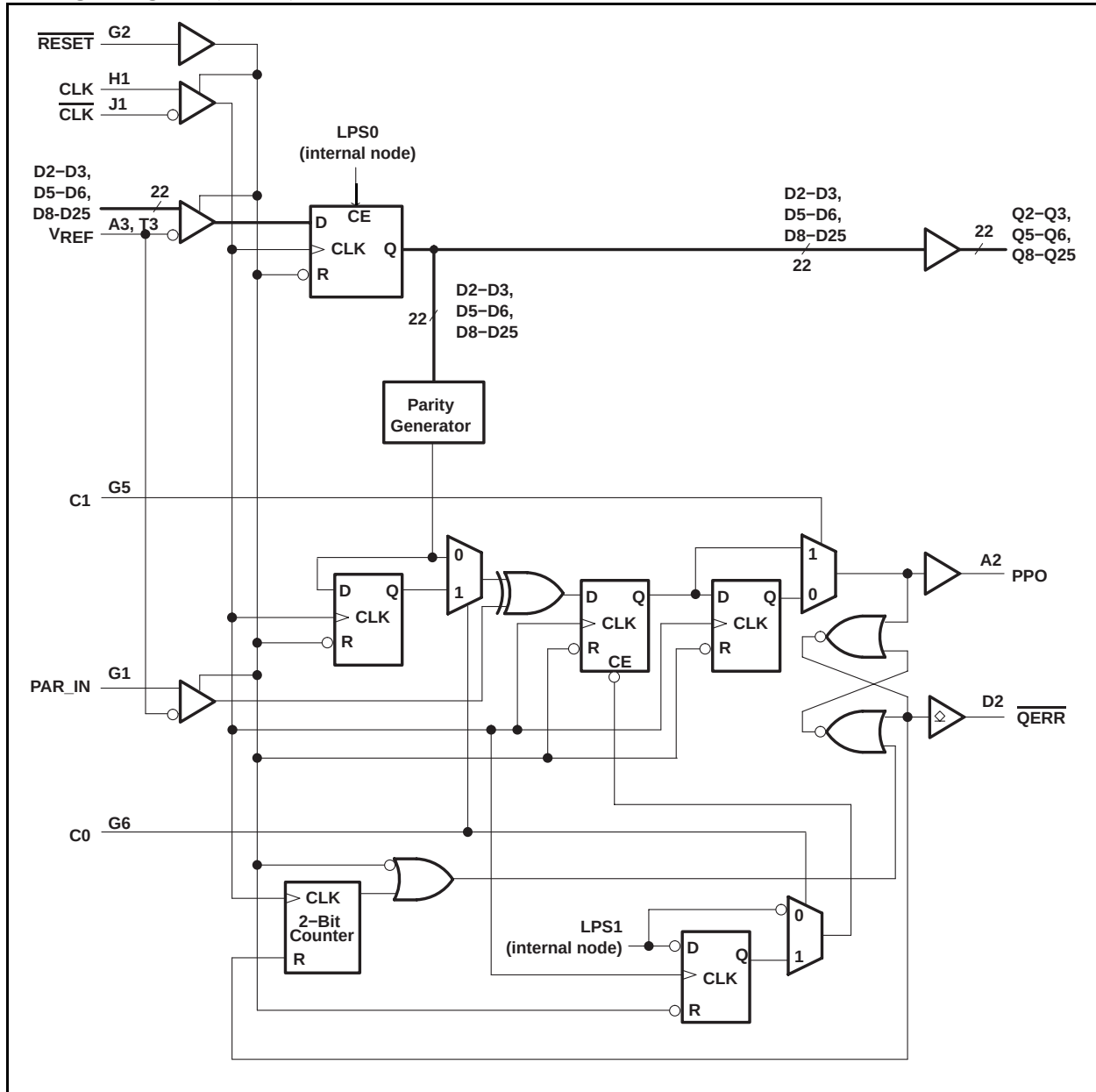


Figure 6 — Parity logic diagram for 1:1 register configuration (positive logic); C0=0, C1=0