

JEDEC STANDARD

Definition of CVP857 PLL Clock Driver for Registered PC1600, PC2100, PC2700 and PC3200 DIMM Applications

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STANDARD FOR DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700 AND PC3200 DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-03-86, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CVF857 PLL clock device for registered PC1600, PC2100, PC2700 and PC3200 DIMM applications.

The purpose is to provide a standard for a CVF857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Terms and definitions (for the purpose of this document)

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is specified for a V_{DDQ} of 2.5 V (PC1600, PC2100 and PC2700) and 2.6 V (PC3200); an AV_{DD} of 2.5 V (PC1600, PC2100 and PC2700) and 2.6 V (PC3200); and differential data input and output levels. Package options include plastic 48-pin Thin Shrink Small-Outline Package (TSSOP) and 40-pin Very Fine Pitch Quad Flat No-Lead Package (VFQFPN).

The device is a zero delay buffer that distributes a differential clock input pair (CK , $\overline{CK}$) to ten differential pair of clock outputs ($Y[0:9]$, $\overline{Y[0:9]}$) and one differential pair feedback clock outputs ($FBOUT$, $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK , $\overline{CK}$), the feedback clocks ($FBIN$, $\overline{FBIN}$), the 2.5-V LVCMOS input ($\overline{PWRDWN}$) and the Analog Power input (AV_{DD}). When input $\overline{PWRDWN}$ is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than approximately 20 MHz, which is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the $\overline{PWRDWN}$ input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair ($FBIN$, $\overline{FBIN}$) and the input clock pair (CK , $\overline{CK}$).

The PLL in the CVF857 clock driver uses the input clocks (CK , $\overline{CK}$) and the feedback clocks ($FBIN$, $\overline{FBIN}$) to provide high-performance, low-skew, low-jitter output differential clocks ($Y[0:9]$, $\overline{Y[0:9]}$). The CVF857 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

The CVF857 is characterized for operation from 0 °C to 70 °C.

3 Device standard (cont'd)

3.2 Pinout figure

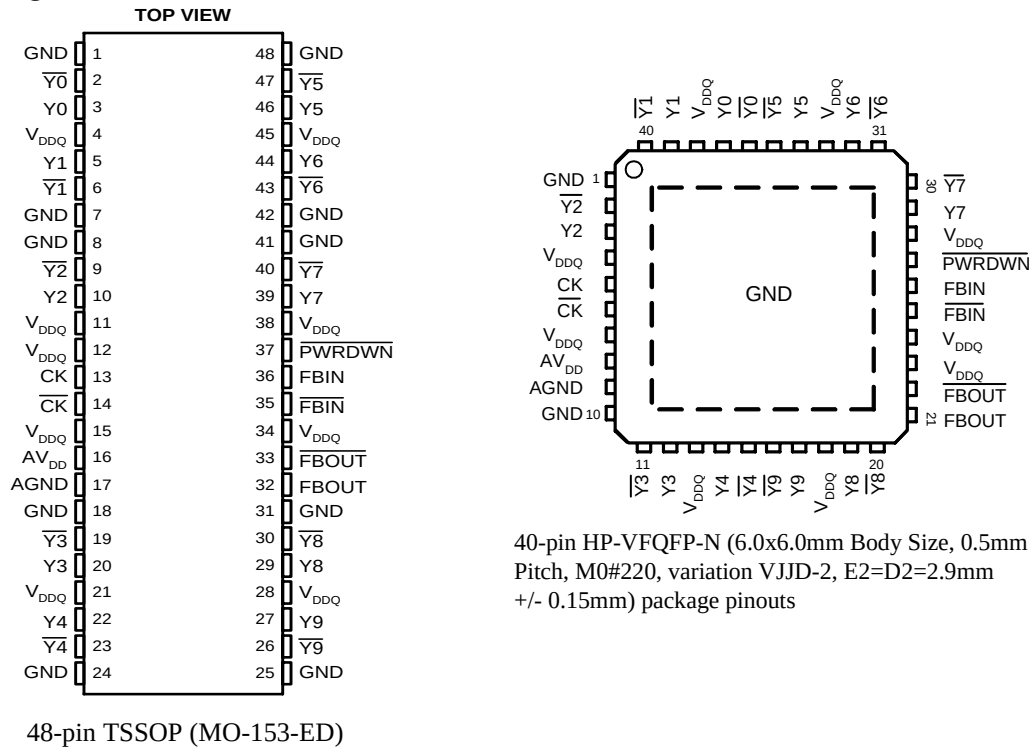


Figure 1 — 48-Pin TSSOP and 40-pin HP-VFQFP-N package pinouts

3.3 Terminal functions

Table 1 — Terminal Functions

Terminal Name	Description		Electrical Characteristics
AGND	Analog Ground		Ground
AV _{DD}	Analog power	PC1600, PC2100, PC2700	2.5 V nominal
		PC3200	2.6 V nominal
CK	Clock input		Differential input
$\overline{\text{CK}}$	Complementary clock input		Differential input
FBIN	Feedback clock input		Differential input
$\overline{\text{FBIN}}$	Complementary feedback clock input		Differential input
FBOU $\overline{\text{T}}$	Feedback clock output		Differential output
$\overline{\text{FBOU}}$	Complementary feedback clock output		Differential output
$\overline{\text{PWRDWN}}$	Power down		LVC MOS input
GND	Ground		Ground
V _{DDQ}	Logic and output power	PC1600, PC2100, PC2700	2.5 V nominal
		PC3200	2.6 V nominal
Y[0:9]	Clock outputs		Differential outputs
$\overline{\text{Y}}[0:9]$	Complementary clock outputs		Differential outputs

3 Device standard (cont'd)

3.4 Function table

Table 2 — Function table (see Note 1)

Inputs				Outputs				PLL
AV _{DD}	$\overline{\text{PWRDWN}}$	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	F _{BOUT}	$\overline{\text{FBOUT}}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
Nominal	H	L	H	L	H	L	H	On
Nominal	H	H	L	H	L	H	L	On
Nominal	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

NOTE 1 AV_{DD} Nominal is 2.5 V for PC1600, PC2100 and PC2700; and 2.6 V for PC3200.

3.5 Logic diagram

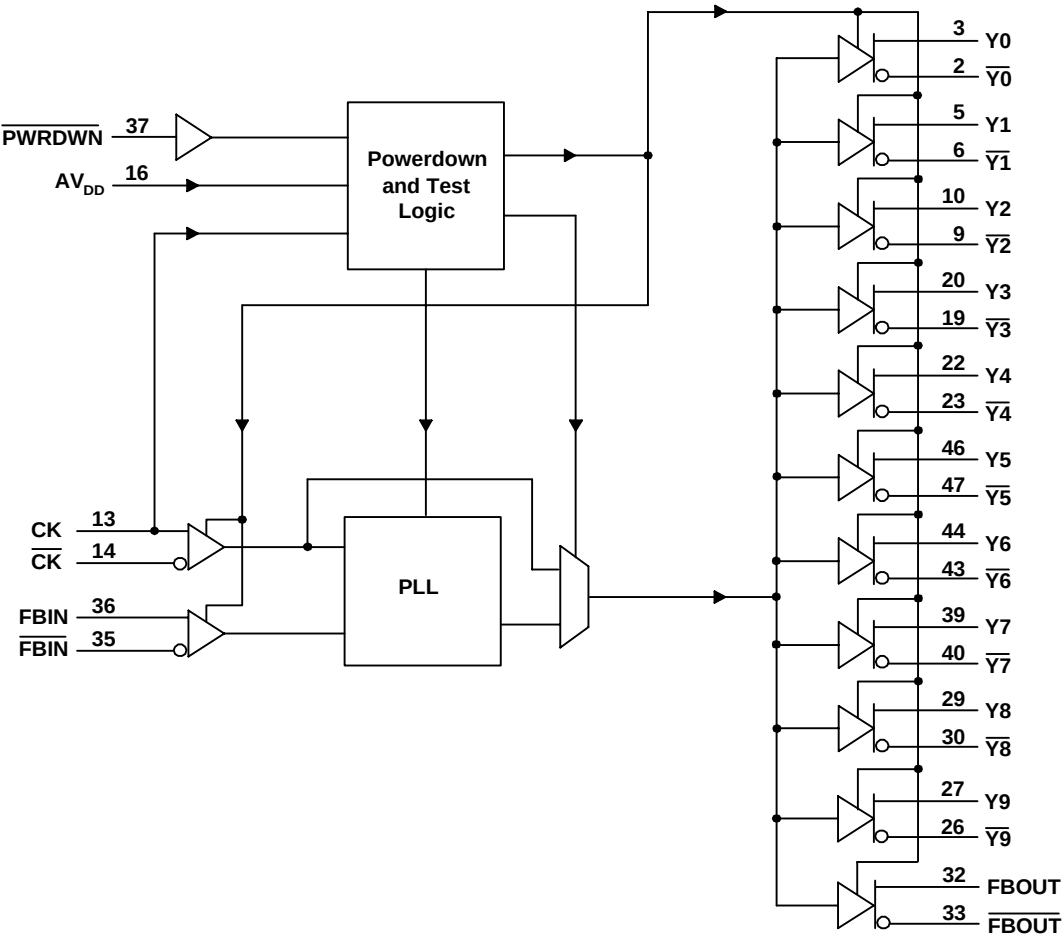


Figure 2 — Logic diagram (positive logic)

3 Device standard (cont'd)

3.6 Absolute maximum ratings

Table 3 — Absolute maximum ratings over operating free-air temperature range (see Note 2)

Supply voltage range, V_{DDQ} or AV_{DD}	–0.5 V to 3.6 V
Input voltage range, V_I (see Notes 3 and 4)	–0.5 V to $V_{DDQ} + 0.5$ V
Output voltage range, V_O (see Notes 3 and 4)	–0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DDQ}$)	±50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each AV_{DD} , V_{DDQ} or GND.	±100 mA
Storage temperature range, T_{STG}	–65 °C to 150 °C

NOTE 2 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3 The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 4 This value is limited to 3.6 V maximum.

3.7 Recommended operating conditions

Table 4 — Recommended operating conditions

			Min	Nom	Max	Unit
V_{DDQ}	Output supply voltage	PC1600-2700	2.3	2.5	2.7	V
		PC3200	2.5	2.6	2.7	V
AV_{DD}	Supply voltage	See Note 5,7	$V_{DDQ}-0.12$	V_{DDQ}	2.7	V
V_{IL}	Low-level input voltage	$\overline{PWRDWN}$	–0.3		0.7	V
V_{IH}	High-level input voltage	$\overline{PWRDWN}$	1.7		$V_{DDQ} + 0.3$	V
I_{OH}	High-level output current				12	mA
I_{OL}	Low-level output current				–12	mA
V_{IX}	Input differential-pair cross voltage		$(V_{DDQ}/2) - 0.2$		$(V_{DDQ}/2) + 0.2$	V
V_{IN}	Input voltage level		–0.3		$V_{DDQ} + 0.3$	V
V_{ID}	Input differential voltage, See Note 6	DC	0.36		$V_{DDQ} + 0.6$	V
		AC	0.70		$V_{DDQ} + 0.6$	V
T_A	Operating free-air temperature		0		70	°C

NOTE 5 The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operationing conditions and no timing parameters are guaranteed.

NOTE 6 V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

NOTE 7 $AV_{DD} \leq V_{DDQ}$ with a tolerance of 0.12 V.