

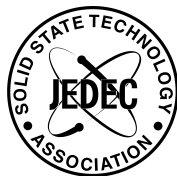
JEDEC STANDARD

Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications

JESD82

JULY 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
JEDEC Solid State Technology Association 2000
2500 Wilson Boulevard
Arlington, VA 22201-3834

This document may be downloaded free of charge, however EIA retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering
Documents, USA and Canada (1-800-854-7179), International (303-397-7956)**

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by the Electronic Industries Alliance and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS

(Formerly JEDEC Council Ballot JCB-00-22, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Background

1.1 Purpose

The purpose is to provide a standard for a CDCV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

1.2 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of a CDCV857 PLL clock device for registered DDR DIMM applications.

2 Definitions for the purpose of this document

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is designed for 2.5 V_{DD} and 2.5 AV_{DD} operation and differential data input and output levels. Package options include plastic Thin Shrink Small-Outline Package (TSSOP).

The device is a zero delay buffer that distributes a differential clock input pair (CK , $\overline{CK}$) to ten differential pair of clock outputs ($Y[0:9]$, $\overline{Y}[0:9]$) and one differential pair feedback clock outputs ($FBOUT$, $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK , $\overline{CK}$), the feedback clocks ($FBIN$, $\overline{FBIN}$), the 2.5-V LVCMOS input ($PWRDWN$) and the Analog Power input (AV_{DD}). When input $\overline{PWRDWN}$ is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than approximately 20 MHz, which is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the $\overline{PWRDWN}$ input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair ($FBIN$, $\overline{FBIN}$) and the input clock pair (CK , $\overline{CK}$).

The PLL in the CDCV857 clock driver uses the input clocks (CK , $\overline{CK}$) and the feedback clocks ($FBIN$, $\overline{FBIN}$) to provide high-performance, low-skew, low-jitter output differential clocks ($Y[0:9]$, $\overline{Y}[0:9]$). The CDCV857 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

The CDCV857 is characterized for operation from 0 °C to 70 °C.

3.2 Pinout figure

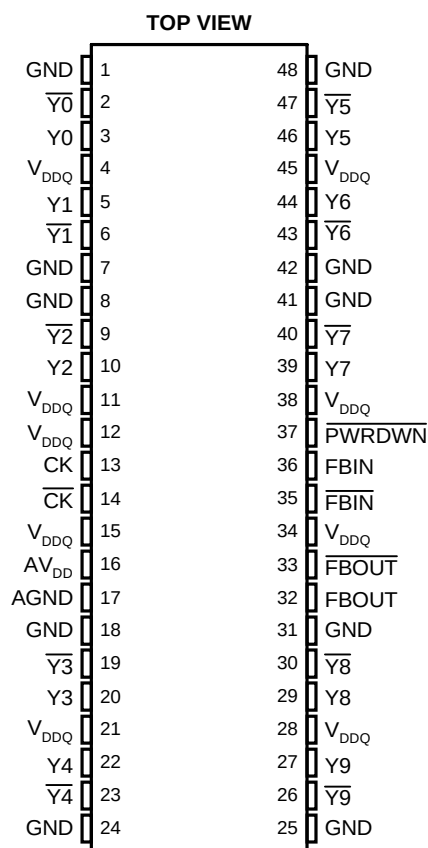


Figure 1 — 48-Pin dual inline package pinout

3.3 Terminal functions

Table 1 — Thermal functions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog power	2.5 V nominal
CK	Clock input	Differential input
$\overline{CK}$	Complementary clock input	Differential input
$FBIN$	Feedback clock input	Differential input
$\overline{FBIN}$	Complementary feedback clock input	Differential input
$FBOUT$	Feedback clock output	Differential input
$\overline{FBOUT}$	Complementary feedback clock output	Differential input
$\overline{PWRDWN}$	Power down	LVTMOS input
GND	Ground	Ground
V_{DDQ}	Logic and output power	2.5 V nominal
$Y[0:9]$	Clock outputs	Differential outputs
$\overline{Y}[0:9]$	Complementary clock outputs	Differential outputs

3.4 Function table

Table 2 — Function table

Inputs				Outputs				PLL
AV _{DD}	PWRDWN	CK	CK	Y	Y	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5V(nom)	H	L	H	L	H	L	H	On
2.5V(nom)	H	H	L	H	L	H	L	On
2.5V(nom)	X	<20MHz	<20MHz	Z	Z	Z	Z	Off

3.5 Logic diagram

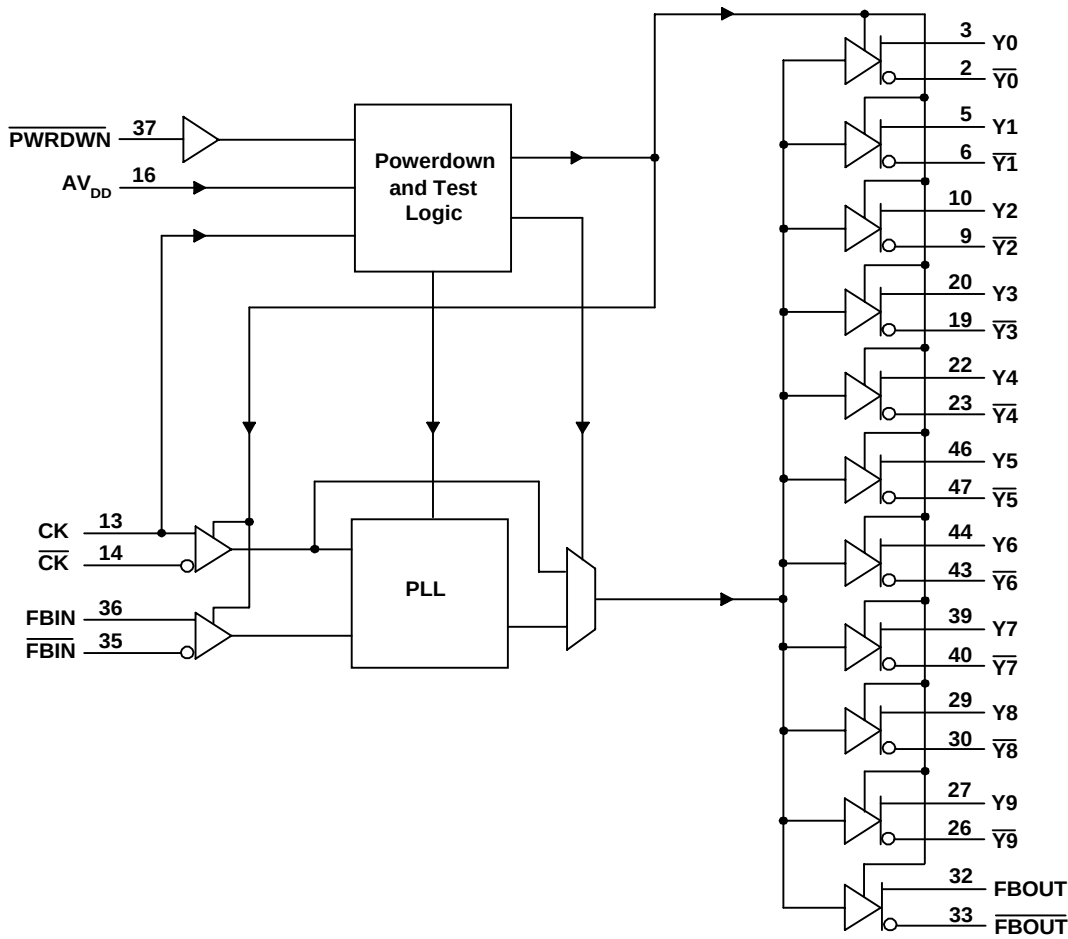


Figure 2 — Logic diagram (positive logic)