

JEDEC STANDARD

FBDIMM Advanced Memory Buffer (AMB)

JESD82-20A

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FBDIMM: Advanced Memory Buffer (AMB)

(From JEDEC Board ballot JCB-06-42 and JCB-08-75, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Introduction

This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification*. It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. The Advanced Memory Buffer is the buffer that isolates the DRAMs from the channel.

1.2 Advanced Memory Buffer Functionality

1.2.1 Advanced Memory Buffer

The Advanced Memory Buffer will perform the following FBD channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the *FB-DIMM Architecture and Protocol Specification* to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FBD configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

1.2.2 Transparent Mode for DRAM Test Support

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FBD I/O pins. This allows the tester to send an arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400.

Transparent mode functionality:

- Reconfigures FBD inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Uses low speed direct drive FBD outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

1.2.3 Debug and Logic Analyzer Interface

When optional LAI functionality is supported, the Advanced Memory Buffer can be used to support the connection of FBD links to a Logic Analyzer (LA) for debug.

Advanced Memory Buffer debug functionality:

- Reconfigures DDR2 interface to act as a Logic Analyzer Interface (LAI) to observe activity on FBD high speed links
- Triggers on programmable events in normal operation

1.2.4 DDR SDRAM

DDR2 SDRAM support:

- Supports DDR2 at speeds of 533, 667 and 800 MT/s
- Supports 256, 512, 1024, 2048 and 4096 Mb devices in x4 and x8 configurations
- 288 devices/channel (8 DIMMs/channel, 1 and 2 ranks/DIMM)
- 72-bit DDR2 SDRAM unregistered, unbuffered memory interface

1.3 Advanced Memory Buffer Block Diagram

Figure 1 is a conceptual block diagram of the Advanced Memory Buffer's data flow and clock domains.

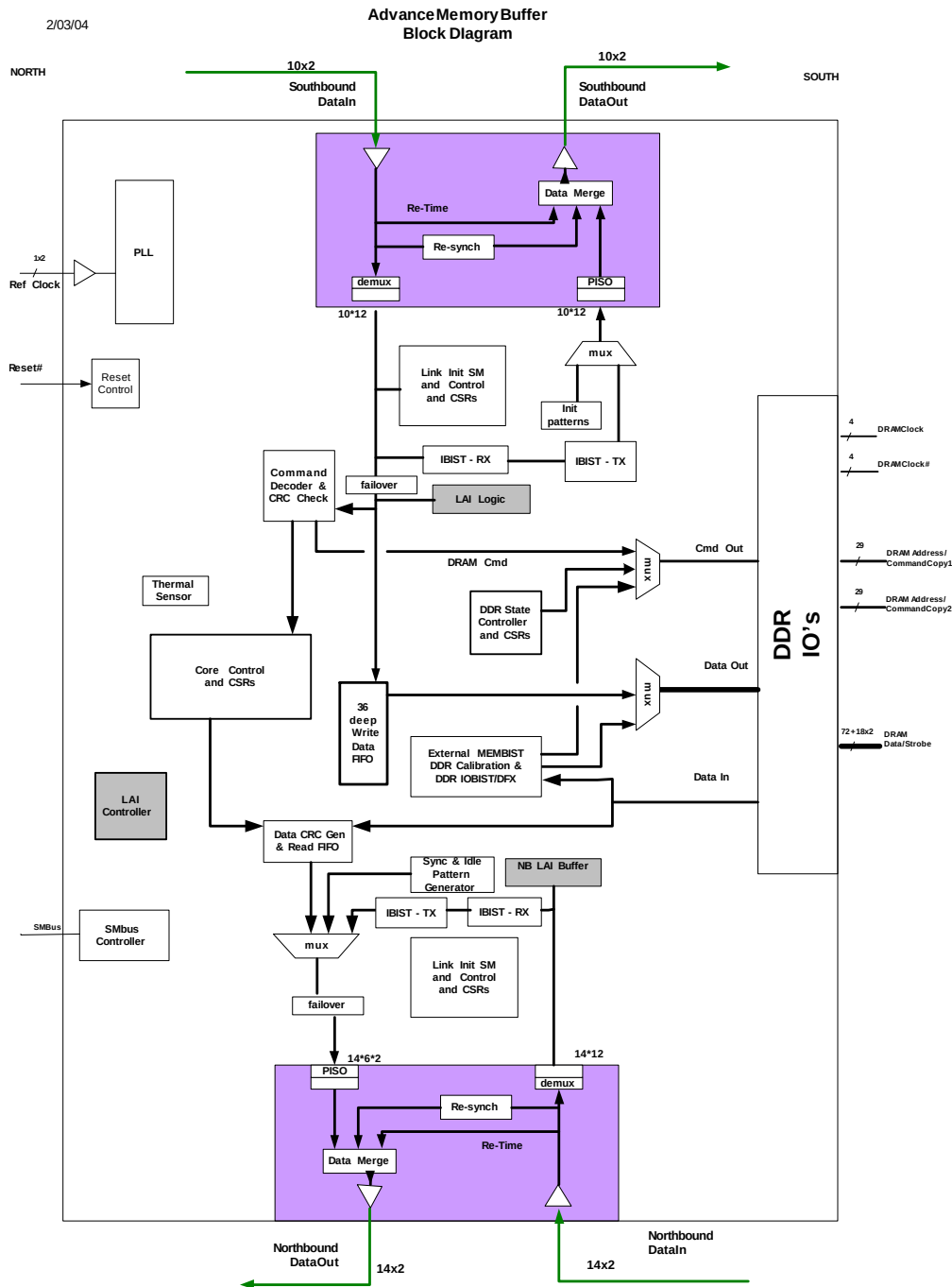


Figure 1 — Advanced Memory Buffer Block Diagram

1.4 Interfaces

Figure 2 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FBD links, one DDR2 channel and an SMBus interface. Each FBD link connects the Advanced Memory Buffer to a host memory controller or an adjacent FBD. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.

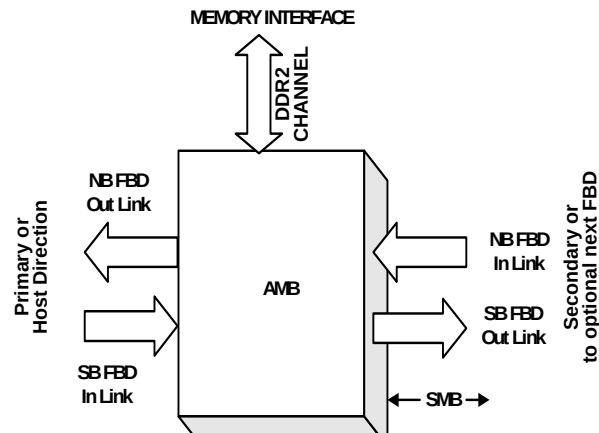


Figure 2 — Advanced Memory Buffer Interfaces

1.4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FBD Channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

1.4.2 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four-transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error (or equivalent implementation). Hardware aligns the read data and check-bits to a single core clock.

The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

1.4 Interfaces (cont'd)

1.4.3 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FBD link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to the Advanced Memory Buffer may be a requirement to boot a system. This provides a mechanism to set link strength, frequency and other parameters needed to insure robust operation given platform specific configurations. It is also required for diagnostic support when the link is down.

The SMBus address straps located on the DIMM connector are used by the Advanced Memory Buffer to get its unique ID.

More information is available in the SMBus chapter of this document.

1.5 References

This revision of the *Advanced Memory Buffer Component Specification* is consistent with the following documents:

- *FB DIMM Architecture and Protocol Specification*, [1]
- *FBD Design for Test, Design for Validation (DFx) Specification*, [2]
- *FB4300/5300/6400 DDR2 Fully Buffered DIMM Design Specification*, [3]
- *JEDEC DDR2 SDRAM Specification*, JC 42.3 [4]
- *High Speed Differential Point-to-Point Link at 1.5 V for Fully Buffered DIMM*, [5]
- *System Management Bus (SMBus) Specification Version 2.0 as published by www.smbus.org* [6]
- *Advanced Configuration and Power Interface Specification Version 2.0c as published by www.acpi.info* [7]

1.6 Glossary

Term	Definition
AMB	Advanced Memory Buffer
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device. The AMB employs an “x8” ECC, which means that all data from a partially or completely failed 8-bit device can be recovered without stopping the system. This same ECC provides the same level of coverage for 4-bit (“x4”) devices.
DDR	Double Data Rate (SDRAM)
DDR Branch	The minimum aggregation of DDR channels which operate in lock-step to support error correction. Two channels per branch supports x8 chip disable ECC. A rank spans a branch.
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an ADDR/CNTRL channel
DDR Data channel	A DDR data channel consists of 72 bits of data, divided into 18 data groups
DDR Data group	Each data group consists of 4 data signals and a differential strobe pair
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.

Term	Definition
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM “stacked” one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code. For the AMB, this is a chip disable code.
EMI	Electromagnetic interference
FBD Channel	Combination of 10 lane Southbound Links and 13 or 14 lane Northbound Links that make up a logical memory channel from host perspective
FBDIMM	Fully-Buffered DIMM
Frame	Group of bits containing commands or data
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBD channel
ISI	Inter Symbol Interference – see section “Initialization / Clocking” for definition
Mesochronous	Small ppm frequency difference.
NB	North Bound
NBI	North Bound Interface control logic
Northbound	The direction of signals running from the furthest DIMM toward the host.
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, <i>DDR SDRAM Specification</i>
LA	Logic Analyzer
LAI	Logic Analyzer Interface
Lane	Differential pair of receivers or transmitters
Link	High speed parallel Differential Point-to-Point interface
Page Replace aka Page Miss, Row Hit / Page Miss	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be precharged.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array.
Plesiochronous	Having the same frequency but arbitrary phase differences.
Primary	In the direction towards the Host controller
PLL	Phase Locked Loop
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature

Term	Definition
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g. a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module. The standard 4-slot DDR2 topology is limited to single rank DIMM due to loading constraints.
RAS	Reliability, Availability, Serviceability
Resample	A resampler is a serial data in and serial data out node that attenuates jitter by regenerating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the retransmitted data.
Resync	A resync repeater is a serial data in and serial data out node that resynchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes only, and not for compensating lane-to-lane skew. Both the jitter and voltage budgets for the retransmitted data are reset.
RPD	Return Path Discontinuity
SDRAM	Synchronous Dynamic Random Access Memory
SB	South Bound
SBI	South Bound Interface control logic
SI	Signal Integrity
Secondary	In the direction away from the Host controller
Serial Present Detect (aka SMBus protocol)	A 2-signal serial bus used to read and write control registers in the AMB and SDRAM
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Limited to 100 kHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSC	Spread Spectrum Clocking. Utilized to lower EMI
SSO	Simultaneously Switching Outputs
SSTL_18	Series Stub Terminated Logic for 1.8V
NB	North Bound
NBI	North Bound Interface control logic
Throttled	Temporarily prohibiting memory accesses when a thermal or electrical limit has been reached.
Transparent Mode	High speed FBD linked I/Os are bypassed with lower speed CMOS I/Os to allow lower speed tester to control and test DRAMs on the DIMM.
Unit Interval	Average time interval between voltage transitions of a signal
V _{SS}	Ground (0V)
V _{DDQ}	I/O buffer voltage for DDR2 buffers. Nominally 1.8V

2 FBD Channel Interface

2.1 Advanced Memory Buffer Support for FBD Operating Modes

The Advanced Memory Buffer (AMB) may not support all operating modes documented in the *FB-DIMM Architecture and Protocol Specification* [1]. The following list defines which features/modes are supported:

- 14 lane northbound (NB) with and without single lane Fail Over
- 13 lane NB with and without single lane Fail Over
- 10 lane southbound (SB) with and without single lane Fail Over
- Repeater mode
- Transparent mode
- Recalibrate state
- Voltage Margin Test

The following are optional FBD features :

- LAI mode
- 12 lane NB non-ECC
- L0s low power state
- Data mask
- Variable read latency
- Timing Margin Test

2.2 Channel Initialization

Refer to Chapter 3, “Channel Initialization” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD initialization protocol. The reset chapter covers some additional details about the initialization process.

2.3 Channel Protocol

2.3.1 General

Refer to Chapter 4, “Channel Protocol” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD protocol.

2.3.2 Timeouts during TS0

The FBDLOCKTO register is used to help the AMB determine when to give up waiting for individual lanes to bit lock. The NBLINKCFG field is used to communicate when lanes are intentionally not in use. The BLTOCNT field is used to set a time out on waiting for a lane to bit lock. Lanes not bit locked by this time will be marked as failed.

2.3 Channel Protocol (cont'd)

2.3.3 Recalibrate state considerations

In addition to what the FBD Architecture and Protocol specification describes around Recalibrate State, the AMB further requires that the host be sending NOP commands in at least the 2 frames preceding the exit from recalibrate state.

Requirement: 2 Cycles before the recalibrate counter expires, NOPs must be sent from the host.

Time	Frame Description	Recal Frame Counter
N	Sync with ERC bit set	0
N+1	NOP frame	RECALDUR
N+2	NOP frame	RECALDUR - 1
...	NOP frame	
N+8	NOP frame	RECALDUR - 7
N+9	NOP frame - host may begin recalibration	RECALDUR - 8
...		
N + RECALDUR - 7	NOP frame - host must be finished with recalibration	8
...		
N + RECALDUR - 3	NOP frame	4
N + RECALDUR - 2	NOP frame	3
N + RECALDUR - 1	NOP frame - must be received at AMB without corruption	2
N + RECALDUR	NOP frame - must be received at AMB without corruption	1
0	Valid Sync Frame	0

Recal Frame Counter:	5	4	3	2	1	0
Rx Data:	X	X	X	NOP	NOP	Valid Cmd
where X represents "don't care" data						

2.3 Channel Protocol (cont'd)

2.3.4 Address Mapping of DDR Commands to DRAMs

DDR2 x4 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	A12	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
DDR2 x8 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (32Mbx8)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (64Mbx8)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (128Mbx8)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (256Mbx8)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.3.5 FBD L0s State

The L0s state provides a low latency power down state for the FBD channel. The L0s state will nominally last for 41 frame times such that no sync packets are missed. The actual amount of time is programmable in the AMB. Times greater than 41 frames are not supported at this time. The L0s state may be used when the memory controller is throttling, and producing no transfers.

The duration of the L0s state is pre-programmed into the MC and AMB registers, and is triggered by a sync command with the L0s command indicated. The basic sequence is:

L0 to L0s Transition

- MC issues L0s command in the SYNC command.
- The MC continues sending one additional command, which is a NOP.
- AMB must gate its inputs and stop accepting commands following the NOP. It need not accept and decode the NOP itself.
- Southbound output drivers and input receivers are disabled following the NOP. The turnoff may be staggered for power supply di/dt reduction.
- Northbound channels are shut down following the status packet corresponding to the sync command.
- AMB takes CKE low to all DRAMs and floats the commands and address bus to the DRAMs (all signals except clock, CKE, and ODT).
- The PLL is never powered down before, during, or after the transition.

2.3 Channel Protocol (cont'd)

2.3.5 FBD L0s State (cont'd)

L0s to L0 Transition

- When the timer expires, interface must be fully functional and ready to receive the sync command. The turning on of circuits occurs the proper amount of time prior to the timer expiring, and is an implementation detail of the AMB.
- Southbound channel begins power-up. The drivers must begin driving a valid state one clock prior to the NOP below.
- The AMB drives command and address lines, and restores CKEs to their previous state with appropriate timing to be able to process a DRAM command which is received on the clock following the sync command.
- MC sends a NOP on the clock prior to the timer expiring. The receiver need not accept and decode the NOP itself.
- MC sends a sync command on the clock that the timer expires.
- Normal commands may commence.
- Northbound lanes are brought back in a similar manner to southbound lanes, but are timed to be able to successfully send the status packet response for the sync command.

Note: DRAM pages need not be closed during the power down, but any DRAM with open pages will consume additional power. This is solely a function of the MC policy.

Note: Upon return to L0, the MC may place the bus back into L0s by issuing another L0s command in the sync command.

2.4 Reliability, Availability, and Serviceability

2.4.1 General

Refer to Chapter 5, “Reliability, Availability and Serviceability” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD RAS requirements.

2.4.2 Channel Error Detection and Logging

See “Errors” chapter for details on the error handling.

2.5 Channel Configuration

2.5.1 Re-sync and Resample Modes

A separate control is available for both the NB and SB FBD links to select between lower latency re-sample and lower jitter re-sync modes for repeating received data. Selection between these two modes is a function of platform design and configuration and should be set by BIOS prior to link initialization

The FBDSBCFGNXT.SBRESYNCEN and FBDNBCFGNXT.NBRESYNCEN bits make this selection.

Descriptions of these two modes follows.

2.5 Channel Configuration (cont'd)

2.5.1.1 Accumulated Tracking Effects (Re-Sample Mode)

Each AMB acts as a repeater for the FBD channel. Since the data driven from each DIMM to the next DIMM may experience random or periodic phase shifts, the affect of these phase shifts must be accommodated in the design. Consider a system with three DIMMs daisy-chained together. A phase shift generated in the first DIMM will be seen by the second DIMM but will not be immediately propagated to the third DIMM. Unlike an analog buffer, the phase shift is not automatically driven to subsequent DIMMs since the data driven to the subsequent DIMMs is re-sampled in the AMB to reduce jitter. The lowest latency implementation would use the derived clock to retransmit the outbound signal. The second DIMM will see the phase shift as a slight change in the position of the data eye at its receiver. The clock tracking loop filter in the second DIMM will measure several bit cells and may eventually determine that it should adjust the phase of its derived clock to capture the data closer to the center of the new data eye location. Only when the second DIMM makes its phase change will the effect propagate to the third DIMM. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

2.5.1.2 Accumulated Tracking Effects (Re-Sync Mode)

An alternative implementation would place a voltage/thermal (VT) drift compensation buffer between the receiver and the transmitter section of the AMB I/O cell. The drift compensation buffer would re-synchronize the signal with a multiple of the reference clock. This buffer would have to be deep enough to handle the absolute magnitude of delay change of the daisy-chain channel over voltage and temperature. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

2.5.2 Other Channel Configuration Modes

Other channel electrical configuration parameters that should be set up prior to link initialization include

- Link frequency (LINKPARNXT.CFREQ)
- SB Transmitter drive current (FBDSBCFGNXT.SBTXDRVCUR)
- SB Transmitter de-emphasis values (FBDSBCFGNXT.SBTPREEMP)
- NB Transmitter drive current (FBDNBCFGNXT.NBTXDRVCUR)
- NB Transmitter de-emphasis values (FBDNBCFGNXT.NBTPREEMP)

The parameters contained in these registers are described more completely in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

Additional channel configuration registers that should be set up prior to link initialization include

- First 6 bytes of the SPD parameter registers
PERSBYTE[5:0]
- FBD Bit Lock Time Out Register (FBDLOCKTO)

2.5.3 Lane to Lane Skew on a Channel

The FBD Channel is expected to support a maximum skew of upto 46UI. The deskew buffers on an individual AMB need to be able to support this amount of accumulated skew. The actual skew observed will be a function of the skew introduced by platform layout, DIMM layout, the number of active AMBs in the channel and skew introduced by AMBs.

2.6 Repeater Mode

The AMB may also be used as an FBD link repeater to extend distances at which links can operate. This mode can be automatically set by the BFUNC and SA pins. In this mode, the AMB functions in the same way as a regular DIMM with the exception that DRAM commands are not supported.

Link behavior is the same as for normal DIMMs

- Participates in link initialization like a normal DIMM
- Responds to Reads and Writes to AMB configuration registers,
- status is returned in response to Sync commands,
- link errors are detected and alerts generated,

SMBus access is the same except for the base Slave address is different than from normal DIMM.

Slave address[6:3] = 4'b0011 for Repeaters, instead of

Slave address[6:3] == 4'b1011 for normal DIMMs

2.7 Performance

This section describes the performance characteristics of FBD: idle memory read latencies, loaded memory read latencies, channel throughput, and system memory capacity.

2.7.1 Idle Memory Read Latency

Memory read latency is an important factor in system level performance. Processor and I/O devices are often blocked from doing other work when reading from memory, until their read requests are satisfied. Therefore, minimizing the amount of time that it takes to satisfy a read request can increase the amount of work that a processor or I/O device can perform. This can improve overall system or benchmark performance.

Memory read latency (also referred as loaded memory read latency) consists of two components: idle memory read latency and queuing delays for various resources such as the front-side bus, memory controller queues, etc. Idle memory read latency is the latency of only one transaction running in the entire system, and is the least amount of latency that is possible for a read transaction. The following sections describe how to measure the FBD channel latency, as well as the overall system latency.

2.7.1.1 FBD Channel Latency

FBD channel latency is measured from the time a read request is driven on the FBD channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.

When not using the Variable Read Latency capability, the latency for a specific FBD DIMM on an FBD channel is always equal to the latency for any other FBD DIMM on that channel. However, the latency for each FBD DIMM in a specific configuration with some number of FBD DIMMs installed may not be equal to the latency for each FBD DIMM in a configuration with some different number of FBD DIMMs installed.

As more DIMMs are added to the FBD channel, additional latency is required to read from each DIMM on the channel. Because the FBD channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1 DIMM channel configuration.

The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host.

The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

2.7.1 Idle Memory Read Latency (cont'd)

2.7.1.1 FBD Channel Latency (cont'd)

The following table shows typical idle read latency, using DDR2 667 (4-4-4) DRAM technology (for a page empty read). Actual values depend on platform board and DIMM routing, AMB timing specs, DRAM characteristics. etc.

Table 1 — Example FBD-667 Channel Idle Memory Read Latencies

DIMMs per Channel	Typical Latencies
1	43-47 ns
2	49-53 ns
3	52-56 ns
4	58-62 ns

Table assumptions:

- Measure from latest valid SB output pin at host to latest valid NB input pin at host
- Includes 4UI serialization delay SB (A slot command) and 12 UI serialization delay NB
- Routing delay of 850ps from host to first DIMM and 600ps DIMM to DIMM
- 4-4-4 SDRAM Access Timing (24ns) plus 400ps Tdqsk
- On-DIMM Clk and DQS propagation delays of 800ps
- FBD SB Cmd In to DDR Clk out that Latches Cmd Out of 8.1ns +/- 1ns
- DDR Read Data In to FBD NB Out (last DIMM) of 5ns +/- 1ns
- Resample cross AMB delays of 1.25ns and Resync pass thru delays of 2.25ns
- First AMB in Resync and other AMBs in Resample mode

2.8 AMB Components of Channel Latency

The critical elements that AMB contributes to the latency calculation are the chip crossing delays.

- Southbound latency contributions
 - Delay from an input FBD link transaction to commands on the DDR interface and
 - Pass-thru delay of forwarded Southbound FBD transactions.
- Northbound latency contributions
 - Delay from DDR Read data input on the last DIMM to FBD link transactions and
 - Pass-thru delay of forwarded Northbound FBD transactions back towards the host.

These timing delay values are documented in Chapter 4, “Electrical, Power, and Thermal.”

2.8 AMB Components of Channel Latency (cont'd)

2.8.1 Command to Data Delay Calculation

Figure shows the various components that make up the over all delay through an AMB for a memory command.

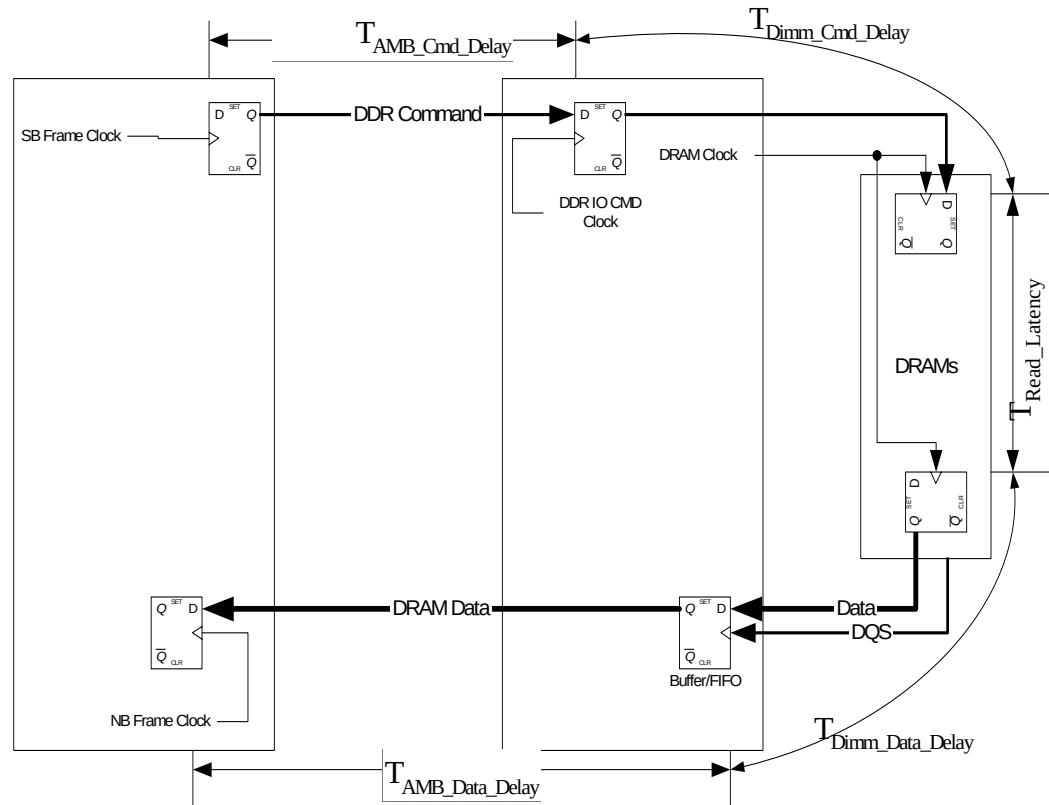


Figure 3 — Delays Through an AMB

The definition for terms used in the Figure are given below.

- UI: This is the unit interval on the FBD link. This is same as the period of the FBD link bit-rate clock.
- NB: Northbound
- SB: Southbound
- $T_{\text{Read_Latency}}$: DRAM Parameter. $T_{\text{CAS}} + T_{\text{Additive_Latency}}$
- $T_{\text{AMB_Cmd_Delay}}$: This value is very specific to an AMB implementation. This is the time it takes for the FBD command to be transferred from the point at which a deskewed and frame aligned command is available to core to the DDR I/O Cluster. This includes any differences between the FBD frame clock and the DDR I/O clock that latches the command into the DDR I/O cluster. This can be different for different DRAM frequencies.
- $T_{\text{AMB_Data_Delay}}$: This value is very specific to an AMB implementation. This is the minimum time it takes for the data that is returned from the DRAMs to be transferred from the DDR I/O cluster to the FBD I/O for transmission on the link. This includes any buffering and clocking delays for the data within the chip. This can be different for different DRAM frequencies.
- $T_{\text{Dimm_Cmd_Delay}}$: This includes the delays for the command through the DDR I/O cluster, differences between DDR I/O CMD Clock and DRAM clock, any routing delays for the clock and command on the DIMM and any set-up and hold-times in the AMB and the DRAMs.

2.8 AMB Components of Channel Latency (cont'd)

2.8.1 Command to Data Delay Calculation (cont'd)

- $T_{\text{Dimm_Data_Delay}}$: This includes the routing delays for the data and strobes from the DRAM to the AMB, skews between the DRAMs, delays through the DDR I/O cluster and any set-up and hold-times in the AMB and DRAMs.
- $T_{\text{CMD_To_Data}}$: This is equal to $(T_{\text{Read_Latency}} + T_{\text{AMB_Cmd_Delay}} + T_{\text{Dimm_Cmd_Delay}} + T_{\text{Dimm_Data_Delay}} + T_{\text{AMB_Data_Delay}})$. This can be specified with 1UI granularity. This will be different for each DRAM type. It does not include any delays inside the I/O to deskew and frame align the incoming data on the SB side nor does it include the delays inside the NB I/O on the transmit side.

The TCAS and TAdditive_Latency are specified in the DRC register (DRC.cl and DRC.al). The AL and CL values are latched from the DRC register during TS2's to establish $T_{\text{Read_Latency}}$. Later changes to AL and CL do not take effect for link data return timing until the next link reset.

The CMD2DATANXT register is initialized with a value equal to $(T_{\text{CMD_To_Data}} - T_{\text{Read_Latency}})$. This value of CMD2DATANXT is specified in the SPD EEPROM. All AMBs are expected to receive the data from the DRAMs with the calculated value of $T_{\text{CMD_To_Data}}$.

All AMBs power up with a default value of 5 for $T_{\text{CMD_To_Data}}$. This can be done either by setting the default values of DRC.CL and DRC.AL or by setting the default value of the CMD2DATACUR.FRMS to be 5. The AMBs must be able to return status and configuration register reads with this default timing. This will enable the BIOS to initialize the proper values from SPD.

The following simplified timing diagram illustrates how the last AMB uses the values specified in DRC.CL, DRC.AL, CMD2DATANXT.DLYFRMS and CMD2DATANXT.DLYFRAC.

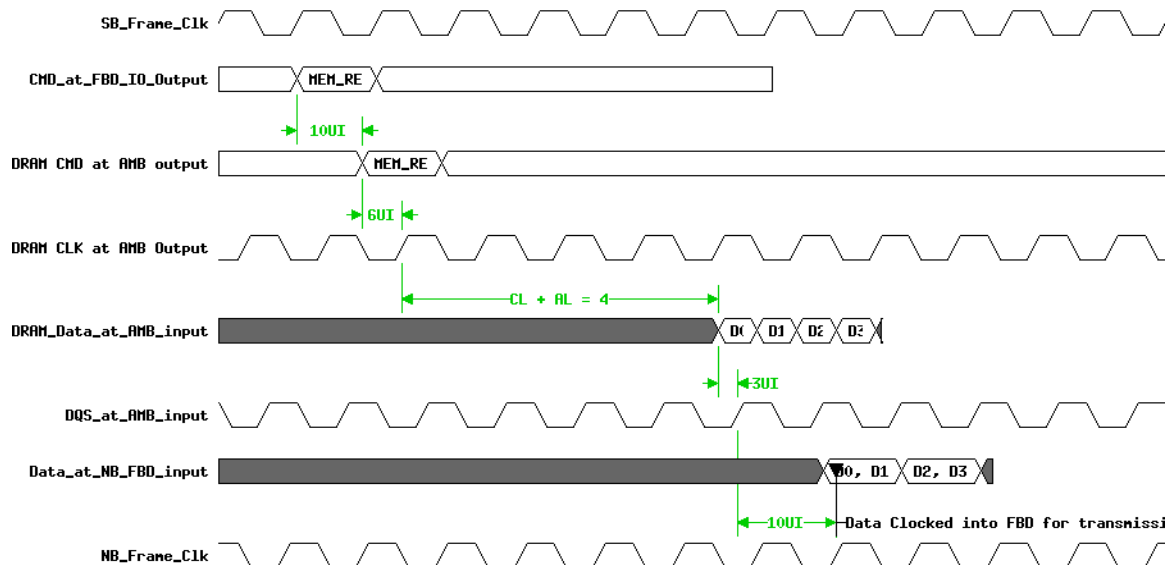


Figure 4 — Command to Data Delay Timing

In Figure , it is assumed that there are no routing delays on the DIMM itself. The command takes 10UI to get from SB FBD to the DDR I/O ($T_{\text{AMB_Cmd_Delay}}$). This includes time it takes to validate CRC of the frame and to decode the command. It is assumed DDR_IO_Cmd_Clk shown in Figure is delayed from the SB_Frame_Clk by 10 UI. The DRAM SCLK is placed at the center of the command window which adds an additional 6UI of delay. The DRAMs are programmed with a $T_{\text{Read_Latency}}$ of 4.

2.8 AMB Components of Channel Latency (cont'd)

2.8.1 Command to Data Delay Calculation (cont'd)

The DQS strobes are centered when they get to the AMB (3UI delay) and the data takes an additional 10 UI to propagate from the DDR I/O to the NB FBD I/O (including setup time at NB FBD and CRC generation) before it can be clocked into the NB FBD for transmission. The total delay without including the DRAM access time in this case is $(10 + 6 + 3 + 10\text{UI})$ 29UI. The CMD2DATANXT.DLYFRMS will be programmed with a value 2 and the CMD2DATANXT.DLYFRAC with 5UI. If the AMB supports only a 2UI granularity, then the values should be 2 frames and 6UI respectively. If an AMB does not support sub-frame delays, it is expected that the value in SPD will be round up to the nearest frame. Any additional delays caused by rounding up should be supported by additional buffering in the DDR I/O.

The above figure shows the last arriving data from the DDR. It is expected that any data arriving earlier than this, due to differences in routing, etc. is buffered up in some way inside the DDR I/O. The expectation is that all AMBs (last and intermediate) unload the data from the DDR I/O with the timing specified by the $T_{\text{CMD_To_DATA}}$. The Last AMB is expected to be able send data on the NB links with no additional delay added, if C2DINRCUR.INCRDLY is 0. Any additional delay needed due to the value programmed in C2DINRCUR.INCRDLY register in the last AMB or to delay the data in intermediate AMB before the merge, is handled by FIFOs in the AMB core.

In the above figure, it is assumed that the AMB can place the clocks in position shown above. If this is not the case, then additional delays due to non-optimal placement of the clocks should be taken into account to calculate the total delay to be programmed into the SPD.

2.8.2 Channel Throughput

2.8.2.1 Peak Theoretical Throughput

An FBD channel transfers read completion data on the FBD Northbound data connection. 144 bits of data are transferred for every FBD Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock-stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

The FBD frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FBD channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec.

Write data is transferred on the FBD Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBD Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

When the FBD frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec.

The total peak theoretical throughput for a single FBD channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the FBD frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBD-533 channel would be 6.4 GB/sec.

3 DDR Interface

3.1 Advanced Memory Buffer DDR Interface Overview

The DDR interface on the Advanced Memory Buffer consists of:

- A command decoder.
- A FIFO write buffer to hold the write data before it is written to the DDR channel. The write FIFO buffer has 36 entries of 72 bits (36 x 72b). A maximum of 35 entries can be used to store DDR bursts. Write data targeted for other Advanced Memory Buffer parts on the channel will use three of the 35 entries until the target Advanced Memory Buffer is known. The write FIFO buffer fills at half of the DDR data rate, and empties at the DDR data rate. The write FIFO buffer must support an invalidate write FIFO command (FBD Soft Reset command).
- A FIFO read buffer to hold the read data so that each DIMM returns data with the same latency as the southernmost DIMM in the chain. Latency is measured in increments of core clock periods. The core clock runs at the DDR command clock rate (half the data rate frequency). The latency through the FIFO read buffer on the southernmost DIMM is expected to be zero.
- A DDR cluster which serves as a DIMM buffer by registering outbound commands and data at output flops. The cluster also captures and levelizes incoming read data.
- A reset FSM which puts the DIMM in self-refresh when reset is asserted, and exits self-refresh when reset is deasserted and southbound frame training is complete.
- A calibration FSM that automatically sets the timing for DQS receiver enable and DQS delay or equivalent DDR timing control mechanism.
- A configuration register set to allow software to issue DRAM power up and DRAM MRS/EMRS commands. These registers are accessible through FBD channel commands and the SMBUS interface.
- "Burst Write Interrupt" is not supported.

3.2 Data Mapping

See the protocol chapter of the *FB DIMM Architecture and Protocol Specification* for the mapping between data in DDR DRAM devices and data in FBD frame formats for 4-bit and 8-bit devices.

3.2.1 Data Mask

Data mask is supported for non-ECC (64-bit) DIMMs only. The AMB is required to support data mask if it supports non-ECC DIMMs.

Non-ECC DIMMs using x4 DRAMs are not supported by the standard AMB pinout, as there are not adequate data mask pins available. 16 data mask pins would be required for proper load matching.

The data mask signals share pins with the DQS[16:9] pins. This puts them in the proper place on the package and die to be matched with the timing of the appropriate DQ pins. DQS#[16:9] are not used in this mode. The following table shows the mapping between DQS pins and data mask pins.

3.2 Data Mapping (cont'd)

3.2.1 Data Mask (cont'd)

Data Lane	Signal	x4 Usage	Non-ECC Usage	x8 or x16 ECC Usage
DQ[7:0]	DQS[9]/DM0	DQS[9]	DM0	Not used
DQ[15:8]	DQS[10]/DM1	DQS[10]	DM1	Not used
DQ[23:16]	DQS[11]/DM2	DQS[11]	DM2	Not used
DQ[31:17]	DQS[12]/DM3	DQS[12]	DM3	Not used
DQ[39:32]	DQS[13]/DM4	DQS[13]	DM4	Not used
DQ[47:40]	DQS[14]/DM5	DQS[14]	DM5	Not used
DQ[55:48]	DQS[15]/DM6	DQS[15]	DM6	Not used
DQ[63:56]	DQS[16]/DM7	DQS[16]	DM7	Not used
DQ[71:64]	DQS[17]	DQS[17]	Not used	Not used
As above	DQS[17:9]#	DQS[17:9]#	Not used	Not used

An AMB in non-ECC mode implies the following:

- 12 lane Northbound mode
- There is no Northbound fail-over mechanism.
- Data Mask Capability.
- Southbound write data frames use the Data Mask version of the frame format.
- 10 lane Southbound with fail-over capability.
- x4 DRAMs are not supported by the standard AMB pinout.

For AMB silicon that supports both ECC and non-ECC modes, there is no strapping signal to indicate which DIMM type it is installed on. The AMB will use the information in the configuration state, transferred from the host in the TS3 packet to determine ECC or non-ECC mode. If programmed for 12-bit northbound mode non-ECC mode is used. If programmed into 14-bit, 14-bit Fail Over, 13-bit, or 13-bit Fail Over modes, ECC mode is used. The host will determine the type of DIMM by reading the SPD.

3.3 Command / Address Outputs

The DDR2 command and address signals are terminated to 0.9V on the DIMM. In order to reduce power, this termination is performed using series resistors to a V_{tt} power supply, which is generated by voltage regulators on the system board and provided to the DIMM via connector pins. This power supply must be capable of sourcing and sinking current.

Two sets, or copies, of DRAM command and address output pins are provided for loading and timing considerations. Each set drives the same DRAM commands, but the two address busses are inverted from each other in order to reduce power consumption and heat produced on the DIMM. The command and address output pin behavior is detailed as follows:

1. Minimum address toggling. The address associated with the last command issued on the DRAM bus is retained during DRAM NOP/Deselect commands. The address and bank bits do not revert to all 1's (or all 0's) when the command bus is idle.

3.3 Command / Address Outputs (cont'd)

2. Balanced bank and address busses. With some exceptions, the bank and address busses on the two bus copies are inverted from each other. This minimizes the current load on the V_{TT} supply regulator because the balanced address bus sinks as much current as it sources. There are exceptions to the inversion behavior to allow for commands that use one or more address bits to control DRAM functionality. Balancing can also be disabled by setting the DRC.BALDIS register field.

Balancing Exceptions:

- a. Address bit A10 is not balanced during all read, write, and precharge commands.
 - b. No address or bank bits are balanced during any MRS and EMRS commands.
 - c. Some MEMBIST operations that are pattern specific. Note that this will limit the number of DIMMs that may run MEMBIST simultaneously.
 - d. No address or bank bits are balanced during any command when the DRC.BALDIS register field is set.
3. Balanced idle command bus. When the command bus is idle, a deselect command is issued with all chip selects high and all RAS/CAS/WE signals driven low on both command/address copies.
 4. Command/Address output control with CKE. All command and address pin outputs, except for ODT, CKE, and CLK, will float one DRAM clock cycle after both CKE pins transition from high to low. The command/address pins will be driven to valid signal levels on the same cycle that either CKE pin is driven from low to high.
 5. Output control during link reset (i.e. fast reset). When the Advanced Memory Buffer core logic is in reset, CKE and ODT will be driven low, and CLK will run at normal levels and frequency. The remaining command/address pins will float during reset.
 6. Command/Address output control in S3 mode. When the Advanced Memory Buffer core logic is in S3 power mode, CKE and ODT will be driven low. CLK and all the other command/address pins can be either driven low or tri-stated. In S3 mode, 1.8V supply is on. 1.5V and V_{tt} supplies are off. 3.3V supply can be either on or off depending on user's design. DRAMs are in self refresh, and the CKE signals must be driven low.
 7. CSR output control of command/address. All command/address pin outputs will float when the appropriate DRC bits are set. Setting the DRC.CADIS field will float the RAS, CAS, WE, Bank, and Address pins. DRC.CSDIS controls the chip select pins. DRC.ODTDIS, DRC.CKEDIS, and DRC.CLKDIS float the ODT, CKE, and clock pins respectively.

3.3.1 CKE Output Control

During normal operation the CKE outputs can be controlled directly with dedicated FBD channel commands and with configuration register writes to the DRC.CKEN0/1 CSR's. Channel commands that affect the CKE outputs are reflected in the DRC.CKEN0/1 CSR's. During channel fast reset events the self-refresh FSM controls the CKE outputs, as well as all other command/address outputs.

3.3.2 Memory Controller / BIOS requirements

The memory controller must take care to not issue multiple MRS/EMRS commands to multiple DIMMs simultaneously in rapid succession if the V_{tt} supply cannot handle the current.

The memory controller may also be required to limit the number of DIMMs in MEMBIST mode at the same time. V_{dd} power supply and thermal limitations may also put a limit on how many DIMMs may be in MEMBIST at one time. These will be system dependent.

3.4 DQS I/O and DM Outputs

Advanced Memory Buffer sends and receives source synchronous differential strobes (DQS) to transfer data (DQ/CB) during write and read DRAM transactions. DQS9 through DQS17 also support the data mask (DM) function in x8 mode. Setting the MTR.WIDTH configuration register enables x8 mode. When driving DM, the timing of the transition from floating, to driving, and back to floating is unchanged, but DQS[17:9] do not toggle and instead drive a constant level. DQSP[17:9] drive low and DQSN[17:9] drive high. In x8 mode DQS[17:9] are not used to capture read data. The table below lists which DQS signals are associated with which DQ/CB pins in x8 and x4 mode.

Table 2 — DQS association with DQ/CB pins in x8 and x4 mode.

DQS pin	x4 Mode: MTR.WIDTH=0		x8 Mode: MTR.WIDTH=1	
	Output Function	Input/Output Data Mapping	Output Function	Input/Output Data Mapping
DQS17	Write DQS	CB[7:4]	DM	N/A
DQS8	Write DQS	CB[3:0]	Write DQS	CB[7:0]
DQS16	Write DQS	DQ[63:60]	DM	N/A
DQS7	Write DQS	DQ[59:56]	Write DQS	DQ[63:56]
DQS15	Write DQS	DQ[55:52]	DM	N/A
DQS6	Write DQS	DQ[51:48]	Write DQS	DQ[55:48]
DQS14	Write DQS	DQ[47:44]	DM	N/A
DQS5	Write DQS	DQ[43:40]	Write DQS	DQ[47:40]
DQS13	Write DQS	DQ[39:36]	DM	N/A
DQS4	Write DQS	DQ[35:32]	Write DQS	DQ[39:32]
DQS12	Write DQS	DQ[31:28]	DM	N/A
DQS3	Write DQS	DQ[27:24]	Write DQS	DQ[31:24]
DQS11	Write DQS	DQ[23:20]	DM	N/A
DQS2	Write DQS	DQ[19:16]	Write DQS	DQ[23:16]
DQS10	Write DQS	DQ[15:12]	DM	N/A
DQS1	Write DQS	DQ[11:8]	Write DQS	DQ[15:8]
DQS9	Write DQS	DQ[7:4]	DM	N/A
DQS0	Write DQS	DQ[3:0]	Write DQS	DQ[7:0]

3.5 Refresh

3.5.1 Self-Refresh During Channel Reset

The Advanced Memory Buffer is required to manage DRAM refresh during channel resets and when refresh is enabled through the DAREFTC CSR. When a channel reset event is detected, the Advanced Memory Buffer will take the DRAM's from an unknown state and put them into self-refresh mode. The Advanced Memory Buffer does not track the DRAM state during normal operation, and so has a single process for getting from any DRAM state starting point to the self-refresh state.

When a reset event is detected, the Advanced Memory Buffer's self-refresh FSM will execute the following steps:

1. Clear the DAREFTC.AREFEN CSR to stop the Advanced Memory Buffer auto-refresh engine if enabled.
2. Block all DRAM commands, except those initiated by the self-refresh FSM.
3. Wait until any in-process read or write commands complete, with a minimum wait time of DSREFTC.TCKE, the DRAM "Minimum CKE pulse width time" specification. In-process reads/writes must complete to ensure that the DRAM ODT control outputs are driven low. The minimum time allows for the case where self-refresh entry or power-down entry was executed just before the channel reset.
4. Assert both CKE output pins by setting the DRC.CKE0/1 CSR fields. This will have no effect on the DRAM's if the CKE pins were already asserted.
5. Wait DSREFTC.TXSNR, the DRAM's "Exit self-refresh to a non-read command" specification, to allow any in process DRAM command to complete. This allows time to complete any command that may have been issued just before the channel reset event, such as an auto-refresh, as well as allows for self-refresh exit that may have been initiated when the self-refresh FSM asserted the CKE pins high.
6. Issue a "precharge all" command to both ranks. This guarantees that the DRAM's will be in an "idle" state.
7. Wait as required by DSREFTC.TRP, the DRAM "Precharge time."
8. Issue an auto-refresh command to both ranks. This meets the DRAM requirement that at least one auto-refresh command is issued between any self-refresh exit to self-refresh entry transition.
9. Wait as required by DAREFTC.TRFC, the DRAM "Refresh to active/refresh command time."
10. Issue a self-refresh entry command to both ranks.

When the channel comes out of "fast reset" (exiting the FBD link disable state), the Advanced Memory Buffer will automatically issue a self-refresh exit command to both ranks after the FBD Link Testing State is reached and the Advanced Memory Buffer core clock is stable. Note that this does not apply when the DISSREXIT bit is set as it should be when the Advanced Memory Buffer is powering up, when exiting S3 mode, or when exiting a channel reset that is a part of powering up or exiting S3 mode.

3.5.2 Automatic Refresh

The Advanced Memory Buffer has a refresh FSM for issuing auto-refresh commands to the DRAM's on regular intervals. This can be enabled when the DRAM bus is otherwise idle, but not during any other mode that generates DRAM commands, including DRAM power up and initialization, DDR I/O calibration, and normal operation where the FBD channel issues DRAM commands. The DAREFTC CSR controls the refresh interval and period.

3.6 Back to Back Turnaround Time

The host controller is required to observe a turnaround time on the DRAM data pins within a DIMM when switching between read and write cycles, and when switching from reads from one rank vs. the other rank on the DIMM. The nominal turnaround time is one clock for each parameter, which is the minimum time required to prevent a collision of the postamble of the first transaction and preamble of the second transaction. Additional clocks may be required by the DIMM, especially at higher speeds.

The three timing parameters are:

- Read to write turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from either rank and a write cycle to either rank.
- Write to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a write to one rank and a read from either rank. The write to read turnaround time to the same rank will generally be dominated by the tWTR specification, which must also be observed.
- Read to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from one rank and a read from the opposite rank.

These parameters are dependent on the AMB design and the DIMM PC board layout. The parameters are stored in the SPD. Each parameter is a 2 bit field allowing 0 to 3 additional clocks of turnaround time. See the *SPD Specification* for additional details.

Figure 5 shows the nominal turnaround times, with no additional clocks. Note that the DQS preamble and postamble may merge slightly when the first transaction is at worst case timings and the second transaction is at best case timings.

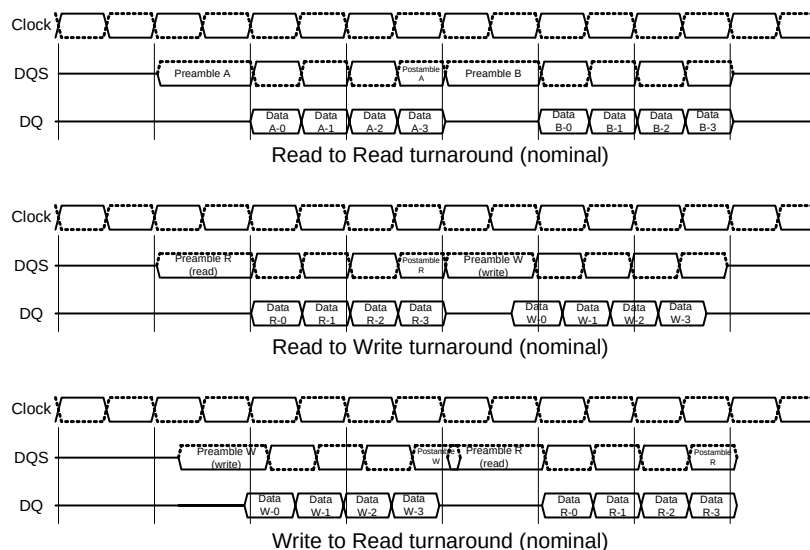


Figure 5 — Nominal Turnaround Time Timing Diagram

3.7 DDR Calibration

The following sections describe these DDR calibration and initialization features:

- DRAM initialization and (E)MRS command CSR's and FSM
- DQS failure CSR
- DQS receive enable calibration
- DQS delay calibration

3.7 DDR Calibration (cont'd)

3.7.1 DRAM Initialization and (E)MRS

The Advanced Memory Buffer provides a set of CSR's that allow BIOS to manage DRAM power up initialization and set DRAM mode register bits. All commands needed for DRAM initialization can be generated, including precharge, refresh, mode register set (MRS), and extended mode register set EMRS commands. The initialization/ (E)MRS FSM only controls the issuing of single commands, and does not automatically initialize the DRAM. It is the responsibility of software to control the command sequence to correctly initialize the DRAM.

The set of CSR's include the DCALCSR and DCALADDR registers. The fields of these CSR's are described in detail in the configuration register chapter.

The DCALCSR is used to select the command to be issued, which ranks to select, start the FSM that issues the command, and provide completion status.

The DCALADDR sets the bank and address issued to the DRAM, and therefore defines the type of (E)MRS to be issued, including limited OCD commands. DCALADDR[31:16] defines the DDR address bus during these commands, and DCALADDR[2:0] defines the ddr bank address bus.

3.7.1.1 OCD EMRS commands

FB DIMM DRAM timing is set up to work with OCD default calibration. Using the MRS/EMRS registers an EMRS OCD default is sent to the DRAMs. When the DCALCSR bit 31 is cleared to zero, an OCD exit command needs to be sent. When the DCALCSR bit 31 is cleared to zero the DRAMs should be in the default state.

Sending OCD EMRS drive(0), drive(1), adjust or exit OCD cal may have implementation dependent outcomes and should not be used in normal operation.

3.7.1.2 MRS Command Example

The following example shows how to send out an MRS command:

1. Write a value of 0x02320000 to the DCALADDR csr. This will configure the address/bank bus for an MRS command with burst length 4, CAS latency 3, and write recovery 2.
2. Write a value of 0x80000003 to the DCALCSR. This selects the (E)MRS command mode and initiates the FSM that will issue the command.
3. Poll the DCALCSR until bit 31 is cleared to zero by hardware. This indicates that the FSM has completed the selected operation.

3.7.2 Automatic DDR Bus Calibration

The Advanced Memory Buffer has two automatic DDR bus calibration functions that must be executed before read data can be captured reliably. These functions issue a series of write and read transactions on the DRAM bus, analyze the read data captured, and program a set of calibration results configuration registers. During subsequent operations, these configuration registers control the DDR I/O circuits and ensure proper data capture. DIMM memory contents are not preserved during calibration. Calibration can take up to several ms to complete. The following steps run the calibration:

1. Program the DCALCSR to 0x8000000c. This selects and initiates the first of two calibrations.
2. Poll the DCALCSR until bit 31 is cleared to zero by hardware.
3. Program the DCALCSR to 0x80000005. This selects/initiates the second calibration.
4. Poll the DCALCSR until bit 31 is cleared to zero by hardware.

3.7.3 S3 Recovery Configuration Registers

The following CSRs should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin.

- DRC
- MTR
- DSREFTC
- DAREFTC
- S3RESTORE[15:0]
- SPDPAR[15:0] - SPD Personality Bytes

Note: Refer to "Advanced Configuration and Power Interface Specification Version 2.0c" as published by www.acpi.info for S3 mode definition.

3.7.4 Receive Enable Calibration

The DQS input receiver needs to be disabled when the DDR bus is floating (tri-stated), e.g. between the read and write data transfers. Otherwise, the floating strobe would cause spurious data to be written into the read data FIFO. Also, the DQS input receiver needs to be disabled during a write so that the write data strobes do not cause unwanted data or check-bits to be written into the read data FIFO.

During a read, the DRAM's initially drive the DQS signals low for a full cycle. This is the preamble. After the preamble, the DQS signals are toggled twice per cycle, for every cycle there is a data transfer, which is determined by the configured burst length and the number of back-to-back read commands that were issued to the selected rank. After the last DQS falling edge, the DQS signal is driven low for a half cycle. This is the post-amble. After the post-amble the DQS signals are tri-stated.

The Advanced Memory Buffer automatically finds the end of the preamble of each of the 18 DQS pairs on the DDR bus. That is, it finds the location of the first waveform transition that defines the end of the preamble of each DQS pair. Once this is complete, the Advanced Memory Buffer calculates the location of the center of the preambles, and stores this information for use during read transactions. Receiver calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM.

3.7.5 DQS Delay Calibration

The DQS Delay calibration adjusts the Advanced Memory Buffer's on-chip delay circuits that align DQS signals to the center of their associated DQ/CB data eyes at the capture flops in the DDR I/O cluster. This maximizes the DQ/CB setup and hold time at these flops, which capture source synchronous data from the DDR data bus.

DQS delay calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM. The calibration is accomplished by issuing a series of write and read transactions, and comparing expected to captured data.

3.8 DDR MEMBIST

The AMB supports memory self test for memory initialization during system boot up and for testing the installed memory. During DIMM manufacturing this mode may be used to apply tests at speed to test the AMB-DRAM interface. The table below describes the features of the MEMBIST engine.

At system level MEMBIST may be executed on multiple DIMMs simultaneously. This is expected to speed memory test during system boot.

3.8 DDR MEMBIST (cont'd)

During DIMM manufacturing, MEMBIST offers a fast method to detect assembly-related defects, interface defects and the majority of core-related defects during DIMM manufacturing. This testing may be initiated either in or out of band, making MEMBIST compatible with motherboards, low cost ATE, or standalone equipment such as continuity testers. During motherboard testing an FBD-enabled system will be required for in-band.

Transparent mode will be used for memory core testing while BIST will be more useful for DRAM interface testing. For this reason there is no plan to specify a comprehensive BIST capability. Traditional system test methods will be used for operating system or application-based testing of the memory subsystem. This may include existing memory stress tests, applications or other tests selected by the DIMM manufacturer.

3.8.1 MEMBIST Features

DATA Type

1. Fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
2. 144-bit user defined data pattern and inverted user defined data pattern
3. 32-bit user defined circular shift data pattern
4. Random data generated from LFSR 32-bit CRC data

Those data patterns combined with addressing should be sufficient to test memory interface defect and DIMM assembly-related defect.

Address Type

1. Increased or decreased address type controlled by user
2. FastX, FastY, FastXY support
3. User defined test address range

DRAM Timing Parameter

1. BL4/BL8 support.
2. Various DDR2 DRAM timing support.
3. DRAM Refresh

Failure status:

1. Pass/Fail indicator, test abort, and halt on error features.
2. Up to five failure address recording.
3. Record one, and optionally up to 4, sets of 144 bits failure data.
4. 144 bit failure data location accumulator through entire test.

3.8.1 MEMBIST Features (cont'd)

Table 3 — MEMBIST Feature Summary

Failure Status	Pass/Fail indicator
Address Pattern	
X address bits	15-16
Y address bits	15-16
Z address (bank) bits	3
Address pattern in tests	User defined init/end physical address scan with increased/decreased FastX, FastY, FastXY support.
Failure Address logger	Up to 5 failure address loggers.
Data Patterns	
Fixed data pattern	fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
User defined data pattern	144 bit data, defined in 5 MBDATA registers by user
LFSR	LFSR (CRC32),
Data Error logger	First 144 bit failure data logger
	144 bits lane failure data location
	Halt on error or run to completion of test
	Test abort during the test
DRAM Timing control	
Programmable Timings	
tCL, tRCD, tRP, tWR, tRC	various DDR2 DRAM timing support
BL	4 or 8
Refresh control	Capable of various DDR2 refresh intervals
BIST Engine	
Access method	all registers and settings could be accessed from FSB or SMBus
DRAM data width	x4 or x8
DRAM initialization and mode register settings	statically set by host
Pattern execution method	SMBus or Host
Failure data access	Failing data is available for read out by the host/SMBus at completion of test
Algorithms Support	
Notation: ^ = increasing addr from start to end v = decreasing addr R/W = Read/Write D/I = Data/ Inverted Data number = sequence of events	

Table 3 — MEMBIST Feature Summary

Failure Status	Pass/Fail indicator
Scan	$\wedge$ (WD1); $\wedge$ (RD2); $\wedge$ (WI3); $\wedge$ (RI4)
Init	$\wedge$ (WD1)
DATA retention	$\wedge$ (WD1); Pause; $\wedge$ (RD2)
Mats+	$\wedge$ (WD ₁); $\wedge$ (RD ₂ , WI ₃); $\vee$ (RI ₄ , WD ₅);
MarchC–	$\wedge$ (WD1); $\wedge$ (RD2, WI3); $\wedge$ (RI4, WD5); $\vee$ (RD6, WI7); $\vee$ (RI8, WD9); $\vee$ (RD10);
Read	$\wedge$ (RD ₁);

3.9 DIMM Organization

The Advanced Memory Buffer supports DIMMs with 1 or 2 independent ranks (chip-selects). Each rank consists of 18 4bit DDR SDRAM devices or 9 8bit DDR SDRAM devices. Dual rank DIMMs consist of 36 4bit DDR SDRAM devices or 18 8bit DDR SDRAM devices. Non-ECC DIMMs could also be built with 16bit DDR SDRAM devices .

4 Electrical, Power, and Thermal

This chapter contains a description of the Advanced Memory Buffer's (AMB) electrical DC parameters, timing parameters, power considerations, and thermal considerations.

4.1 Electrical DC Parameters

4.1.1 Absolute maximum ratings

Table 4 contains absolute maximum ratings over operating free-air temperature range (see Note 1).

Table 4 — Absolute maximum ratings over operating free-air temperature range (see Note 1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage DRAM Interface	−0.5	+2.3	V
V_{IN} (DDR2), V_{OUT} (DDR2)	Voltage on any DDR2 interface pin relative to Vss (See Notes 2 and 3)	−0.5	+2.3	V
I_{INK} ($V_{IN} < 0$ or $V_{IN} > V_{DD}$)	Input clamp current		±30	mA
I_{OUTK} ($V_{OUT} < 0$ or $V_{OUT} > V_{DD}$)	Output clamp current		±30	mA
I_{OUT} ($V_{OUT} =$ 0 to V_{DD})	Continuous output current		±30	mA
N/A	Continuous current through each V_{DD} or GND		±100	mA
V_{CC}	Supply voltage for Core and High Speed Interface	−0.3	+1.75	V
T_{stg}	Storage temperature range	−55	+100	°C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This value is limited to 2.3V maximum.

4.1.2 Normal Mode

Table 5 contains the electrical DC parameters for the Advanced Memory Buffer part in normal mode.

Table 5 — Advanced Memory Buffer Normal Mode DC Electrical Parameters

Parameter		Units	Min	Typ	Max
V _{CC} link / core	0kHz - 30kHz	Volts	1.455	1.5	1.575
V _{DD}		Volts	1.7	1.8	1.9
V _{DDSPD}		Volts	3.0	3.3	3.6

NOTE There will also be a V_{TT} termination supply at V_{DD}/2 available on the DIMM but does not connect to the Advanced Memory Buffer.

Table 5A contains the electrical DC+AC parameters for the Advanced Memory Buffer part in normal mode.

Table 5A — Advanced Memory Buffer Normal Mode DC+AC Electrical Parameters

Parameter		Units	Min	Typ	Max
V _{CC} link / core	30kHz - 1MHz	Volts	1.425	1.5	1.590

NOTE There is also a +7/-5% tolerance allowed for current load steps associated with initialization/error-recovery state transitions, such as into and out of EI, IBIST, and MEMBIST. For these transitions, a temporary voltage overshoot is expected and acceptable as long as it is within +7% (step transition for 20μs and max duty cycle of 10⁻⁶). Transitions between Active and Idle states are not included in this +7%/-5% tolerance.

Table 6 contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 6 — AMB Power Specification Parameters and Test Conditions

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Idle_0	Idle Current, single or last DIMM L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
	Idd_Idle_0 Total Power			W	
Idd_Idle_1	Idle Current, first DIMM L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
	Idd_Idle_1 Total Power			W	
Idd_Idle_2	Idle Current, DRAM power down L0 state, idle (0 BW) Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
	Idd_Idle_2 Total Power			W	

Table 6 — AMB Power Specification Parameters and Test Conditions

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Active_1	Active Power L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_1 Total Power				W	
Idd_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_2 Total Power				W	
Idd_L0s	Channel Standby Average power over 42 frames where the channel enters and exits L0s. DRAMs Idle (0 BW). CKE low. Command and address lines floated DRAM clock active, ODE and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_L0s Total Power				W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Training Total Power				W	

Assumptions for all parameters:

Primary channel Drive strength at 100% with De-emphasis at -6.5dB

Secondary channel drive strength at 60% with De-emphasis at -3dB when enabled.

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer

BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

SPD specific assumption:

Number of devices on the specific DIMM assumed.

Termination of command, address, and control is actual value used on the DIMM.

ECC or non-ECC as per the specific DIMM.

SPD specifies Delta T

4.1.2 Normal Mode (cont'd)

AMB power spec specific assumptions:

Dual rank x8 ECC DIMM assumed (18 DRAM devices present on DIMM)

ECC DIMM assumed (72 bit data, 14 lanes northbound).

AMB specification specifies current for each rail.

Table 6A contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 6A — Table 6 Values for x8 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Idle_0	Idle Current, single or last DIMM L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_0 Total Power			3.5		4.0		TBD		W	
Idd_Idle_1	Idle Current, first DIMM L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_1 Total Power			4.6		5.1		TBD		W	
Idd_TDP_0 (for AMB spec, Not in SPD)	Active Power, TDP BW, Single or Last DIMM L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	@1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A	1
		@1.8V	1.1	1.3	1.2	1.3	TBD	TBD	A	1
		@3.3V								A
Idd_TDP_0 Total Power			5.2		5.8		TBD		W	1
Idd_TDP_1 (for AMB spec, Not in SPD)	Active Power, TDP BW, First DIMM L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A	1
		@1.8V	0.9	1.0	0.9	1.0	TBD	TBD	A	1
		@3.3V								A
Idd_TDP_1 Total Power			5.8		6.4		TBD		W	1

Table 6A — Table 6 Values for x8 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Active_1	Active Power L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A	
		@1.8V	1.2	1.3	1.2	1.3	TBD	TBD	A	
		@3.3V							A	
Idd_Active_1 Total Power			6.4		7.1		TBD		W	
Idd_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Active_2 Total Power			5.0		5.6		TBD		W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	TBD	TBD	A	
		@1.8V		0.7		0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Training Total Power							TBD		W	
Idd_IBIST (for AMB spec, Not in SPD)	IBIST Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	TBD	TBD	A	
		@1.8V		0.7		0.7	TBD	TBD	A	
		@3.3V							A	
Idd_IBIST Total Power							TBD		W	
Idd_MemBIST (for AMB spec, Not in SPD)	MemBIST Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	TBD	TBD	A	
		@1.8V		2.1		2.1	TBD	TBD	A	
		@3.3V							A	
Idd_MemBIST Total Power							TBD		W	
Idd_EI (for AMB spec, Not in SPD)	Electrical Idle DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	TBD	TBD	A	
		@1.8V		0.2		0.2	TBD	TBD	A	
		@3.3V							A	
Idd_EI Total Power							TBD		W	

4.1.2 Normal Mode (cont'd)

Table 6B contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 6B — Table 6 Values for x4 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Idle_0	Idle Current, single or last DIMM L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_0 Total Power			3.9		4.4		TBD		W	
Idd_Idle_1	Idle Current, first DIMM L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_1 Total Power			4.9		5.5		TBD		W	
Idd_TDP_0 (for AMB spec, Not in SPD)	Active Power, TDP BW, Single or Last DIMM L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	@1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A	1
		@1.8V	1.5	1.6	1.5	1.6	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_0 Total Power			5.9		6.5		TBD		W	1
Idd_TDP_1 (for AMB spec, Not in SPD)	Active Power, TDP BW, First DIMM L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A	1
		@1.8V	1.3	1.4	1.3	1.4	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_1 Total Power			6.3		6.9		TBD		W	1
Idd_Active_1	Active Power L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A	
		@1.8V	1.6	1.7	1.6	1.7	TBD	TBD	A	
		@3.3V							A	
Idd_Active_1 Total Power			6.9		7.6		TBD		W	

Table 6B — Table 6 Values for x4 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Active_2 Total Power			5.5		6.1		TBD		W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	TBD	TBD	A	
		@1.8V		0.9		0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Training Total Power							TBD		W	
Idd_IBIST (for AMB spec, Not in SPD)	IBIST Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	TBD	TBD	A	
		@1.8V		0.9		0.9	TBD	TBD	A	
		@3.3V							A	
Idd_IBIST Total Power							TBD		W	
Idd_MemBIST (for AMB spec, Not in SPD)	MemBIST Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	TBD	TBD	A	
		@1.8V		2.4		2.4	TBD	TBD	A	
		@3.3V							A	
Idd_MemBIST Total Power							TBD		W	
Idd_EI (for AMB spec, Not in SPD)	Electrical Idle DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	TBD	TBD	A	
		@1.8V		0.2		0.2	TBD	TBD	A	
		@3.3V							A	
Idd_EI Total Power							TBD		W	

4.1.2 Normal Mode (cont'd)

Notes and Assumptions:

NOTE 1 Values highlighted in 'Red' are for reference (i.e. placeholder value)

V_{dd} : Thermal Design = 1.845V (+2.5%) ; Max Current = 1.900V (+5.5%)

V_{cc} : Thermal Design = 1.530V (+2%) ; Max Current = 1.575V (+5%)

Includes all DIMM DRAM organizations (SRx4, DRx4, SRx8, DRx8) and Raw Cards (A, B, C, D, E, H, J)

For x8, measured with DRx8 raw card B with 39 ohm termination for command, address, and clocks, and 47 ohm termination for CS and CKE

For x4, measured with DRx4 raw card E with parallel 33 ohm termination for command, address, and 39 ohm termination for CS, CKE and clocks

Note: cards using smaller termination resistors will have higher powers. e.g. x4 cards parallel 22 ohm termination for command and address could add as much as 0.4W to the power for all states.

Primary channel Drive strengths at 100% with De-emphasis at -6.5dB

Secondary channel Drive strengths at 60% with De-emphasis at -3.5dB when enabled

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

V_{ddsp} rail assumed to be insignificant (<0.1 A max @ 3.3v)

Thermal Max is for cooling and heat sink / heat spreader requirements

VR Max is for voltage regulator sizing and voltage distribution and tolerance requirements

Total Power assumes some 1.8v current is dissipated in the DIMM terminations (not in the AMB)

4.1.3 S3 current Specification

S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode. This AMB S3 current specification is required for the sizing of the power supply used for the S3 mode.

In this mode is defined as:

DRAMs in self refresh.

AMB maintaining the DRAMs in self refresh by driving the CKE signals low.

REFCLK not toggling.

VDD = VDDmax (1.9V).

VCC = 0V

VTT = 0V

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Nominal	Max Current	Nominal	Max Current	Nominal	Max Current	Units
Idd_S3	S3 current VDD = 1.9V VCC = 0V VTT = 0V Across process variations Across the operating TCASE temperature range. DIMM types: Raw Card A, B, C, D, E, H, J, and future raw card type as adopted by FB-DIMM.	VDD (1.8V)		75		75		75	mA

Note that the total DIMM current will include the AMB IDD_S3 value as well as the self refresh current of all of the DRAMs on the DIMM.

4.2 FBD Channel Interface

Refer to “High Speed Differential PTP Link at 1.5V Specification” for recommended operating conditions.

4.2.1 FBD Electrical Timing Specifications

Table 7 contains the FBD electrical timing specifications.

Table 7 — Advanced Memory Buffer FBD Timing/Electrical

Symbol	Parameter	Units	Min	Typ	Max	Notes
tEI Propagate	EI Assertion Pass-Thru Timing	nS			60	
tEID	EI Deassertion Pass-Thru Timing	clks			bit lock	
tEI	EI Assertion Duration	clks	100			1
tBitLock	Bit Lock Interval	frames			119	1
tFrameLock	Frame Lock Interval	frames			154	1

1. Defined in FBD Architecture and Protocol Spec

4.2.2 AMB Latency Parameters

Parameter	Date Rate	Min	Typ	Max	Units	Comments
tSCL Southbound Command Latency	533				ns	1, 8, 9
	667				ns	
	800				ns	
tNDL Northbound Data Latency	533				ns	2, 9
	667				ns	
	800				ns	
tCCL Core Command Latency	533				ns	3, 5
	667				ns	
	800				ns	
tCDL Core Data Latency	533				ns	4, 5
	667				ns	
	800				ns	
tRESAMPLE Resample Delay	533				ns	6
	667				ns	
	800				ns	
tRESYNC Resync Delay	533				ns	7, 8, 9
	667				ns	
	800				ns	

NOTE 1 tSCL is measured from the center of the data eye of the first bit of the command frame at the SB input to the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below.

NOTE 2 tNDL is measured from the rising edge of the latest DQS input to the AMB to the center of the data eye of the first bit of the matching data frame at the NB outputs. See diagram below.

NOTE 3 tCCL is calculated as the maximum time from an internal point where the deskewed frame aligned command is available to the core from the SB I/O (the start of the Command to Data Delay) until the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below. This maximum considers worst case operating conditions.

NOTE 4 tCDL is calculated as the maximum time from the rising edge of the latest DQS input to the time where the data is available to be sent to the NB I/O (end point of the Command to Data Delay). See diagram below. This maximum considers worst case operating conditions.

NOTE 5 tCCL and tCDL are meant to provide the DIMM vendor with the AMB portion of the Command to Data delay which is included in the SPD. The Command to Data Delay in the SPD consists of tCCL + tCMD_FLT + tDQSCK (DRAM spec) + tDQS_FLT + tCDL. The XXXX_FLT parameters are PCB flight delays. tSCL may have a programmable added delay on some DIMM configurations which must also be added in.

NOTE 6 tRESAMPLE is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resample mode, measured from the center of the data eye.

NOTE 7 tRESYNC is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resync mode, measured from the center of the data eye.

NOTE 8 Measured upon entering L0 state immediately after channel reset, before the input has drifted with respect to REFCLK.

NOTE 9 Typical numbers include the average of any clock synchronizing.