

JEDEC STANDARD

Definition of the SSTUA32S869 and SSTUA32D869 Registered Buffer with Parity for DDR2 RDIMM Applications

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DEFINITION OF THE SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-09, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUA32S869 and SSTUA32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The SSTUA32S869 and SSTUA32D869 are identical in functionality to the SSTU32S869 and SSTU32D869 devices respectively but specify tighter timing characteristics and a higher application frequency of up to 410MHz.

The purpose is to provide a standard for the SSTUA32S869 and SSTUA32D869 (see Note) logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designations SSTUA32S869 and SSTUA32D869 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 14-bit 1:2 registered buffer with parity is designed for 1.7 V .. 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers optimized to drive the DDR2 DIMM load, following the SSTL_18 standard. They provide 50% more dynamic driver strength than the standard SSTUA32866 outputs.

The SSTUA32S869 and SSTUA32D869 operate from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and un-driven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs except $\overline{PTYERR}$ are forced low. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

2 Device standard (cont'd)

2.1 Description (cont'd)

SSTUA32S869 and SSTUA32D869 must ensure that the outputs remain low as long as the data inputs are low, the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ and the input receivers are fully enabled. This will ensure that there are no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held high, DODT and DCKE must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

The parity error output $\overline{\text{PTYERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS}}$ and/or $\overline{\text{CSR}}$ are asserted low.

The device monitors both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs and will gate the Qn, PPO (Partial-Parity-Out) and $\overline{\text{PTYERR}}$ (Parity Error) Parity outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn, PPO and $\overline{\text{PTYERR}}$ outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls and will force the Qn and PPO outputs low and the $\overline{\text{PTYERR}}$ high.

The SSTUA32S869 and SSTUA32D869 include a parity checking function. The SSTUA32S869 and SSTUA32D869 accept a parity bit from the memory controller at its input pin PARIN one or two cycles after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain $\overline{\text{PTYERR}}$ pin (active low) whether a parity error has occurred. The number of cycles depends on the setting of C1/C2, see Figure 6 and 7.

When used as a single device, the C1/C2 inputs are tied low. When used in pairs, the C1/C2 inputs are tied low for the first register (front) and the C1/C2 inputs are tied high for the second register. When used as a single register, the PPO and $\overline{\text{PTYERR}}$ signals are produced two clock cycles after the corresponding data input. When used in pairs, the $\overline{\text{PTYERR}}$ signals of the first register are left floating. The PPO outputs of the first register are cascaded to the PARIN signals on the second register (back). The PPO and $\overline{\text{PTYERR}}$ signals of the second register are produced three clock cycles after the corresponding data input. Parity implementation and device wiring for single and dual die is described in Figure 1.

If an error occurs, and the $\overline{\text{PTYERR}}$ is driven low, it stays low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE, $\overline{\text{DCS}}$, $\overline{\text{CSR}}$ and DODT) are not included in the parity check computations.

All registers used on an individual DIMM must be of the same configuration, i.e single or dual die.

2 Device standard (cont'd)

2.1 Description (cont'd)

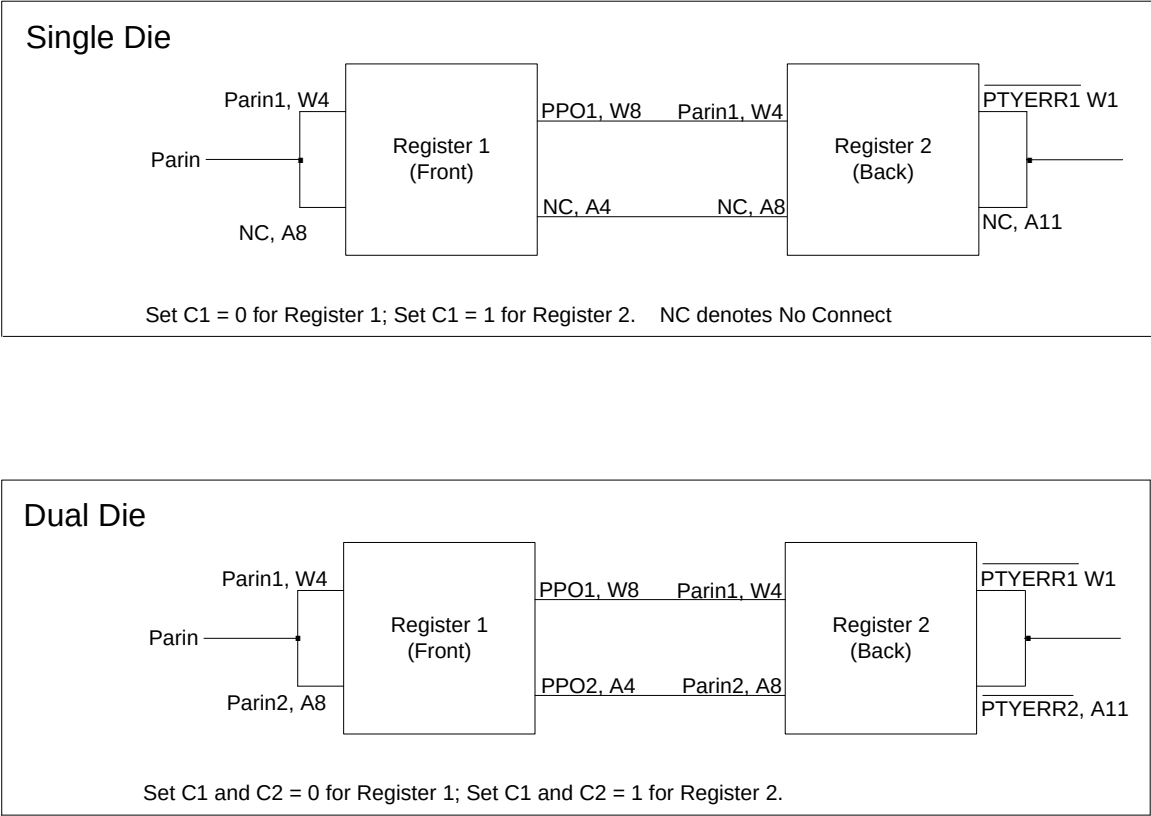


Figure 1 — Parity implementation and device wiring for SSTUA32S869 and SSTUA32D869

2 Device standard (cont'd)

2.2 150-ball TFBGA (MO-246)

Package options include 150-ball Thin Profile Fine Pitch BGA (TFBGA) (11×19 array, 8.0×13.0 mm body size, 0.65 mm pitch, 1.2mm height, MO-246, Variation TBD).

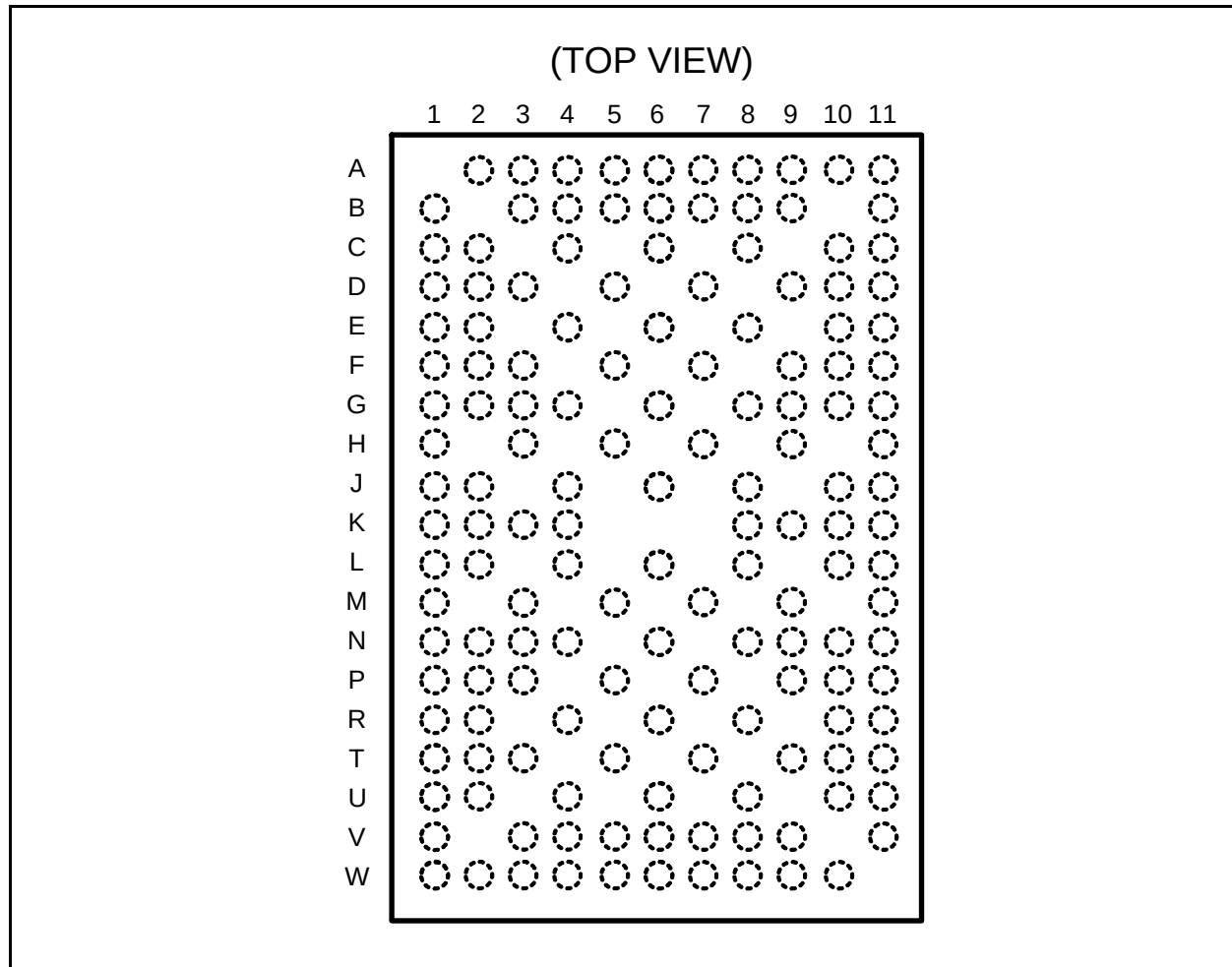


Figure 2 — Pinout configuration

2 Device standard (cont'd)

2.3 Pinout top view for 150-ball TFBGA

150-ball, 11 × 19 grid, TOP VIEW

Figure 3 specifies the pinout for SSTUA32S869 and SSTUA32D869. Unlike other configurable registers the device has symmetric pinout with center inputs and outputs to the left and right sides. Therefore the pinout for the device in front configuration is identical to pinout in back configuration. The recommended placement is back to back on both sides of the PCB. VIAs for the inner ball connections (Vdd, GND, Inputs) are to be placed at the NB locations.

	1	2	3	4	5	6	7	8	9	10	11
A	NB	VDD	MCL ⁽¹⁾	PP02 ⁽²⁾	GND	VREF	GND	PARIN2 ⁽²⁾	MCL ⁽¹⁾	VDD	PTYERR2 ⁽²⁾
B	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
C	QCKEA	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	QCKEB
D	Q2A	VDD	GND	NB	DCKE	NB	D2	NB	GND	VDD	Q2B
E	Q3A	VDD	NB	D3	NB	NC	NB	DODT	NB	C2 ⁽²⁾	Q3B
F	QODTA	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	QODTB
G	Q5A	VDD	GND	D5	NB	CLK	NB	D6	GND	VDD	Q5B
H	Q6A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q6B
J	QCSA	VDD	NB	NC	NB	RESET	NB	CSR	NB	VDD	QCSB
K	VDD	VDD	GND	GND	NB	NB	NB	GND	VDD	VDD	VDD
L	Q8A	VDD	NB	DCS	NB	CLK	NB	D8	NB	VDD	Q8B
M	Q9A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q9B
N	Q10A	VDD	GND	D9	NB	NC	NB	D10	GND	VDD	Q10B
P	Q11A	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	Q11B
R	Q12A	C1	NB	D11	NB	NC	NB	D12	NB	VDD	Q12B
T	Q13A	VDD	GND	NB	D13	NB	D14	NB	GND	VDD	Q13B
U	Q14A	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	Q14B
V	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
W	PTYERR1	VDD	MCL ⁽¹⁾	PARIN1	GND	VREF	GND	PPO1	MCL ⁽¹⁾	VDD	NB

NB indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die).

Figure 3 — Pinout top view for 150-ball TFBGA

NOTE 1 MCL denotes input pin that must be connected Low. Register Vendors: Implement NC or input on Ball A3, A9, W3, W9

NOTE 2 NC for single die version

2 Device standard (cont'd)

2.4 Terminal functions

Table 1 — Terminal functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE, DODT	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D1 ... D14 ⁽¹⁾	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{DCS}$, $\overline{CSR}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present.
Re-driven outputs	Q1A...Q14A, Q1B ... Q14B, $\overline{QCSA}$, $\overline{QCSB}$ QCKEA, QCKEB QODTA, QODTB	1.8 V CMOS	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN1, PARIN2 ⁽²⁾	SSTL_18	Input parity is received on pin PARIN and should maintain parity across the D1...D14 ⁽¹⁾ inputs, at the rising edge of the clock, one clock cycle after Chip Select is LOW.
Parity output	PPO1, PPO2 ⁽²⁾	SSTL_18	Partial Parity Output. Indicates parity out of D1-D14 ⁽¹⁾
Parity error output	$\overline{PTYERR1}$, $\overline{PTYERR2}$ ⁽²⁾	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by in total 2 clock cycles for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition).
Configuration Inputs	C1, C2	1.8V LVCMOS	When Low, register is configured as Register 1. When High, register is configured as Register 2.
Clock inputs	CK, $\overline{CK}$	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	$\overline{RESET}$	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.
	VDD	Power Input	Power supply voltage
	GND	Ground Input	Ground

NOTE 1 Inputs D1, D4 and D7 and their corresponding outputs Qn are not included in this range.

NOTE 2 NC for single die version.