

JEDEC STANDARD

Definition of the SSTUB32865 28-bit 1:2 Registered Buffer with Parity for DDR2 RDIMM Applications

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DEFINITION OF THE SSTUB32865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-14, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. The SSTUB32865 is identical in functionality to the SSTU32865 but specifies tighter timing characteristics and a higher application frequency of up to 410 MHz.

The purpose is to provide a standard for the SSTUB32865 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32865 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 28-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVC MOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTUB32865 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and un-driven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs except $\overline{PTYERR}$ are forced low. The LVC MOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

2.1 Description (cont'd)

As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the SSTUB32865 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ must be held high, DODT0 and DODT1, DCKE0, and DCKE1 must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

The device monitors both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are high. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and will force the Qn outputs low and the $\overline{\text{PTYERR}}$ output high. If the DCS-control functionality is not desired, then the CSGateEN input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The SSTUB32865 includes a parity checking function. The SSTUB32865 accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs (with either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ active) and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active LOW). If an error occurs and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{PTYERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power mode (LPM) and the $\overline{\text{PTYERR}}$ output is driven low, then it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

The parity error output $\overline{\text{PTYERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS0}}$ and/or $\overline{\text{DCS1}}$ are asserted low. CSGateEN does not affect $\overline{\text{PTYERR}}$ operation.

2.2 160-ball TFBGA (MO-246A)

Package options include 160-ball Thin Profile Fine Pitch BGA (TFBGA) (12×18 array, 9.0×13.0 mm body size, 0.65 mm pitch, MO-246, Issue A).

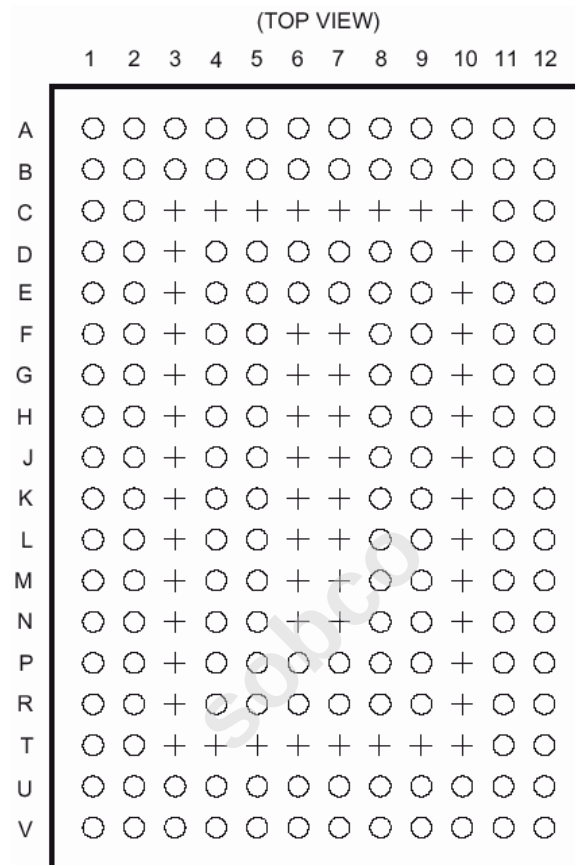


Figure 1 — Pinout Configuration

2.3 Pinout Top View for 160-ball TFBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGate EN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	$\overline{\text{DCS0}}$		GND	GND			VDDR	VDDR		$\overline{\text{QCS0B}}$	$\overline{\text{QCS0A}}$
K	$\overline{\text{CK}}$	$\overline{\text{DCS1}}$		VDDL	VDDL			GND	GND		$\overline{\text{QCS1B}}$	$\overline{\text{QCS1A}}$
L	$\overline{\text{RESET}}$	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL	$\overline{\text{PTYERR}}$	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

An empty cell indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die). MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

Figure 2 — Pinout Top View for 160-ball TFBGA (12 × 18 Grid)

2.4 Terminal Functions

Table 1 — Terminal Functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D0 ... D21	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{DCS0}$, $\overline{DCS1}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes and parity checking, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-driven outputs	Q0A...Q21A, Q0B ... Q21B, $\overline{QCS0}$ -1A,B, QCKE0-1A,B, QODT0-1A,B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN	SSTL_18	Parity input for the D0 ... D21 inputs; arrives one clock cycle after the corresponding data input.
Parity error output	$\overline{PTYERR}$	Open drain	When LOW, this output indicates that a parity error was identified associated with a valid address and/or command input. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program inputs	CSGateEN	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D21 inputs will be latched and re-driven on every rising edge of the clock.
Clock inputs	CK, $\overline{CK}$	SSTL_18	Differential system clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	MCL, MCH		Must be connected to a logic LOW or HIGH.
	$\overline{RESET}$	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.