

JEDEC STANDARD

Definition of the SSTUB32868 Registered Buffer with Parity for 2R x4 DDR2 RDIMM Applications

JESD82-26.01

(Editorial Revision of JESD82-26, May 2007)

JANUARY 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2Rx4 DDR2 RDIMM APPLICATIONS

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DEFINITION OF THE SSTUB32868 1.8-V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-17, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTUB32868 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32868 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 28-bit 1:2 configurable registered buffer is designed for 1.7 V to 1.9 V V_{DD} operation.

All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{\text{RESET}}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for un-terminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{\text{QERR}}$) output.

The SSTUB32868 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and un-driven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and C inputs always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

2.1 Description (cont'd)

As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUB32868 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ must be held high, DODT0 and DODT1 , DCKE0 , and DCKE1 must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

The SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding $\overline{\text{QERR}}$ output signal for the data inputs is generated two clock cycles after the data, to which the $\overline{\text{QERR}}$ signal applies, is registered.

The SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when $C = 0$; or D1-D12, D17-D20, D22, D24-D28 when $C = 1$) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power (LPM) and the $\overline{\text{QERR}}$ output is driven low, then it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0 , DCKE1 , DODT0 , DODT1 , $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

The parity error output $\overline{\text{QERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS0}}$ and/or $\overline{\text{DCS1}}$ are asserted low. CSGEN does not affect $\overline{\text{QERR}}$ operation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hard-wired to a valid low or high level to configure the register in the desired mode.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN , $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high. If CSGEN , $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. Also, if both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs are high, the device will gate the $\overline{\text{QERR}}$ output from changing states. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ is low, the $\overline{\text{QERR}}$ output will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and when driven low will force the Qn outputs low, and the $\overline{\text{QERR}}$ output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ only, then the CSGEN input should be pulled up to V_{DD} through a pull-up resistor.

The two V_{REF} pins (A1 and V1) are connected together internally by approximately 150 Ω . However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

2.2 176-ball TFBGA (MO-246)

Package options include 176-ball TFBGA (MO-246 version B).

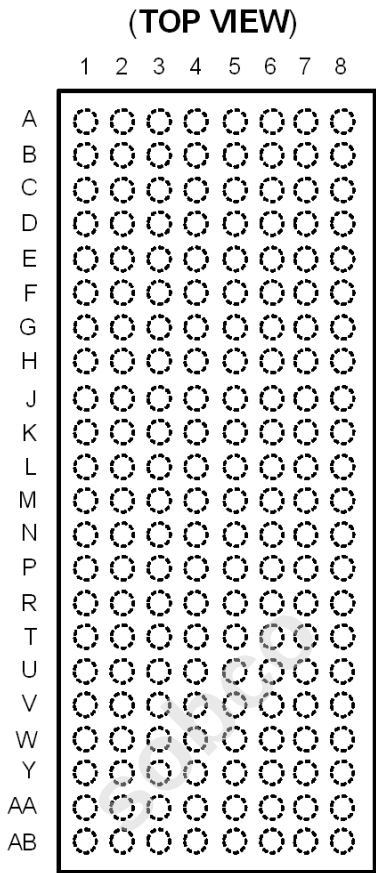


Figure 1 — Pinout Configuration

NOTE 1 8 x 22 array, 6.0 x 15.0 mm body size, 0.65 mm pitch. Diagram is for reference only. See MO-246 for detailed package specification.