

JEDEC STANDARD

Fully Buffered DIMM Design for Test, Design for Validation (DFx)

JESD82-28A.01

(Editorial revision of JESD82-28A, July 2008)

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Fully Buffered DIMM Design for Test, Design for Validation (DFx)

From JEDEC Board ballot, JCB-06-68 and JCB-08-30, formulated under the cognizance of the JC-40.4 Subcommittee for Digital Logic Liaison and the JC-40.5 Subcommittee on Logic Verification and Validation.

1 Scope

This FBDIMM DFx standard covers Design for Test, Design for Manufacturing, and Design for Validation (“DFx”) requirements and implementation guidelines for Fully Buffered DIMM technology.

2 Related Documents

Table 2-1 — Related Documents

Document	Revision	Description
FBDIMM Architecture and Protocol Specification	1.0	FBDIMM architecture and interface protocol
FBDIMM Connector Specification	1.0	Connector physical parameters: pinout, footprint, mechanical drawing, and requirements
FBDIMM Signaling Specification	1.0	PTP link parameters: signaling, I/O, and AC and DC parameters
FBDIMM AMB Specification	1.0	AMB Characteristics: pinout, package type, mechanical outline, footprint, AC/DC specs, power/thermal requirements, buffer TPT, special feature requirements (e.g., thermal sensor), & basics DFT
FBDIMM DIMM Specification	1.0	DIMM module parameters: multiple raw card designs, block diagrams, net topologies, routing details, timing budget, pin out, mech. Outline, stack up, and SPD requirements
SMBus	2.0	System Management Bus Specification http://smbus.org/specs/smbus20.pdf
DDR2 JEDEC Spec		JEDEC DDR 2 SDRAM Data Sheet JC-42.3

3 Terms, Definitions, and Abbreviations

This standard uses the following terms, definitions, and abbreviations:

NOTE The terms chipset and memory controller are used interchangeably throughout the rest of this document. The term motherboard is used as a generic term to describe the PCB onto which the memory controller is mounted. Actual implementations could have distributed memory controllers mounted on separate memory boards.

3 Terms, Definitions, and Abbreviations (cont'd)

Table 3-1 — Terms, Definitions, and Abbreviations

TERM	Definition
AMB	Advanced Memory Buffer
ATE	Automatic Test Equipment
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device.
Bit Lane	A differential pair of signals in one direction.
D+ and D-	The D+ and D- terms used in this document are used to indicate the two conductors or signals of a differential signaling pair.
DDR	Double Data Rate (SDRAM)
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an addr/ control channel
DFx	Design-for-(test, validation, debug etc.). The collection of design features for silicon test, validation and other uses.
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR Channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM “stacked” one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code.
EMI	Electro-magnetic interference
FBDIMM	Fully Buffered DIMM
Frame	Group of bits containing commands or data
HMI	Host-memory interface. The connection between a host controller and memory.
Host	Memory controller agent on an FBDIMM channel
ISI	Inter Symbol Interference
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)

3 Terms, Definitions, and Abbreviations (cont'd)

Table 3-1 — Terms, Definitions, and Abbreviations (cont'd)

JESD79	JEDEC Standard 79, DDR SDRAM Specification
Link	A dual-simplex communications path between two components. The collection of two Ports and their interconnecting bit lanes.
NB	Northbound
Northbound	The direction of signals running from the farthest DIMM toward the host.
PCB	Printed circuit board
PLL	Phase Locked Loop
Port	In physical terms, a group of transmitters and receivers physically located on the same chip that define one end of a Link.
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g., a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module.
Resample	A resampler repeater is a serial data in and serial data out node that attenuates jitter by re-generating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the re-transmitted data.
Resync	A resync repeater is a serial data in and serial data out node that re-synchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes. Both the jitter and voltage budgets for the re-transmitted data are reset.
SB	Southbound
SDRAM	Synchronous Dynamic Random Access Memory
SI	Signal Integrity
Serial Presence Detect	An EEPROM device on the DIMM, used to store DIMM and DRAM parameters
SMBus	System Management Bus. Controlled by a system management controller to read and write configuration registers. Limited to 100 KHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSTL_18	Series Stub Terminated Logic for 1.8 V
Unit Interval	Average time interval between voltage transitions of a signal

3 Terms, Definitions, and Abbreviations (cont'd)

Table 3-1 — Terms, Definitions, and Abbreviations (cont'd)

Vss	Ground (0V)
Vddq	I/O buffer voltage for DDR-II buffers. Nominally 1.8 V

4 Test and Validation Overview

4.1 FBDIMM Overview

The Fully Buffered DIMM (FBDIMM) interface is a high speed (2.4 to 4.8 GT/s) narrow (67 pin) interface. The DFT strategy for FBDIMM has several objectives: first, because the memories on an FBDIMM can only be accessed via the AMB, DFT features in the AMB are required to allow economical testing of the memories. Second, DFT functions in the AMB can automate some test functions that can reduce the cost and improve the quality of DIMM testing. Third, DFT functions can facilitate system level debug operations such as memory channel integrity verification that will be useful to OEMs and end users of systems employing FBDIMM technology.

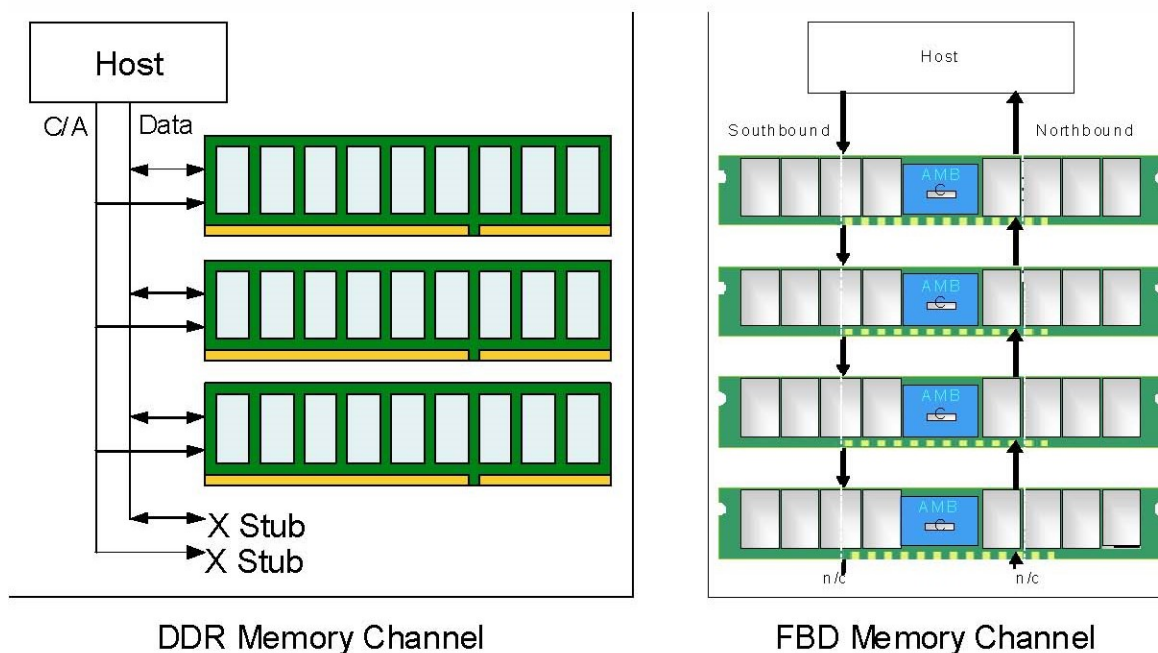


Figure 4-1 — Memory Channel Architecture

Traditional memory solutions are based on stub bus architecture with up to 4 DIMMs per memory channel. Normally the maximum speed of the bus is determined by the number of DIMMs on the bus. The FBD architecture connects DIMMs together in a daisy chain fashion using a high speed point to signaling scheme.

4.1 FBDIMM Overview (cont'd)

Each DIMM has a buffer (Advanced Memory Buffer or 'AMB') that decodes/encodes data for local DRAMs and re-drives high speed data to the next DIMM in the chain. The signaling speed on an FBD channel therefore does not change as more DMMS are added, although latency would increase. Note that there is no direct access to the DRAMs after DIMM assembly. Furthermore the native high speed interface is beyond the capability of conventional production testers. This makes DFT support on the AMB essential for the cost efficient production testing of FBDIMMs.

4.2 FBDIMM DfX Objectives

The desired outcomes of the DFT/DfX strategy are:

- FBDIMM must be testable using conventional equipment and methods
- DFT will allow enhanced testing over traditional methods at component, DIMM and system level
- DFT will be compatible with tools and methods developed for other interfaces Evaluation of these objectives led to the several key test modes:
- Memory BIST to be used during buffer, DIMM test and system test
- Transparent mode, which allows access to the DRAMs behind the buffer
- IBIST – used for interconnect testing at DIMM and system level
- LAI mode – allows the AMB to act as an intelligent front end for a logic analyzer

4.3 DIMM Test Process

DRAMs are tested at the manufacturer using standard test processes: sort, package test, burn in, and class test. There are variations in the use of parallel test and test time. DRAMs tend to have very long test times but due to the moderate pin count, many DRAMs (typically 64 or 128) are tested in parallel.

For DIMM test many suppliers use a 2 pass test. The first pass uses ATE or low cost leakage and continuity tester to verify connectivity, shorts and DRAM leakage. This step is also used to program the SPD device with appropriate parameters. The second step uses ATE or a motherboard-based tester. Test time on ATE varies depending on manufacturer or customer requirements. On the motherboard-based tester test times are typically one to three minutes, consisting of a simple boot test and memory stress tests. In some cases, suppliers use gravity-fed handlers to automate insertion of the DIMM. Motherboard system manufacturing uses a similar test strategy with memory test times of approximately 60 seconds.

For suppliers that rely on ATE, it is possible to test the DIMM in one insertion. One advantage of ATE is the DIMM can be tested with controlled timings, voltages and algorithmic patterns. If the DRAM topology is known the tester can apply topologically correct patterns, re-creating the conditions present during DRAM manufacturing.

The reason suppliers use stress tests is that DRAMs are sensitive to the surrounding electrical environment. This environment is different than that presented at DRAM component test, resulting in some level of fallout due to differences in loading, noise, or power delivery. Existing memory buffers (used on registered DIMMs) provide partial isolation, reducing electrical loading.

4.3 DIMM Test Process (cont'd)

Registered DIMMs have an added cycle of latency but the DRAM is otherwise accessible from the edge fingers of the DIMM. With FBDIMM the DRAM is completely isolated behind a high speed interface and a memory buffer. This reduces the load on the DRAMs but has the disadvantage of loss of direct access to the DRAMs from the DIMM connector. This isolation presents new challenges for failure analysis or application of specific DRAM tests.

Although it is possible to model much of the environment, it will take time and product volume to determine the impact on DIMM manufacturability and quality. Furthermore, it will take time to develop new manufacturing techniques while maintaining product quality. This places us in a position of needing to support traditional test methods while paving the way for improvements. For this reason there may be extra DFT features to facilitate learning and test process improvement.

FBDIMM supports ATE, motherboard-based testing or testing with dedicated fixtures. In a system setting the test process need not change significantly from the traditional process. System behavior will propagate to the DRAMs in much the same way it does with conventional DIMMs. For higher throughput and reduced test cost AMB DFT features may be used to deliver known patterns to the DRAMs. Several DIMMs can be tested in parallel using this method.

4.4 Memory Manufacturing Flow

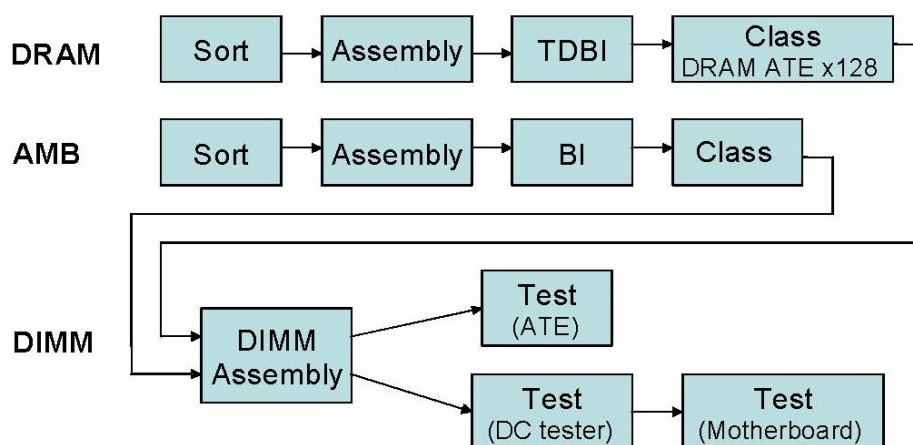


Figure 4-2 — Memory Assembly and Test Procedure

4.5 Reducing Test Cost

Most of the DFT features are aimed at improving testability and test coverage. However there is another benefit to be gained. Consider use of Memory BIST and IBIST at system power on. Rather than executing a traditional power on self test, an FBDIMM enabled system can run IBIST to verify the integrity of the installed DIMMs. This would include the DIMMs, connectors and other hardware along the path. The system can also use memory BIST to test and zero all DIMMs at the same time rather than one by one as in today's systems. This will save considerable startup time on systems with dozens of DIMMs.

The same principle can be applied to DIMM test. Memory manufacturers tend to use motherboards or other low cost testers to test DIMMs after assembly. With FBDIMM it is easy to construct a system capable of testing four, 8, 16, or more DIMMs in parallel.

4.6 Test Strategy

It is desirable to define a set of features that allow testing of the buffer, DIMM and system with little or no new capital equipment. In many cases FBDIMM features can be tested on older equipment through the use of DFT. The supplier of the AMB or DIMM will determine the equipment to be used but there are some useful guidelines.

A typical test strategy is illustrated in Table 4-1. Rows in the table represent key tests at various stages of integration (AMB, DIMM, system). The table columns show which DFX features would be used at each test step. During AMB test the functions of the buffer and the DFX features should be tested. Several of the DFX features can help with testing interfaces that exceed tester capability.

Table 4-1 — Test Overview

AMB test	ATE	Transp Mode	Mem BIST	IBIST	LAI Mode	Vendor Specific
(1st insertion, 100-200 MHz tester, FBDIMM looped back, DDR connected to tester)						
High speed IO test				✓		
Test AMB core function and defects	✓					
DDR functional test at speed	✓					
Verify thermal sensor	✓					
Test DFX features	✓	✓	✓			
(2nd insertion or relay on load board, all pins connected to tester)						
High speed IO leakage	✓					
Additional AMB functional or structural test	✓					✓
Test transparent mode	✓					
DIMM Test						
(1st insertion, all pins connected to tester)						
Assembly defects (opens, shorts)	✓					
High speed IO leakage	✓					
DRAM array test (ATE only)	✓	✓				
Program SPD	✓					
(2nd insertion or relay on load board, IO looped back)						
High speed IO functional test	✓					
DDR functional test at speed	✓					
System Test						
DIMM initialization, DRAM function	✓					
FBDIMM link test				✓		
System Validation						
Analog Inspection	✓	✓	✓			
Link observability			✓			
Protocol verification					✓	

4.7 AMB Test

Most of the AMB features can be tested with the DDR pins connected to a tester and the FBDIMM pins configured for loop back testing.

There are two ways to loop FBDIMM outputs to inputs. The simplest method is to loop the ten southbound transmitters back to the receivers and the northbound Tx to Rx. The disadvantage of this method is that it may not allow testing of the re-time path in the IO.

To cover the re-time path, connect 10 SB lanes to 10 NB lanes, test the interface and then connect and test the remaining NB lanes. This results in a figure-8 type of loop back. The four remaining NB lanes may be connected using internal loop back if the design supports this. Otherwise external RF relays may be used to switch in the remaining lanes.

4.7.1 AMB Functionality and Defects

Many of the DfX features can help with AMB self-test. AMB suppliers may implement specific functional or structural tests. The exact nature of these tests will vary depending on the internal buffer implementation and manufacturing test strategy. For the purpose of this document the primary focus is testing of the external interfaces and externally-visible functionality.

Testing at this step would include all of the core logic of the buffer, digital sections in the IO area, thermal sensor and other circuits. In some cases FBDIMM pins may need to be connected to the tester.

4.7.2 DDR Functionality and Timing

DDR pins may be tested with low speed equipment by using the MemBIST engine to read or write DDR traffic at full speed. If patterns are constructed to read multiple bits from the tester, MemBIST may be used to over-sample tester data. For example, if MemBIST is programmed to expect "11110000" at 400 MTS, apply a "10" sequence from a tester at 200 MTS. This is usually possible even on 100 MHz testers with pin multiplexing. For DDR writes, MemBIST will drive data at full speed. This data can be sampled by a tester using multi-pass testing. Using a combination of these modes functionality and timing of MemBIST engine and the DDR interface may be verified.

In the example below, the tester is driving a "01" at 200 MHz while the AMB is programmed to expect four zeros followed by four ones at 800 MHz. This example uses a combination of user-defined data and circular shifting for the expected data pattern. Tester data needs to be delayed by varying amounts depending on the DQ line. For example DQ0 will drive 0 starting at 0ns while DQ1, DQ2, and DQ3 will drive the same data delayed by 1.25 ns, 2.5 ns, or 3.75 ns respectively. DQS timing would be offset in the middle of the DRAM cycle at 625 ps. One difficulty is DQS will need to toggle at 400 MHz. This may require a combination of pin multiplexing and surround by compliment formatting. This should be straightforward on a 200 MHz tester but will require creative timing on a 100 MHz tester. The problem of creating 400 MHz DQS for FBDIMM should follow established solutions for DDR2-800 DRAMs or unbuffered DIMMs.

4.7.2 DDR Functionality and Timing (cont'd)

Tester Cycle	DQ Cycle	DQ pin							
		7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	0
0	1	0	0	1	1	1	1	0	0
0	2	0	1	1	1	1	0	0	0
0	3	1	1	1	1	0	0	0	0
1	4	1	1	1	0	0	0	0	1
1	5	1	1	0	0	0	0	1	1
1	6	1	0	0	0	0	1	1	1
1	7	0	0	0	0	1	1	1	1
2	8	0	0	0	1	1	1	1	0

Figure 4-3 — 200 MHz Tester Driving 800 MHz DQ

4.7.3 FBDIMM Functionality and Timing

The FBDIMM interface can be tested with IBIST. IBIST provides a programmable pattern generator and checker for each FBDIMM path (one for north and one for south). This capability allows generation of streams of traffic at the normal data rate of the channel. The tester will need to provide a reference clock of 100 MHz to 200 MHz. IBIST registers can be programmed from the SMBus, which will be connected to the tester.

The AMB supplier may choose to implement additional capability to stress the FBDIMM interface. These methods will vary somewhat depending on the specific IO buffer design. Note that all AMBs will support reduced drive strength on FBDIMM links. This reduced drive (60% drive strength) will create smaller than normal swing allowing verification of voltage margin. Design capability signal quality can be verified during AMB characterization using high speed lab equipment.

4.7.4 Connection of FBDIMM Pins to the Tester

Several features of the AMB require connection to the tester. For these situations there are three possible approaches:

- Two insertion testing: In one insertion the FBDIMM pins are looped back as described above. For the second insertion the pins would be connected to the tester. This is a straightforward test method but undesirable as it involves two test steps, two passes through the tester and handler, additional material tracking and so forth.
- RF relays: RF relays may be used to allow connection of pins to the tester for part of the test program and loop back for the other. There are manufacturers that specialize in relays of this type.
- Two socket testing: This is similar to two insertion testing but there is a looped back socket and a direct connect socket on the same load board. Automatic handling equipment can be used to move the AMB from one socket to the other, completing the AMB test in one step. Depending on tester and handler capability one might test two buffers, switching the positions of the devices mid-test.

4.7.5 FBDIMM and DDR DC Tests

Assuming the FBDIMM and DDR pins are connected to the tester, one may perform DC testing in the usual manner with tester pin electronics. The test limits to be used are described in the AMB component specification.

The DFX IO chapter describes more sophisticated IO test methods using self test circuitry. These methods allow IO testing without connection to the tester.

4.7.6 Testing DRAM Access Features

Transparent mode assumes connection to the tester for proper operation. This will require a second test insertion or relays as described above. Since transparent mode is only used at DDR2-400 timings the tester will supply a 100 MHz reference clock. In this mode each leg of the FBDIMM differential inputs will supply data to the AMB. This data will be presented to the DDR interface but delayed by one clock. Transparent mode pin mapping and timing are described later in this standard.

If the AMB supplier has implemented structural test methods (e.g. logic scan chains) these may be used in place of some or all of the functional tests described above.

4.8 DIMM Test

A key objective of DIMM testing is to verify proper assembly and connectivity of the components on the DIMM.

4.8.1 Assembly Defects

Assembly-related opens or shorts on the DDR interface may be detected with a memory BIST pattern. Unlike older DIMM technology the FB DIMM uses ball-grid packages. This complicates opens and shorts testing since there may be several neighboring pins or traces corresponding to each ball location. One of the capabilities provided in the MemBIST engine is the ability to rotate data through the 72-bit DQ bus. This can be used during opens and shorts testing by walking a one through a field of zeros and vice versa. MemBIST can also increment addresses in the X, Y or XY direction. Combining these capabilities, fairly compact patterns may be constructed that test all possible address and data lines. The command lines will toggle as a by-product of the test, allowing us to verify these as well.

4.8.2 Leakage Testing

The FBDIMM pins may be tested at DIMM level as described above for AMB testing. If the pins are connected to the tester as with transparent mode the pins may be tested directly. If the pins are not connected to the tester they can be tested using the IO techniques described later in this standard.

4.8.3 DRAM Array Test

In many cases the exact topology or sensitivities of a DRAM are not known. In these situations it is probably best to use random data or other MemBIST or system-generated patterns to verify the DRAM on DIMM.

If the DRAM topology is known, or there are other DRAM specific tests, transparent mode can be used to gain direct access to the DRAMs behind the AMB. Transparent mode is designed to operate at 200 MHz, which is the maximum speed within the DRAM array. By varying timing of address and data arrival it is possible to test the array and its associated timings such as T_{cl} or T_{rcd}.

4.8.4 Programming the SPD

The SPD device may be programmed at any time during the DIMM test flow using the same methods as any other DIMM.

4.8.5 FBDIMM IO Test

As with the AMB component the DIMM FBDIMM pins may be looped back and tested with the interconnect BIST engine. The IBIST engine allows definition of the type of pattern(s) desired and the length of time to run the pattern(s). The selection of patterns may vary somewhat from the standalone AMB due to DIMM routing. In most cases, targeted patterns should be created that have lone pulses, neighboring traces in opposite states and so forth to detect signaling anomalies.

4.8.6 DDR Interface Testing

The DRAM on DIMM may be tested at full speed using the MemBIST engine. As described later in this document, the engine is can read, write or run a few industry-standard algorithms with various data patterns and addressing schemes. The ability provided should be adequate for testing the interfaces and internal multiplexers, decoders and related logic inside the DRAM.

4.9 System Test

At system level the AMB provides the ability to test and initialize memory as well as testing the FBDIMM links from host to DIMM and DIMM to DIMM.

Memory initialization may be accomplished with the MemBIST engine using one of the built-in or a user defined pattern. The MemBIST engine can initialize ECC bits to the correct value for shorter ECC codes. If the system uses a more complex ECC code it may be necessary to initialize some or all memory in the usual manner through the host controller.

AMB and DRAM functionality may be verified at system boot time with the MemBIST engine. It is noteworthy this process can be executed much faster than with conventional methods. Multiple DIMMs may be tested at the same time, reducing test time considerably. Since the MemBIST engine can generate data at the full DRAM rate, the test will consume considerable power, taxing both DRAM/DIMM cooling and the system power supplies. The number of DIMMs that can be safely tested and the duration of test will vary depending on system design.

The FBDIMM links can be tested in much the same way as AMB and DIMM. However, testing will be from one link agent to another (between two AMBs for example). The selection of patterns should be tailored to the topology of the memory channel in the system.

4.10 Validation

Link observability is supported in some AMB implementations with logic analyzer mode. In this mode the AMB will de-serialize FBDIMM traffic (both north and southbound) and present the data on the DDR pins. This data stream will be one sixth of the link rate, or 800MTS for a full speed 4800 MTS link. The LAI interface is designed to be usable on a logic analyzer or similar equipment. It is expected that equipment suppliers will provide LA probes and related instrumentation to be used with this mode.

The electrical behavior of the FBDIMM interface can be tested by programming appropriate test sequences into the IBIST engine, letting the engine run in continuous mode and, using probes and an oscilloscope, verifying that the interface meets the voltage and timing specifications. This testing may be performed at any level of integration from standalone AMB to complete systems.

5 Requirement Summary

5.1 DFx Requirements

FBDIMM DFT, DFV and related features are intended to facilitate testing, validation and coverage of defects. The key requirements are:

- DRAM access: The AMB must allow testing of DRAM behind the buffer by direct access, BIST or a combination of the two.
- Determinism: Operation must be deterministic in all modes.
- Tester connectivity: FBDIMM interfaces must allow connection to low speed (100-200 MHz) testers.
- Control and Observation: All DFx features must be controllable either in-band (as applicable) or SMBus. The AMB will provide features to allow observation of internal registers, link behavior and DRAM response. There must be debug hooks in the AMB and host interface to support validation/debug of FBDIMM components and the systems employing them.

5.2 Required Features

DFT features that relate to normal functionality or test modes for manufacturing must be included in all AMBs and must function as described in this specification. DFT features that support debug or evaluation are strongly recommended but are not required. It is permissible to implement additional, AMB specific innovations. AMB-specific features will not be considered part of the FBDIMM DFx specification. The specific breakdown of required features is listed in Table 5-1.

5.2 Required Features (cont'd)

Table 5-1 — Required DFT Features

Feature	Description	Required?	Anticipated Use		
			AMB	DIMM	System
Transparent Mode	Allows access to DRAM, can be used for DRAM core test; requires ATE or equivalent stimulus/response	Required	Yes	Yes	No
Memory BIST	Test DDR interface and DRAM functionality	Required	Yes	Yes	Yes
Interconnect BIST	Tests high speed link integrity; used during initialization	Required	Yes	Yes	Yes
DDR Leakage	Indirect DC leakage test of DDR interface	Required	No	Yes	Yes
Error Injection	Allows injection of errors to test controller/BIOS response	Required	Yes	No	Yes
Logic Analyzer Mode	De-serializes high speed link for analyzer or capture; needed for LAI or similar capture tools	Recommended	Yes	No	Yes
Voltage Margin	Transmitter drive strength settings to stress FBDIMM link	Required	No	No	Yes
Timing Margin	Receiver timing control allow intentional offset of data eye	Recommended	No	No	Yes

5.3 DFx Features and Usage

The FBDIMM DFx features are summarized in Table 5-2. As indicated by type, the DFx features support a variety of requirements: ATE test, burn in, IO interfaces and margin testing. The major DFx features include:

- MemBIST for memory initialization at system power on and testing the DRAM behind the buffer
- Interconnect BIST, which allows testing of the high speed interconnects at system level
- LAI mode, which de-serializes link traffic and presents in a form usable by a logic analyzer for link and protocol debug
- Transparent mode which allows a tester to connect to the high speed pins and send data to/from the DRAMs behind the buffer

5.4 AMB Overview

The major DFT blocks are the MemBIST engine and IBIST block. All DFT modes and registers are accessible from the SMBus controller.

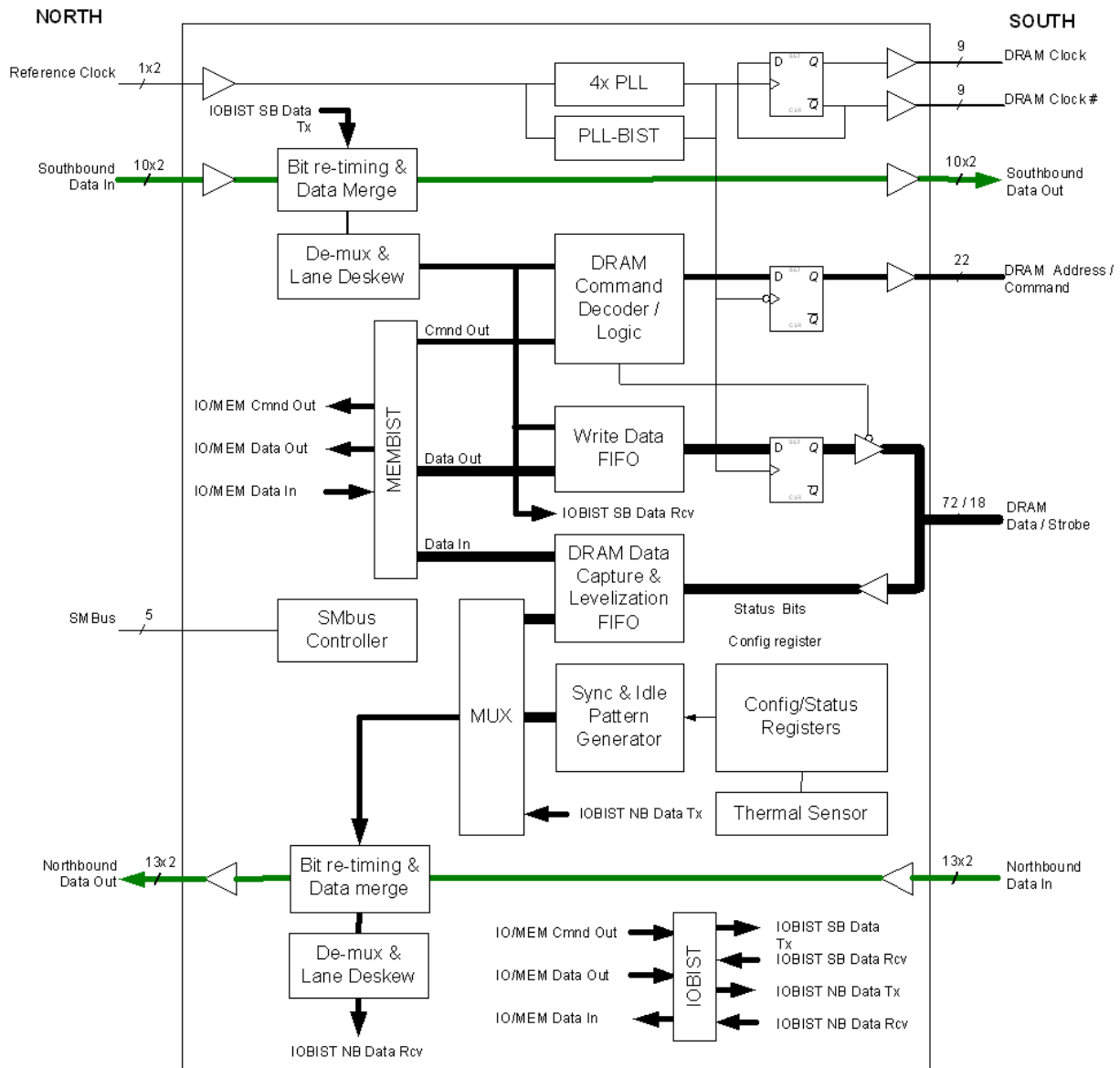


Figure 5-1 — AMB Architecture and DFT Blocks

5.4.1 Memory BIST

The DIMM has two primary failure mechanisms: assembly related defects and unexpected electrical behavior. Assuming DRAMs have been tested prior to assembly, there is less need to look for cell failures, although the need will arise from time to time to support re-screening of DRAMs for issues discovered after DIMM assembly. In most cases simple patterns can verify proper connectivity between the buffer and DRAM. If there are connectivity or gross DRAM component failure the BIST engine will be used to identify the specific failing net or DRAM to be replaced.

5.4.1 Memory BIST (cont'd)

To stress electrical behavior or to facilitate failure analysis there is a need to generate patterns to isolate electrical failures or interactions. Some of this analysis will be completed in systems and some will be conducted on testers, creating a need to accommodate both methods.

5.4.2 Interconnect BIST

As illustrated in Figure 5-2 there are two pattern generators and comparators: one for southbound data and one for northbound data. The pattern generator is used to create fixed patterns during link initialization or programmable patterns for IO buffer testing.

For buffer component test, the north and southbound drivers and receivers may be connected as shown. This will allow testing of the IOs with various test patterns or other conditions. There are two methods for loopback. The simplest is to connect the southbound outputs to southbound inputs and north to north. The advantage of this approach is the lane widths are balanced. The disadvantage is it may be possible to test only the resync path through the AMB. With the second approach we gain the ability to test the re-sample path, with some added complexity due to the imbalanced lane widths. In this mode the tester will have to drive 10 pins in one pass and the remaining 4 in a second pass. This may be accomplished with two insertions or with RF relays on the tester load board.

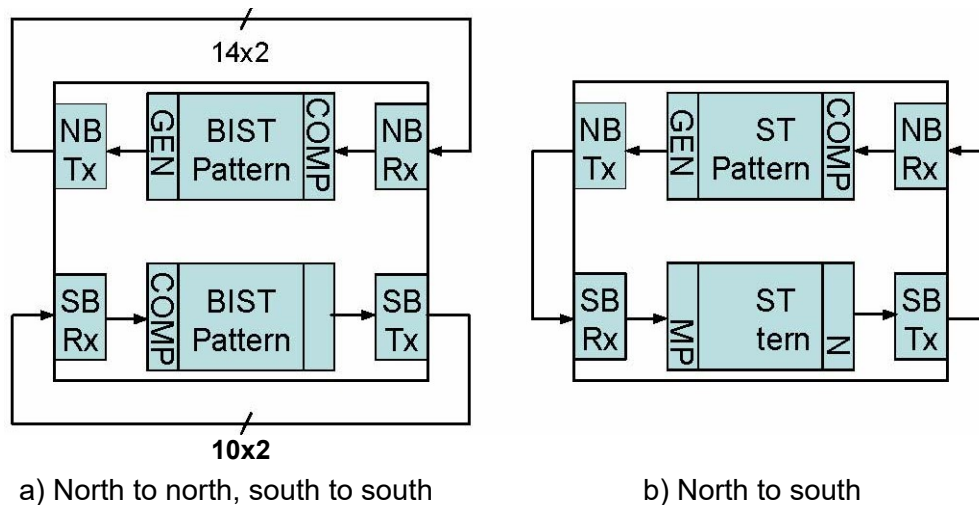


Figure 5-2 — AMB IO Loopback Methods

5.5 DDR Interface Tester Compatibility

The AMB interfaces with the DRAM memory through the DDR interface which runs at a data rate of 800 MT/s. With testers capable of only supporting a max data transfer rate of 100 to 200 MT/s, there exists the issue of having to exercise the core behind DDR I/O at speed functionally while running the I/O's themselves slower.

One solution is to apply the same data for more than one DDR clock, reducing the input data rate to 200 MT/s. For example, one might apply "01" at 200 MHz, which would be interpreted as "00001111" at DDR2-800 speeds. In this mode MemBIST can generate full speed address and data. The DDR outputs can be sampled with 2-pass testing in this mode to verify AMB operation. Transparent mode should be used to verify proper operation of the DRAM core.

5.5 DDR Interface Tester Compatibility (cont'd)

Supplier-specific DFT may be added to the DDR interface to facilitate testing on specific equipment. There are several possible approaches depending on supplier preference and equipment capability. It is not expected suppliers will use full speed testers in production as this would contribute significantly to the overall cost of the AMB.

5.5.1 Logic Analyzer Interface

In addition to the full complement of DFT features, the buffer will support validation and debug by having a mode to act as a transparent repeater which captures North- and South-bound link traffic, passing it de-multiplexed and framed to a logic analyzer. The high speed ports (link interfaces) run at 2.4 to 4.8 GT/s. At these frequencies it is virtually impossible to physically probe the signals. In addition, input to the logic analyzer capture module is limited to operation below about 800 MHz. To resolve this issue the buffer operating in a LA interface mode decodes link activity and sends the decoded, de-multiplexed data out through the DRAM pins for direct input to LA capture modules. In this mode the north and south-bound links will pass data to the next buffer in the normal manner. Triggering events on the links will be recognized using protocol-aware logic and match registers in order to supplement native triggering capabilities of the logic analyzer. Simple filtering of events may be performed in the buffer with simple signals passed to the logic analyzer to qualify trace storage.

LAI mode can be incorporated in the AMB design or in a dedicated chip. This function is recommended but not required as a test mode in the AMB design.

An LAI card is being developed to provide link traffic trace capability to support debug and validation needs for systems featuring FBDIMM links. The FBDIMM LAI probing solution is intended to support silicon debug and evaluation of memory channel behavior.

In the LAI mode, the AMB performs the following functions:

- Retain normal repeater pass-through southbound and northbound links.
- Perform enough link protocol unwinding to provide extraction of frame boundaries, idle filtering opportunities, and pattern match triggering.
- Enable independent de-multiplexed Northbound and Southbound traffic stream in LA compatible signal levels and timing format using AMB DDR IO pins.
- Provide system independent SMB access to configure the AMB in LAI mode.

As illustrated in Figure 5-3 the AMB in LAI mode passes data to the next AMB in the chain as normal as well as providing decoded data and event triggers to a logic analyzer via the DRAM pins. The pass through data may be sent to the displaced DIMM, allowing full channel memory capacity while in LAI mode.

5.5.1 Logic Analyzer Interface (cont'd)

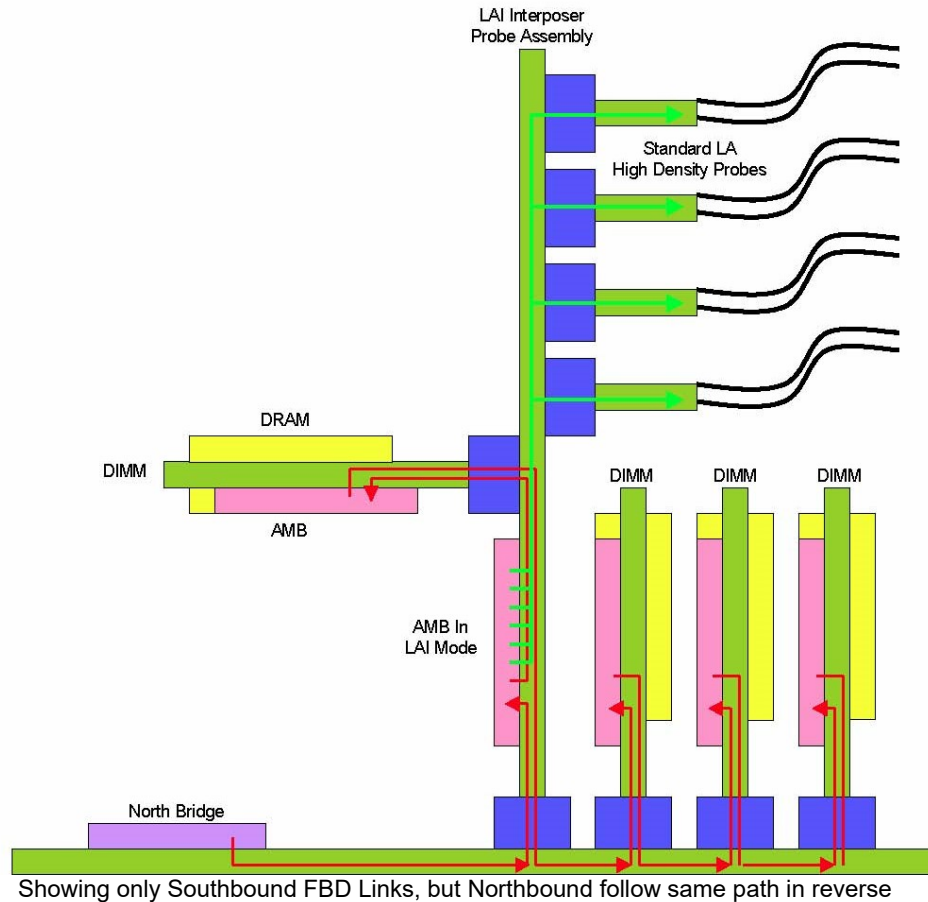


Figure 5-3 — Logic Analyzer Interface Card

The LAI interposer features a single buffer chip which operates in a Logic Analyzer Interface (LAI) mode, a standard slot for installation of the first DIMM on the chain, and connectors (or direct attach cables) for output to a logic analyzer. The connector for the interposed DIMM is assumed to be the normal vertical connector, but alternate connector styles, such as angled or straddle mount, might be more appropriate to minimize possible physical interference problems. Users would install the LAI interposer on one or more FBDIMM links within a target system to trace link activity. Additional cables to provide LAI power, SMB programming and cross-triggering between multiple LAI are not shown, but would be required.

5.5.2 DC Testing

At component level all pins may be tested in the conventional manner. The BIST engine can be programmed to drive outputs to the correct state for drive strength testing.

At DIMM level, most assembly-related defects can be detected with a simple functional test. The MemBIST engine may be programmed to walk a one or a zero across the 72 data bits. Toggling one pin at a time will detect all possible open or shorted conditions. The same is true for address lines - the walking data pattern (or other BIST pattern) may be repeated over the address space.

5.6 Host Controller Requirements

The host controller will have access to the buffer either in-band through the FBDIMM memory channel or out of band through SMBus. Since FBDIMM has a controller-target architecture the host will be responsible for initializing the channel and directing operations within the memory buffer. For the most part this is no different than normal operation. However the host must understand how to work with buffers that are in LAI or other special modes of operation.

6 AMB Component DfX

6.1 Normal Mode Debug/Validation Hooks

Each AMB used to buffer DRAM shall require a minimum set of debug features to support debug/validation of both HW and SW at the channel, component, and system levels. These features are defined in the following clauses.

6.2 Error Injection and In-Band Events

Debug and validation require selectable stimuli to drive timing of response mechanisms.

6.2.1 Decode of Southbound In-Band Debug Events

Each AMB shall support detection and decode of In-band Debug Commands and conversion of each of the eight carried events into local event pulses. These local events then can be used as stimuli for various response mechanisms defined below.

6.2.2 Pattern Match on a Command

The AMB will support pattern matching on command position A, B or C using one mask and one value register. This local event may be used as stimulus for various response mechanisms defined below. If LAI mode is supported as described below the pattern matching mechanism in LAI should be used instead.

6.2.3 Programmed Event Delay

Because it is difficult to time sensed events (in-band or command match) with the desired response time, the AMB must provide a programmable event delay. This programmable delay must accommodate a minimum of 63 frame times.

6.2.4 Error Injection

The AMB supports injection of specific errors in response to selected in-band events or stimulated by mask/match of commands arriving at the AMB, or in one case (stuck lanes) directly via control registers on the AMB.

There are several types of errors that buffers must be able to inject in order to enable validation and debug hardware and software mechanisms intended to deal with each error type in operating systems.

6.2.4.1 Errors Injected In Northbound Read and Read Data Frames

In response to a selected local event, the AMB will inject an error in frame data during or after calculating frame CRC's to be transmitted Northbound.

6.2.4.1.1 Force Alert

In response to a selected local event, the AMB will force an alert Northbound. Note that forcing an error status in a following status block will likely be required.

6.2.4.1.2 Selectively Force "Stuck" on Lanes

This capability is required to test ability of components and system to accomplish lane fail-over. Note that this is the only error injection feature which is not event driven, but rather shall be controlled directly by a register in the AMB.

6.2.5 Sourcing Northbound In-Band Event

The Northbound event shall be asserted in the next transmitted status block following assertion of a selected local event.

6.3 Logic Analyzer Interface Mode

Implementation of Logic Analyzer mode in the AMB is recommended, but it is not a required AMB feature. If implemented, LAI mode must follow the description in this specification. Note that LAI mode requires more sophisticated pattern matching capability than that described above for error injection. If LAI mode is supported the LAI pattern matching mechanism should be used for error injection.

The AMB in LAI mode converts the DRAM pins from the normal use to drive logic analyzer probes instead. The logic analyzer requires more pins than can be supplied from the data bus alone, so some of the CA pins are re-used to drive additional LA signals.

The primary uses of the LA features will be debugging FBDIMM or system issues that will have visibility through the FBDIMM channels or observing the AMB for correct behavior in a system environment. This observability may be used to verify hardware, software or BIOS functionality.

6.3 Logic Analyzer Interface Mode (cont'd)

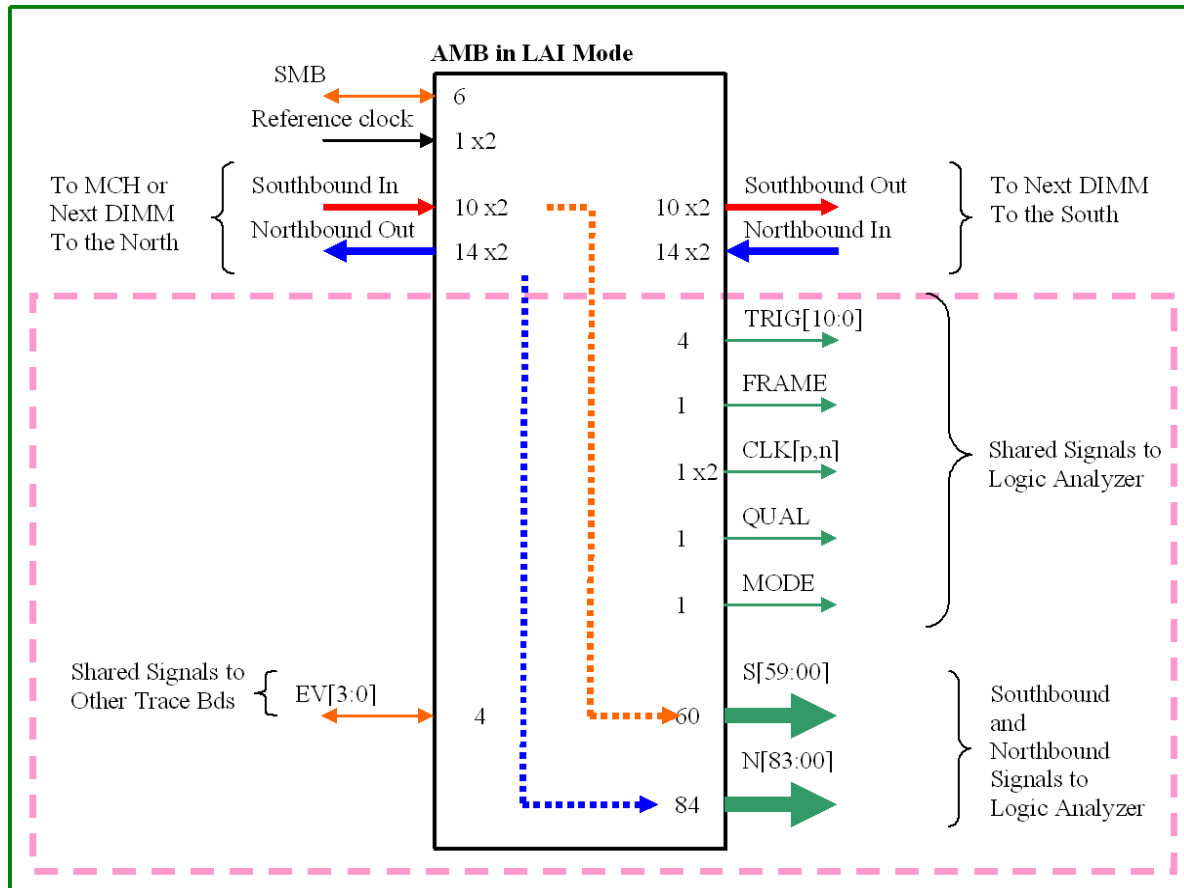


Figure 6-1 — AMB LAI Mode Signals

6.3.1 Link Protocol Validation/Debug

In this scenario, traces will be captured of single FBDIMM links performing simple to complex operations. The traces will be used to debug low level link protocol/operations (link init, retraining, power transitions, resets, error recovery, and other normal link transactions). For this purpose the host side agent would usually initiate traffic as result of diagnostic or focus test software execution, rather than operating system/application activity, since this would allow specific behaviors to be produced repeatedly and without significant interference due to other link activity. Analysis of the traces could be primarily manual, since it is expected to be fairly simple, although automated checkers could also be employed to check rigorously for protocol flaws.

6.3.2 LAI Debug Examples

In this case traces would be used to debug/validate BIOS (and other SW) configuration of buffer chip register write and read sequences as part of system initialization.

Memory controller logic interaction with AMB may be captured to enable debug of DRAM control issues. FBDIMM traffic would reveal the exact sequences and timing of interactions, aiding diagnosis of the problem. The FBDIMM trace could also be used to validate and debug test software used to stress the memory components.

6.3.3 System Level Debug

Traces of FBDIMM traffic under normal operating system and application execution might reveal important clues about misbehavior of logic elsewhere in the system. In this case the interaction with FBDIMM and DRAM may work flawlessly, but the content and/or sequencing of the traffic on the link can be used to provide indirect observability of system behavior. The trace data, with time stamps, could also be combined with other data for a complete record of the system state leading to an event or failure.

System Debug Case - FBDIMM on Processor

When a FBDIMM channel is hosted directly by a processor chip, additional debug data will be needed as other trace data won't provide adequate clues on what agent initiated transactions to memory via the FBDIMM channel. A debug mode supporting additional debug bits per command can provide agent ID and/or other debug information (definition for exposing these added debug bits synchronously in FBDIMM frames is provided in later clauses).

6.3.4 LAI Mode Architecture

The diagram below illustrates the AMB as a functional block when used as an LAI. The normal Southbound and Northbound links, the reference clock, and the SMBus are used “as is” with the DRAM interface reused for added LAI functionality. To be effective in collecting useful FBDIMM traces, the information provided to a logic analyzer must include not only a demuxed copy of the direct information transferred on the links, but also several types of derived information that a logic analyzer is not equipped to derive itself. These include specifically:

- Cross-triggering information with finer timing granularity than LA can achieve
- Filtering (qualified storage) opportunities recognition
- Traffic framing

A normal mode AMB will have to be configured to operate in the LAI mode. The AMB BFUNC and SA[2:0] pins define the buffer operating mode (normal, repeater, and LAI). The last four combinations of those bits represent the LAI mode (see Table 6-1). The two most significant pins (along with a fuse) have to be correctly set to enable the AMB to function as a Logic Analyzer Interface buffer.

6.3.4 LAI Mode Architecture (cont'd)

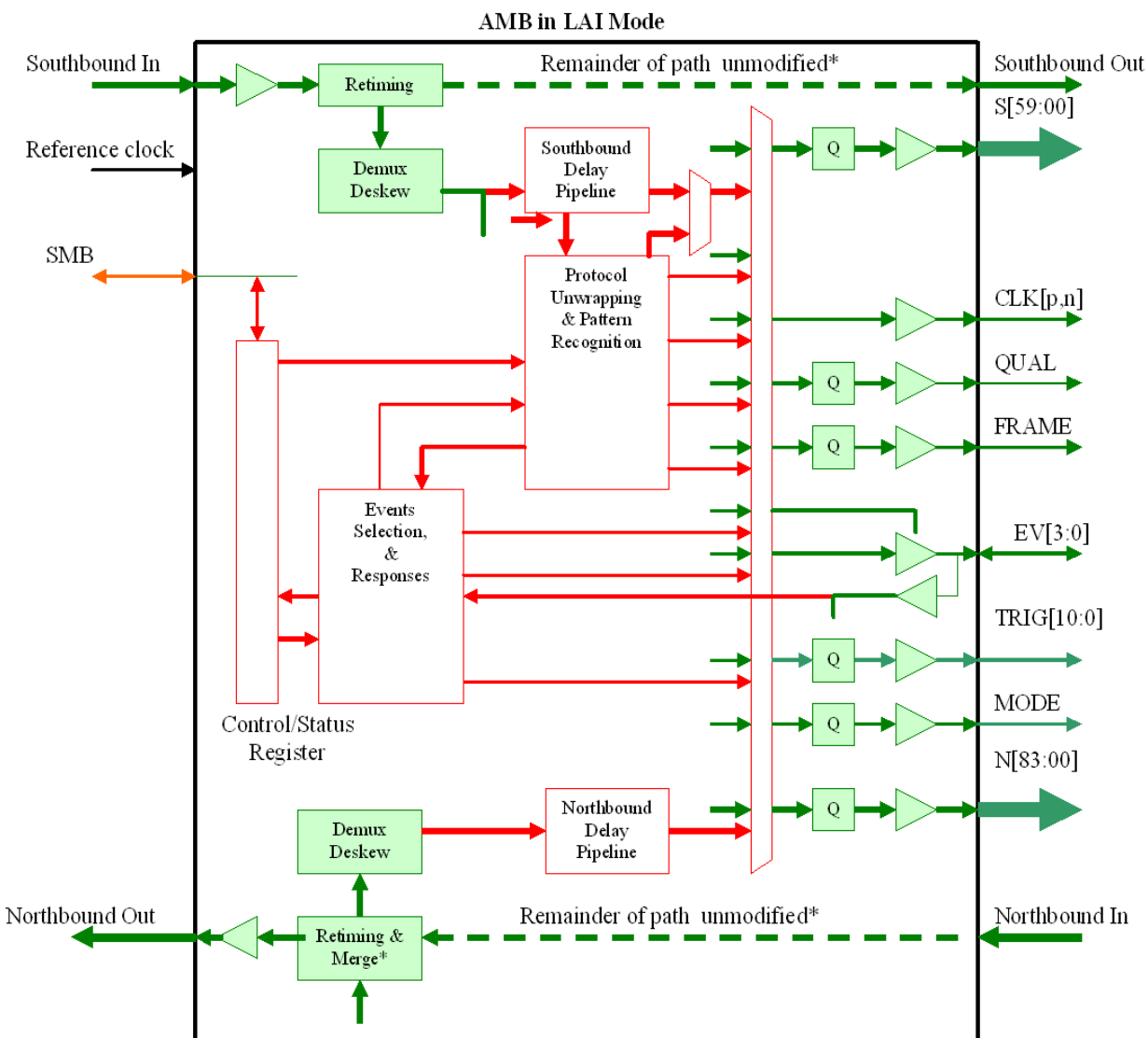


Figure 6-2 — AMB LAI Mode Architecture

Table 6-1 — AMB SMBus Addressing for Logic Analyzer Mode

AMB BFUNC, SA[2:0]	AMB Function (other modes not shown)
1100	Logic Analyzer Interface 0
1101	Logic Analyzer Interface 1
1110	Logic Analyzer Interface 2
1111	Logic Analyzer Interface 3

6.3.4 LAI Mode Architecture (cont'd)

As the most two significant bits are pulled high to define the logic analyzer mode, only four AMB or similar devices can be addressed on a single SMBus, i.e., with the addresses 1100, 1101, 1110, and 1111. Also, to avoid any conflict and errors in configuration programming via the SMBus, the LAI configuration registers should not normally be dually accessible by the FBDIMM link and LAI.

6.3.4.1 Configuration of LAI Device

The Logic Analyzer Interface buffers will only be addressable using SMBus. The AMB device on the LAI card will not normally be connected to the System SMBus channel, except immediately following channel hard Reset and possibly at other (infrequent) times to set critical link interface parameters necessary to allow the LAI to operate on the link. These shall necessarily occur prior to starting any link training. Normal isolation of the AMB-LAI from the system SMBus is necessary to avoid conflict between the system controller and AMB-LAI configuration controller when the LA is setting LAI mode parameters. An external SMBus controller will be used to configure the AMB-LAI. In the laboratory, more than one AMB-LAI device can be on the same SMBus, in which case there is an additional constraint that the SMBus addresses for each AMB-LAI must be configured with different values to be able to program each separately.

6.3.4.2 Pin Assignment

In LAI mode the DRAM interface pins will be remapped to logic analyzer mode signals to send traffic and data to the logic analyzer. All the LAI signals (except the event bus pins) will transmit signals to the Logic analyzer. The event pins will both transmit on and receive data from the event bus. The AMB-LAI signals must be correctly mapped to the appropriate DRAM interface IO, as not all the AMB-LAI signals have the same electrical characteristics.

6.3.4.3 DDR Pin Reuse

The DDR interface, i.e., i/o buffers and pins will be re-used to transmit or receive the LAI signals. Based on the available DDRII pin out, there are just enough DDR pins to map against the required LAI signals. Therefore, no additional pins will be added to accommodate the AMB-LAI mode. Most LAI signals are required to operate at equivalent DDR speed. The LAI signals will be single-ended, except the clocking, which will be the differential DRAM clock.

All AMB-LAI signals except the Event signal i/o will transmit data to the logic analyzer. The event bus does not connect to the logic analyzer but has a daisy chain topology connecting all AMB-LAIs. This will allow communication of event triggers between AMB and similar components.

6.3.4.4 FBDIMM Signals

The FBDIMM signals will be operating unmodified from the default normal mode. The signals will connect to the preceding AMB or host-interface on the primary side. In the secondary side it will connect to the downstream DIMM AMB. The FBDIMM channel will operate at link speed. The AMB-LAI along with the two AMB on the two downstream DIMMs must run at full strength (and correct pre-emphasis level) even if the other AMB-DIMMs are configured differently to operate in half strength mode to conserve power. Check design guide to determine which of the SB and NB in the two downstream AMB devices must be operated in full strength.

6.3.4.4 FBDIMM Signals (cont'd)

The default drive strength in AMB-LAI will be full strength. The System SMBus may have to be provided direct access to the AMB-LAI to configure select registers which are necessary to make the channel acceptably functional. FBDIMM systems should not be allowed to reconfigure the drive strength register in the AMB-LAI using the in-band commands. To avoid potential conflict, the LAI SMBus management resource should not be used to modify these CSRs.

6.3.4.5 LAI Signal List

The LAI signals at the DRAM interface are listed below. All of the AMB-LAI signals (except the Event signals) will transmit data to the logic analyzer. The event bus does not connect to the logic analyzer in its topology. It implements a daisy chain to connect AMB-LAIs. This allows transmission and receipt of event triggers between AMB and similar components. More description are given later.

Table 6-2 — LAI Mode Signal and Pin Count

AMB Signal in LAI Mode	Signal Name	Pins	Comment
Northbound Data	N[83:0]	84	FBDIMM signal
Southbound Data	S[59:0]	60	FBDIMM signal
Trigger signal	TRIG[10:0]	11	LAI mode signal
Clk – differential	CLK[1:0]	2	One differential clock
Qualifier	QUAL	1	LAI mode signal
Frame boundary identifier	FRAME	1	LAI mode signal
Event signals	EV[3:0]	4	AMB-AMB shared signal
FBDIMM Mode signal	MODE	1	LAI mode signal
Total		164	

6.3.4.6 Pattern Matching

The LAI block can pattern match on three command values at any of three positions and combine the results into independent and combined local events. There are 13 total pattern matching events: a command value matches a command slot (9 events), a command value matches any slot (3 events), and all command values appear in the frame (1 event).

A pictorial presentation of the LAI match and mask logic is shown in Figure 6-3.