

JEDEC STANDARD

Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3/DDR3L/DDR3U RDIMM 1.5 V/1.35 V/1.25 V Applications

JESD82-29A.01

(Editorial Revision of JESD82-29A, December 2010)

SEPTEMBER 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by

©JEDEC Solid State Technology Association 2022

3103 North 10th Street

Suite 240 South

Arlington, VA 22201-2107

JEDEC retains the copyright on this material.

By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.

All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by the JEDEC Solid State Technology Association and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street, Suite 240 South
Arlington, Virginia 22201-2107

or refer to www.jedec.org under Standards and Documents for alternative contact information.

This page intentionally left blank

DEFINITION OF THE SSTE32882 REGISTERING CLOCK DRIVER WITH PARITY AND QUAD CHIP SELECTS FOR DD3/DDR3L/DDR3U RDIMM 1.5 V, 1.35 V, OR 1.25 V APPLICATIONS

(From JEDEC Board Ballot JCB-10-55, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTE32882 registered buffer with parity for driving address and control nets on DDR3/DDR3L/DDR3U RDIMM applications.

The purpose is to provide a standard for the SSTE32882 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTE32882 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for 1.5 V, 1.35 V, or 1.25 V V_{DD} operation.

All inputs are 1.5 V, 1.35 V, or 1.25 V CMOS compatible. All outputs are 1.5 V, 1.35 V, or 1.25 V CMOS drivers optimized to drive single terminated 25..50 Ohms traces in DDR3/DDR3L/DDR3U RDIMM applications. The clock outputs Y_n and $Y_n\#$ and control net outputs Q_nCKEn , $Q_nCSn\#$ and Q_nODTn can be driven with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882 has two basic modes of operation associated with the Quad Chip Select Enable (QCSSEN#) input. When the QCSSEN# input pin is open (or pulled HIGH), the component has two chip select inputs, DCS0# and DCS1#, and two copies of each chip select output, QACS0#, QACS1#, QBCS0# and QBCS1#. This is the "QuadCS disabled" mode. When the QCSSEN# input pin is pulled LOW, the component has four chip select inputs DCS[3:0]#, and four chip select outputs, QCS[3:0]#. This is the "QuadCS enabled" mode. Through the remainder of this specification, DCS[n:0]# will indicate all of the chip select inputs, where $n=1$ for QuadCS disabled, and $n=3$ for QuadCS enabled. QxCS[n:0]# will indicate all of the chip select outputs.

The SSTE32882 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going HIGH, and CK# going LOW. The data could be either re-driven to the outputs once exactly one of the input signals DCS[n:0]# is driven LOW or it could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in 2.2.

Based on control register settings the device can change its output characteristics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

2.1.1 Initialization

The DDR3/DDR3L/DDR3U RCD (Ultra Low Voltage) SSTE32882 can be powered-on at 1.5 V, 1.35 V, or 1.25 V. After the voltage transition, stable power is provided for a minimum of 200 μ s with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. Therefore the reference voltage (VREF) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a **LOW** to **HIGH** transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

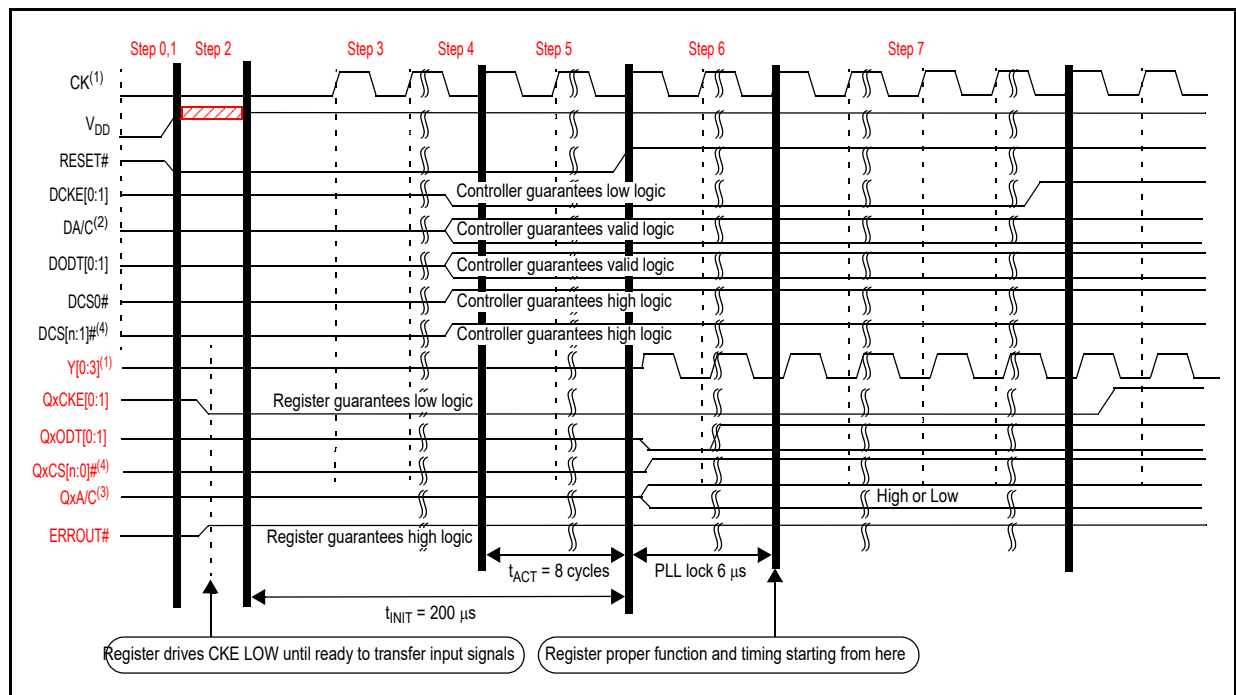


Figure 1 — Timing of Clock and Data During Initialization Sequence

NOTE 1 CK# is left out for better visibility

NOTE 2 DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

NOTE 3 QxCKEn, QxODTn, QxCsSn# are not included in this range.

NOTE 4 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

2.1.1 Initialization (cont'd)

From a device perspective, the initialization sequence must be as shown in [Table 1](#).

Table 1 — SSTE32882 Device Initialization Sequence¹

Step	Power	Inputs: Signals Provided by the Controller								Outputs: Signals Provided by the Device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0] ²	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK CK#	QCS# [n:0] ²	QODT [0:1]	QCKE [0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT ³
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
1	0→V _{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2 ⁴	VDD 1.5 V→1.35 V 1.35 V→1.5 V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L ⁵	Z	H ⁵	Z	Z
3	V _{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
4	V _{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ⁶	L	X	H	running	running
7 ⁷	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12 , Table 14 and Table 16).						

NOTE 1

X = Logic LOW or logic HIGH. Z = floating.

NOTE 2

n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

NOTE 3

The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.

NOTE 4

The system may power up using either 1.5 V, 1.35 V or 1.25 V. The BIOS reads the SPD and adjusts the voltage if needed. Stable power is provided for a minimum of 200 μs with RESET# asserted.

NOTE 5

QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5 V, 1.35 V or 1.25 V (nominal).

NOTE 6

This indicates the state of QxODTx after RESET# switches from **LOW**-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) μs, the state of QxODTx is a function of DODTx (HIGH or **LOW**).

NOTE 7

Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is “0”, except for RC6 and RC7, which are vendor-defined. After initialization, the memory controller does only need to write to those control registers whose contents need to be changed.

2.1.1.1 Reset Initialization with Stable Power

The timing diagram in Figure 1 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3.

2.1.1.1 Reset Initialization with Stable Power (cont'd)

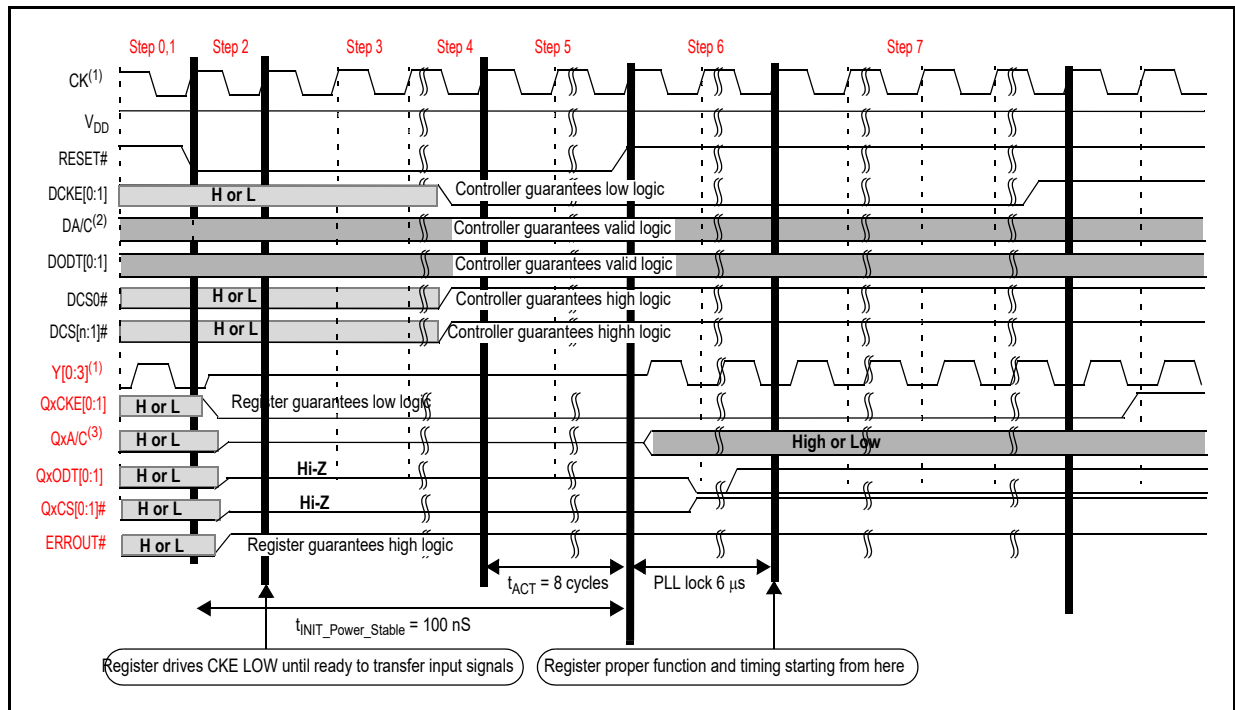


Figure 2 — Timing of Clock and Data During Initialization Sequence with Stable Power

NOTE 1 CK# left out for better visibility

NOTE 2 DCE0, DCE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

NOTE 3 QxCKEn, QxODTn, QxCSn# are not included in this range.

NOTE 4 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

Table 2 — SSTE32882 Device Initialization Sequence¹ when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:1] ²	DODT [0:1]	DCE [0:1]	DA/C	PAR_IN	CK CK#	QCS# [0:1]	QODT [0:1]	QCKE [0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT ³
0	VDD	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
1	VDD	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
2	VDD	L	stable voltage	X	X	X	X	X	running	Z	Z	L ⁴	Z	H ⁴	Z	Z
3	VDD	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z	Z
4	VDD	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
5	VDD	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	VDD	H	stable voltage	H	X	L	X	X	running	H	L ⁵	L	X	H	running	running
7	VDD	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14, and Table 16).						

NOTE 1 X = Logic LOW or logic HIGH. Z = floating.

NOTE 2 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

NOTE 3 The feedback clock (FBOU and FBOU#) pins may or may not be actively driven by the device.

NOTE 4 QxCKEn and ERR OUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is nominal.

NOTE 5 This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) μs, the state of QxODTx is a function of DODTx (HIGH or LOW).

2.1.2 Parity

The SSTE32882 includes a parity checking function. The SSTE32882 accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT# pin (active **LOW**) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]# signals being **LOW**.

If an error occurs, and ERROUT# is driven LOW with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors ERROUT# becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE0, DCKE1, DCS0#, DCS1#, DODT0 and DODT1) are not included in the parity check computations.

2.1.2.1 Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT# is generated three input clock cycles after the corresponding data is registered. If ERROUT# goes **LOW**, it stays LOW for a minimum of two input clock cycles or until RESET# is driven **LOW**. Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

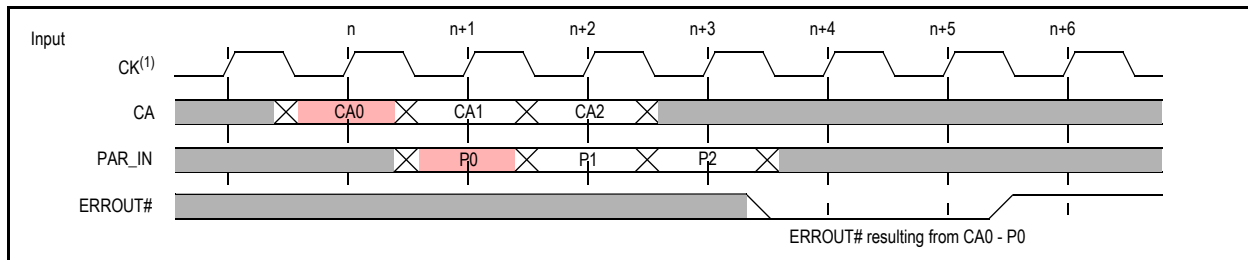


Figure 3 — Timing of Clock, Data, and Parity Signals

NOTE 1 CK# left out for better visibility

Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).

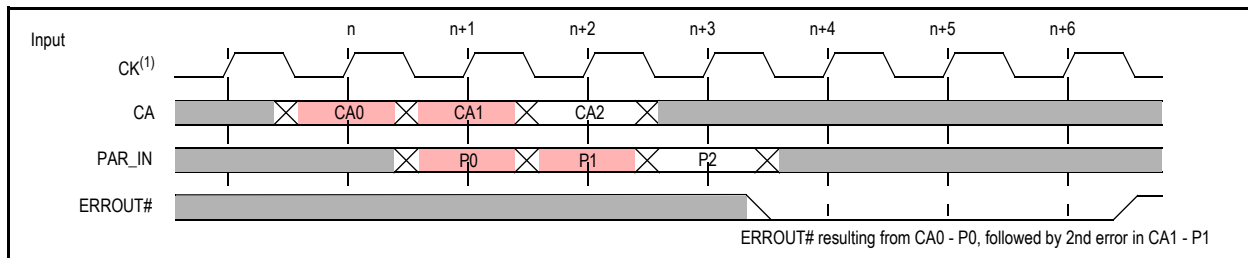


Figure 4 — Two Consecutive Parity-Error Occurrences

NOTE 1 CK# left out for better visibility

2.1.2.1 Parity Timing Scheme Waveforms (cont'd)

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and $n+2$ input clock cycles (PAR_IN clocked in on the $n+1$ and $n+3$ input clock cycles).

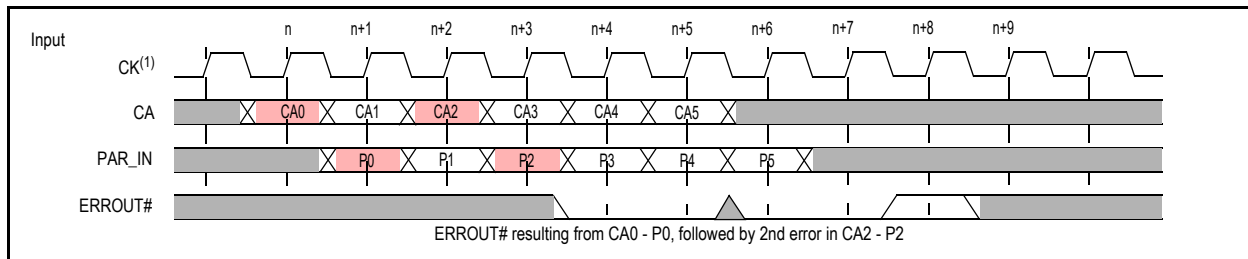


Figure 5 — Two Parity-Error Occurrences Separated by a Clock Cycle of No Error Occurrence

NOTE 1 CK# left out for better visibility

Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and $n+3$ input clock cycles (PAR_IN clocked in on the $n+1$ and $n+4$ input clock cycles).

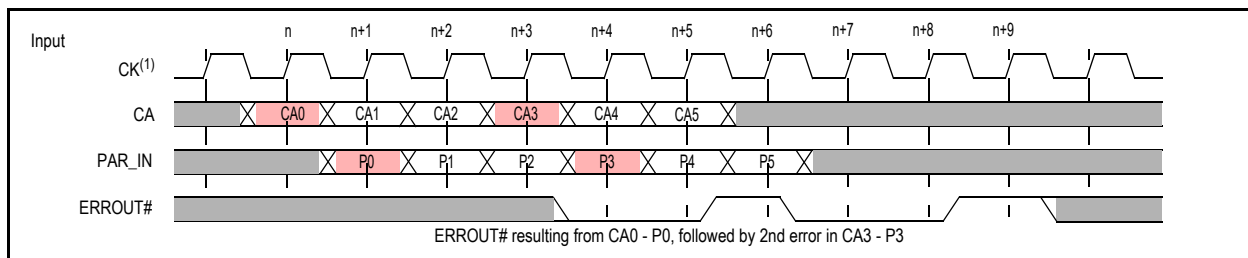


Figure 6 — Two Parity-Error Occurrences Separated by Two Clock Cycle of No Error Occurrence

NOTE 1 CK# left out for better visibility

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and $n+1$ input clock cycles (PAR_IN clocked in on the $n+1$ and $n+2$ input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

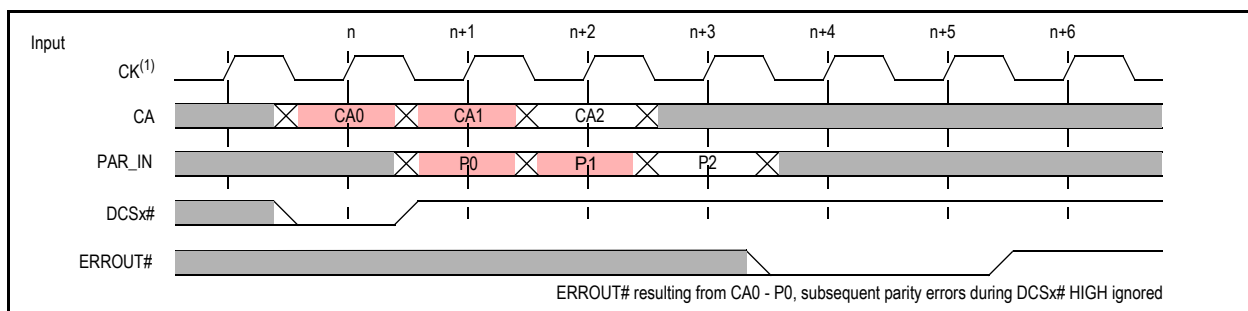


Figure 7 — Parity-Error Occurrence in Chip-Deselect Mode

NOTE 1 CK# left out for better visibility

2.1.2.1 Parity Timing Scheme Waveforms (cont'd)

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and $n+3$ input clock cycles (PAR_IN clocked in on the $n+1$ and $n+4$ input clock cycles). The data on the $n+3$ input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

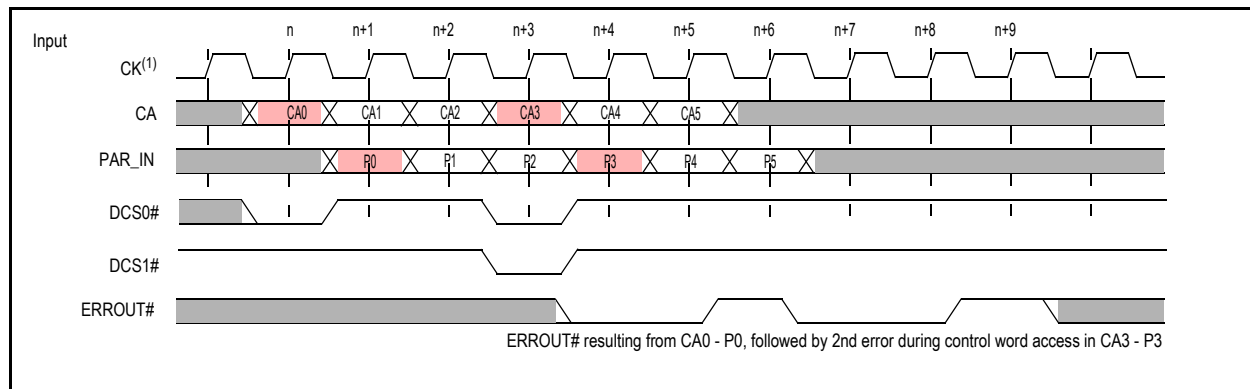


Figure 8 — Parity-Error Occurrences During Control Word Programming

NOTE 1 CK# left out for better visibility

2.1.3 Power Saving Modes

The device supports different power saving mechanisms.

When both inputs CK and CK# are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACE0, QACE1, QBCKE0 and QBCKE1 which are kept driven **LOW**. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK=CK#=LOW) will only put the SSTE32882 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when RESET# is driven **LOW**.

A float feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]# inputs and to float all outputs corresponding with the chip select gated inputs when all the DCS[n:0]# inputs are HIGH. If any one of the DCS[n:0]# input is **LOW**, the Qn outputs will function normally.

Once all the DCS[n:0]# inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The RESET# input has priority over all other power saving mechanisms. When RESET# is driven **LOW**, it will force the Qn outputs to float, the ERROUT# output HIGH, the QACE0, QACE1, QBCKE0 and QBCKE1 outputs LOW and disables Input Bus Termination (IBT).

2.1.4 Register CKE Power Down

The SSTE32882 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to **LOW**. If either input Chip Select signal, DCS[n:0]#, is asserted together with DCKEn, the SSTE32882 transfers the corresponding command to its outputs together with QxCKEn **LOW**.

There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 indicates whether register turns off IBT or keeps IBT on.

2.1.4.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers are disabled except for CK/CK#, DCKEn, FBIN/FBIN# and RESET#. Upon entry into CKE Power Down mode with IBT off, IBT will be off on all inputs except DCKEn.. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn **LOW**. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS} , the register can tolerate floating input except for CK/CK#, DCKEn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven **LOW**. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven **LOW**. This is shown in Figure 9.

2.1.4.1 Register CKE Power Down with IBT Off (cont'd)

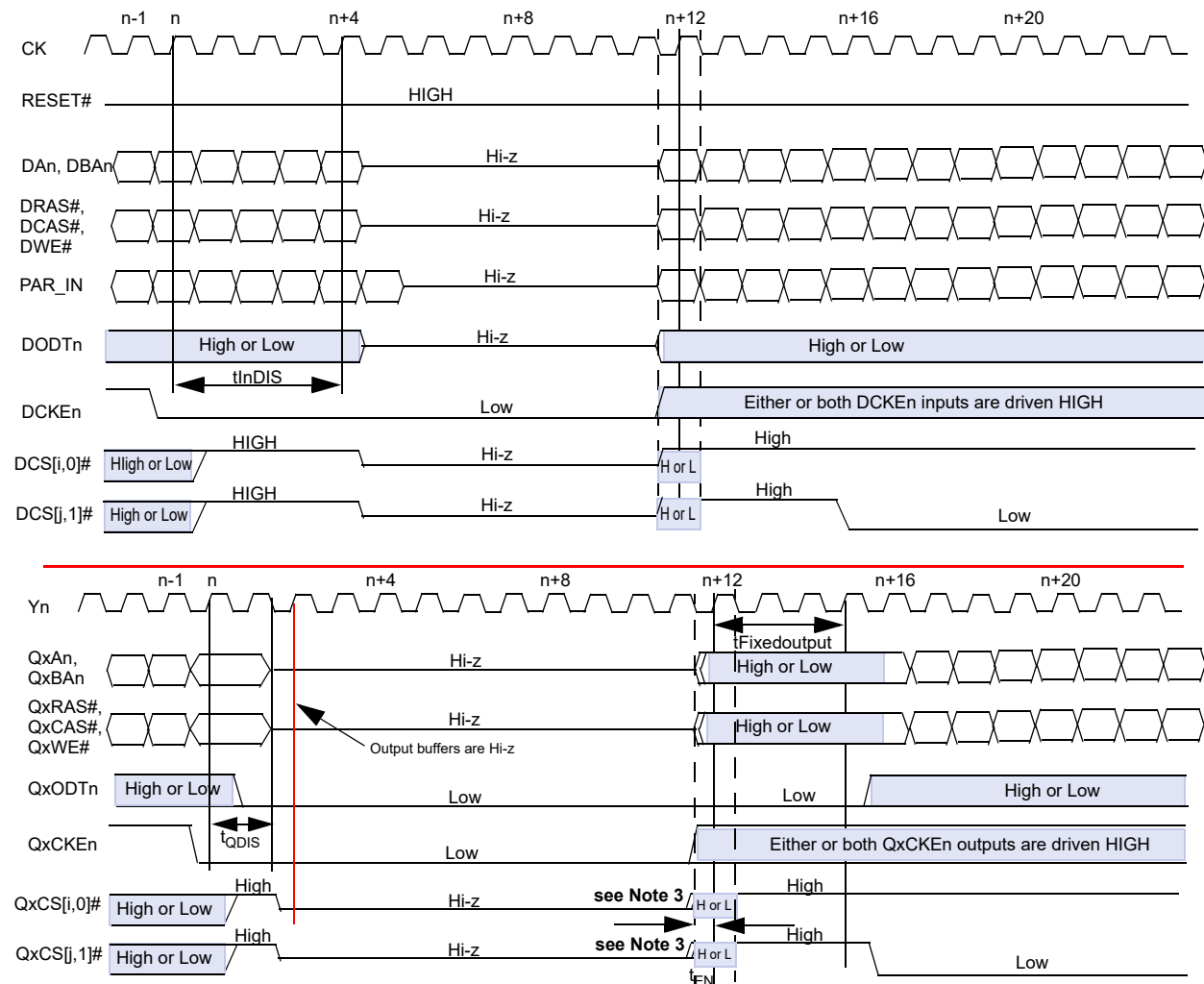


Figure 9 — Power Down Mode Entry and Exit with IBT Off

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3

NOTE 2 QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SST32882 into Register Control Word access mode.

NOTE 3 Upon CKE Power Down exit, QxCsn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for t_{FIXEDOUTPUT} regardless of what DCSn# input level is. For all other operation QxCsn# outputs will follow DCSn# inputs.

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately starts driving HIGH on the appropriate QxCKEn signal. The QxCsn# signals are driven HIGH and QxODTn signals are driven **LOW**. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all register outputs when QxCKEn goes HIGH. The register drives output signals to these levels for t_{FIXEDOUTPUT} to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within t_{FIXEDOUTPUT} clocks after DCKEn input is driven HIGH. This is shown in Figure 9.

2.1.4.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down mode with IBT on, all register input buffers are disabled except for CK/CK#, DCKEn, DODTn, FBIN/FBIN# and RESET#. Upon entry into CKE Power Down mode with IBT on, IBT will remain on for all inputs. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn **LOW**. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS} , the register can tolerate floating input except for CK/CK#, DCKEn, DODTn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOU/FBOU#. The Yn/Yn# and FBOU/FBOU# outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven **LOW**. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven **LOW**. This is shown in Figure 10.

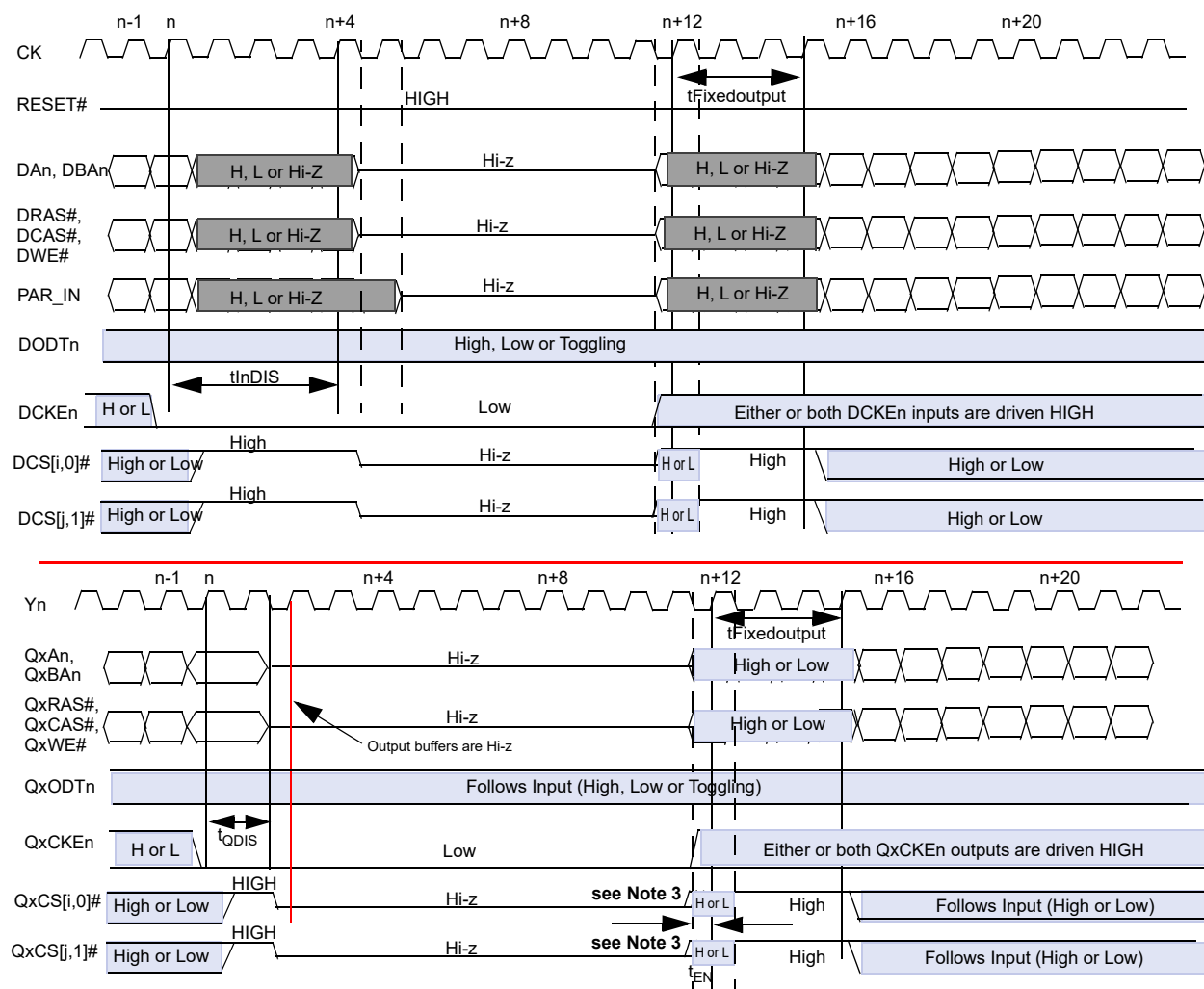


Figure 10 — Power Down Mode Entry and Exit with IBT On

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3

NOTE 2 QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.

NOTE 3 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for $t_{FIXEDOUTPUT}$ regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

2.1.4.2 Register CKE Power Down with IBT On (cont'd)

To re-enable the SSTE32882 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the SSTE32882 immediately starts driving HIGH on the appropriate QxCKEn signals. The QxCsn# signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The device drives output signals to these levels for $t_{\text{Fixedoutput}}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The device guarantees that input receivers are stabilized within $t_{\text{Fixedoutput}}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10.

2.1.5 Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the SSTE32882 supports a Clock Stopped power down mode. When both inputs CK and CK# are being held LOW ($V_{\text{IL (static)}}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 11, “Clock Stopped Power Down Entry and Exit with IBT On” and Figure 12, “Clock Stopped Power Down Entry and Exit with IBT Off”. The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which must be kept driven LOW. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0 and QxCKE1 can be disabled.

2.1.5.1 Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, DCKEn will continue be deasserted for a minimum of one tCKoff before pulling CK and CK# LOW. After holding CK and CK# LOW ($V_{\text{IL (static)}}$) for at least one tCKEV, both CK and CK# can be floated (because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer, CK/CK# will stay at LOW even though they are not being driven). The register is now in Clock Stopped Power Down mode. After CK and CK# are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can be floated (if needed to be float). At this point, all input receivers and input termination of the SSTE32882 are disabled. The only active input circuits are CK and CK#, which are required to detect the wake up request from the host.

2.1.5.2 Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS[n:0]# must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within tACT after CK and CK# resumed normal operation, the SSTE32882 outputs start becoming a function of their corresponding inputs. The state of the DCS[n:0]# inputs must not be changed before the end of tSTAB. The input clock CK and CK# must be stable for a time equal or greater than tSTAB before any access to the SSTE32882 can take place.

2.1.5 Clock Stopped Power Down Mode (cont'd)

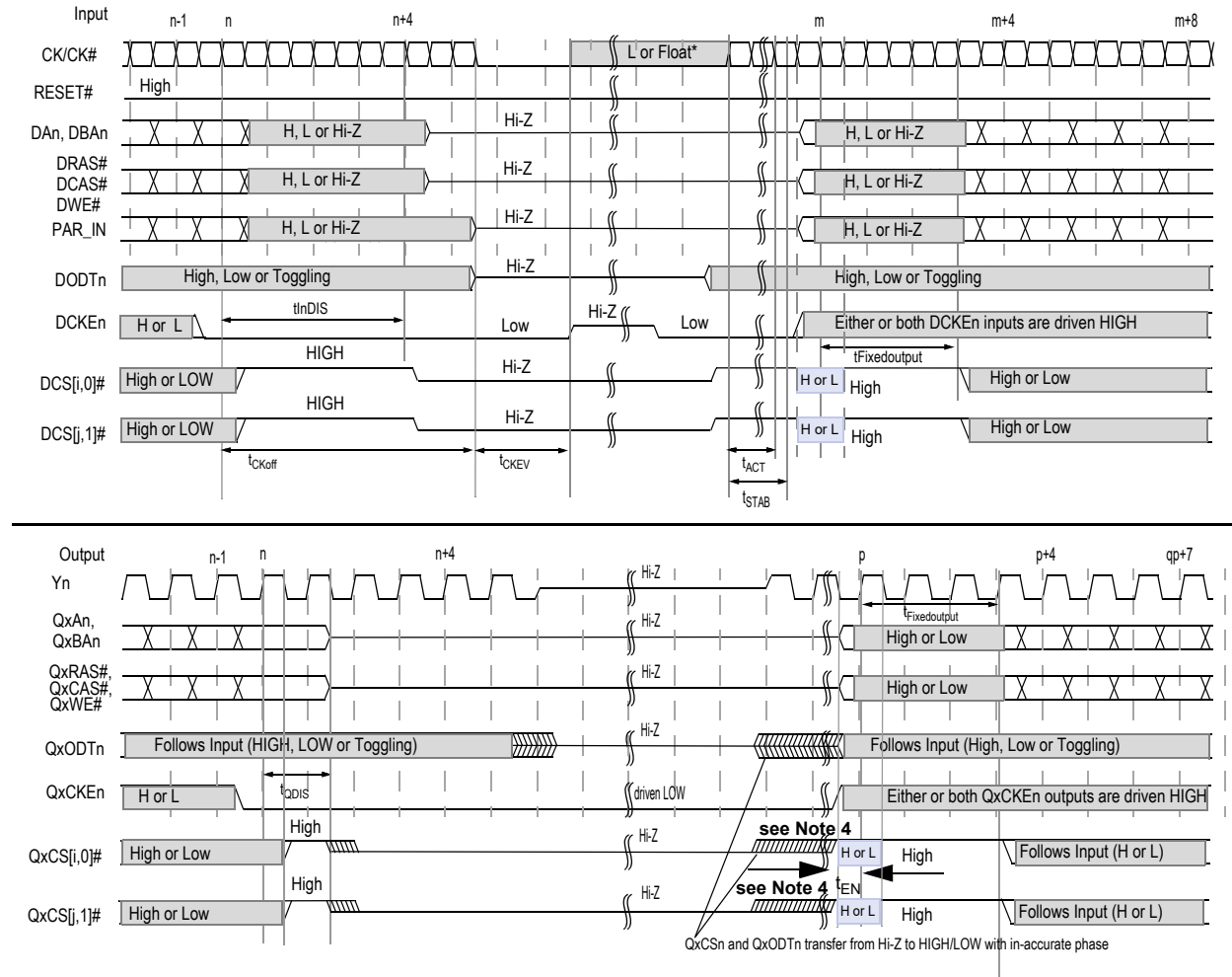


Figure 11 — Clock Stopped Power Down Entry and Exit with IBT On

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, $i = 2, j = 3$

NOTE 2 With RC9 DBA0='0'

NOTE 3 When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.

NOTE 4 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 t_{CK} , or be held HIGH for $t_{FIXEDOUTPUT}$ regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

2.1.5 Clock Stopped Power Down Mode (cont'd)

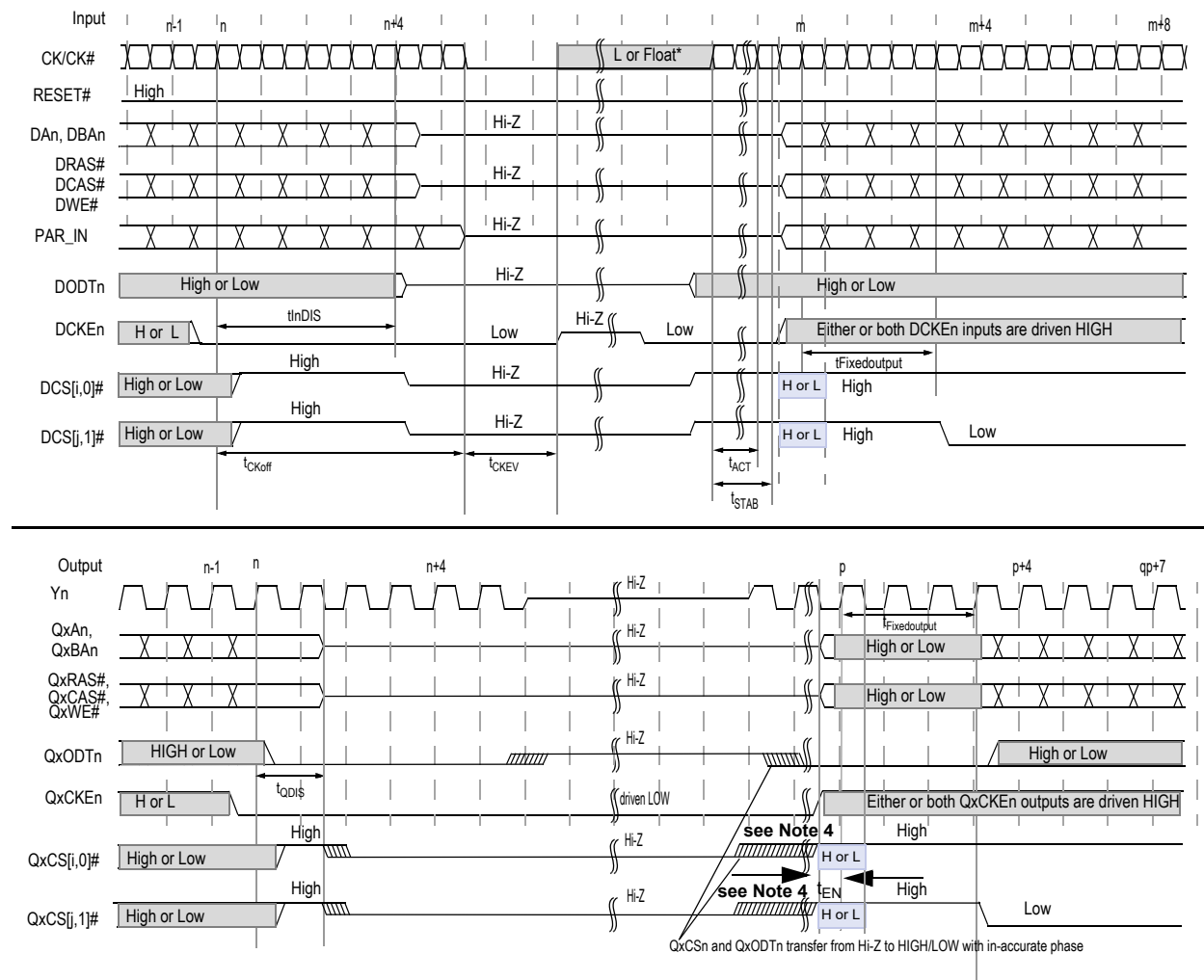


Figure 12 — Clock Stopped Power Down Entry and Exit with IBT Off

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, $i = 2, j = 3$

NOTE 2 With RC9 DBA0='1'

NOTE 3 When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.

NOTE 4 Upon CKE Power Down exit, QxCsn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for tFIXEDOUTPUT regardless of what DCSn# input level is. For all other operation QxCsn# outputs will follow DCSn# inputs.

2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET# is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

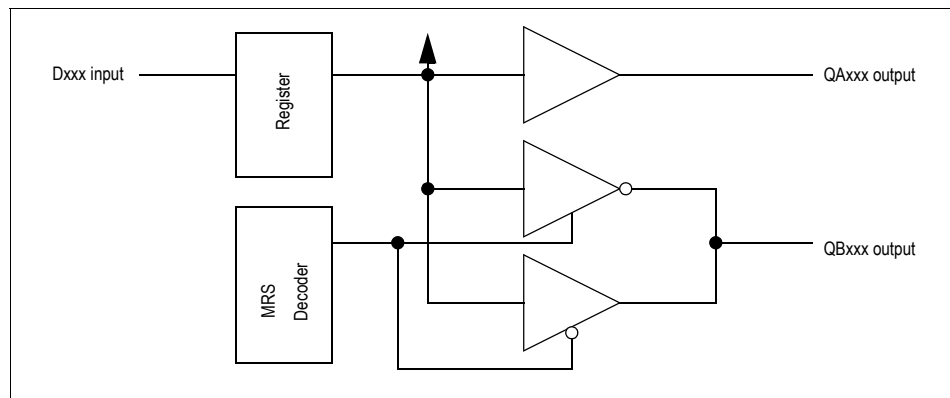


Figure 13 — Output Inversion Functional Diagram

The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the SSTE32882 are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the device supports 3T timing. If this feature is invoked the device drives the received data on its outputs for three cycles instead of one. The only exception are the QxCS[n:0]# outputs, which are the QACS0#, QACS1#, QBCS0# and QBCS1# outputs in the QuadCS disabled mode and are QCS[3:0]# in the QuadCS enabled mode.

When the device decodes the MRS command (DRAS#=0, DCAS#=0, DWE=0 and only one DCSn#=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QnCSx# signal to the DRAM. Back-to-back MRS command via the SSTE32882 must have a minimum of three clock delays. The SSTE32882 will automatically enable Output Inversion if there is no DRAM MRS command three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 14, Figure 15 and Figure 16.

2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

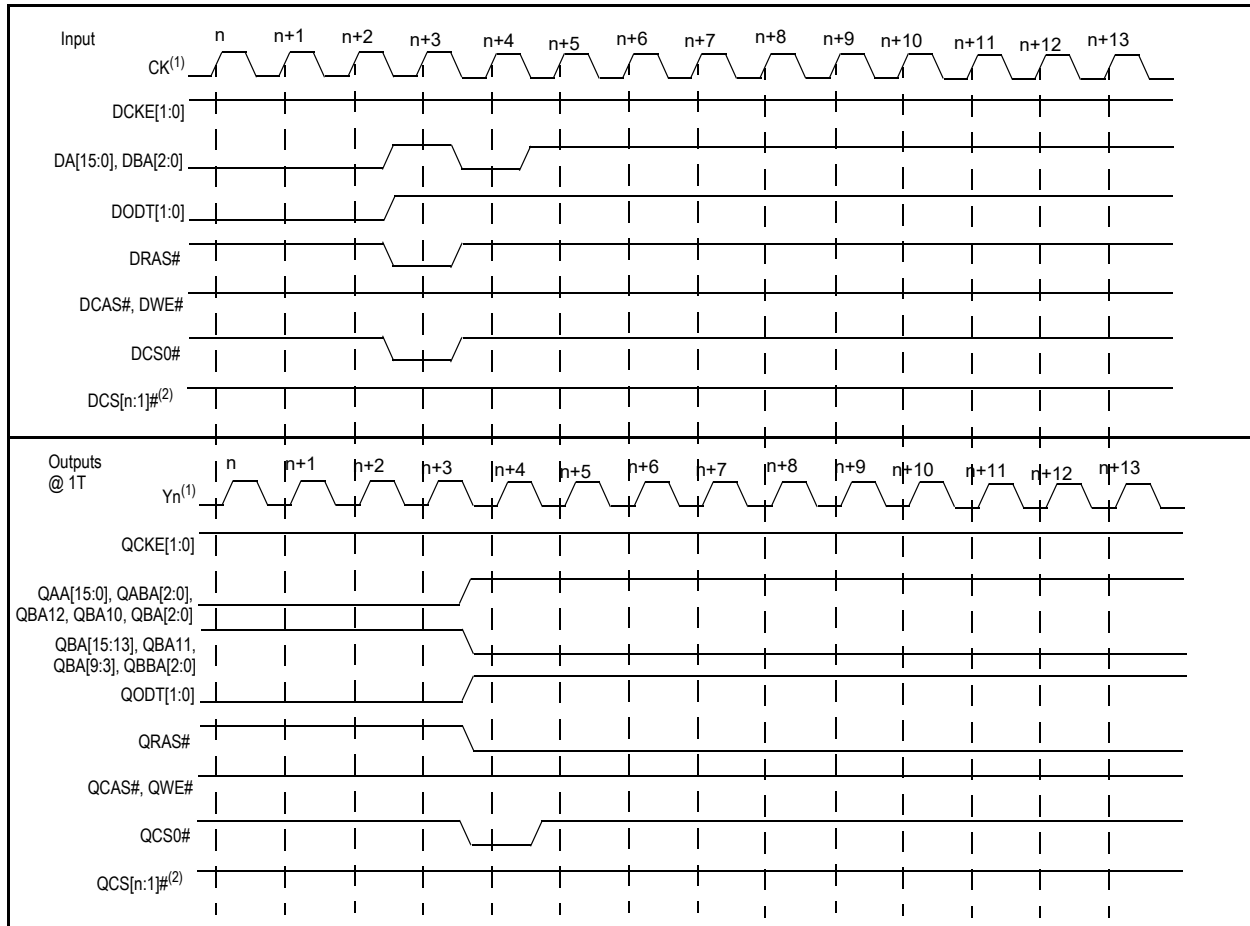


Figure 14 — 1T Timing During Normal Operation

NOTE 1 CK# and Yn# left out for better visibility

NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

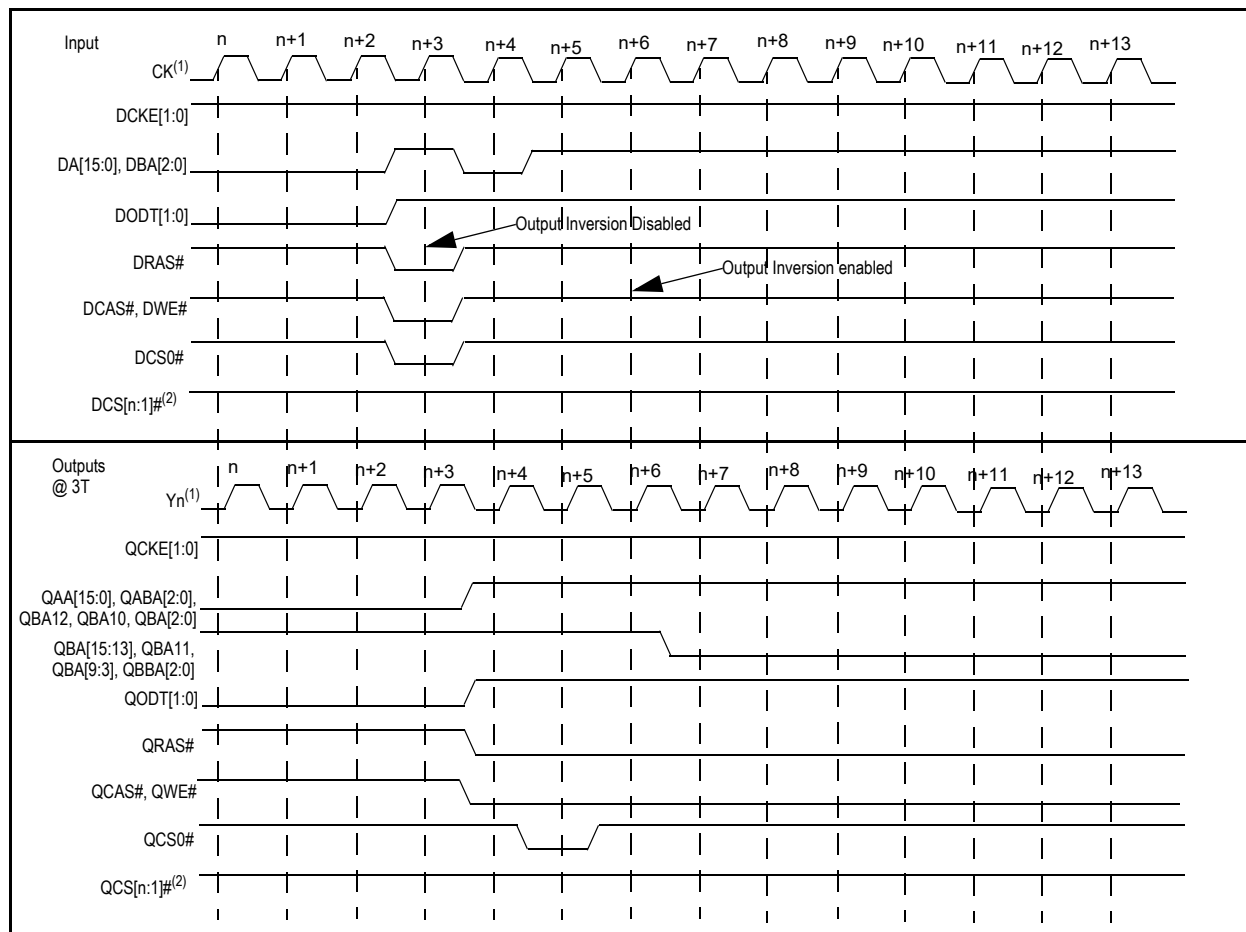


Figure 15 — 3T Timing During DRAM MRS Command

NOTE 1 CK# and Yn# left out for better visibility

NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

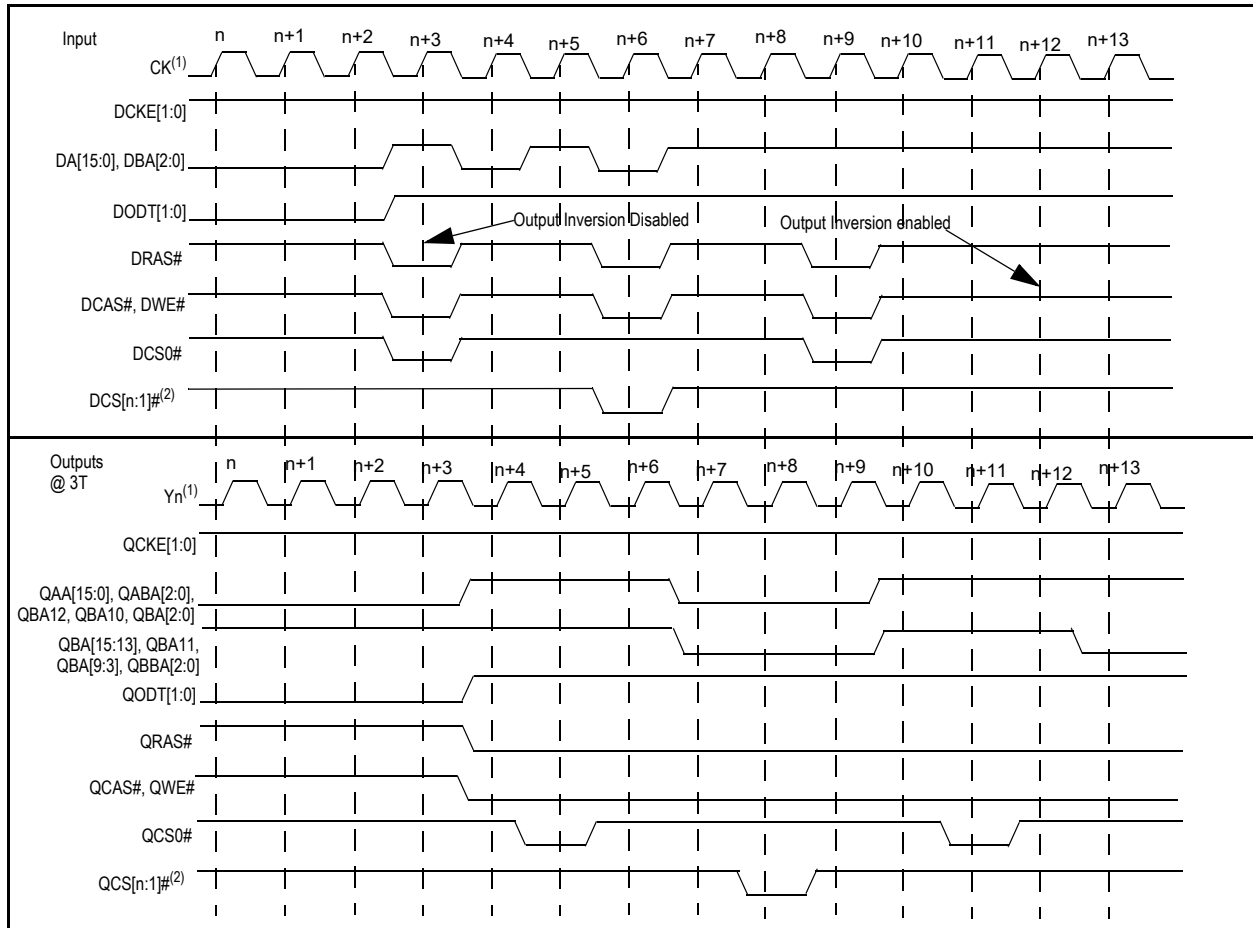


Figure 16 — 3T Timing During Multiple DRAM MRS Commands

NOTE 1 CK# and Yn# left out for better visibility

NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

2.2 Control Words

The SSTE32882 registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# in the QuadCS disabled mode. In the QuadCS enable mode, the simultaneous assertion of both DCS2# and DCS3# during normal operation, and the assertion of all four DCS[3:0]# inputs also result in control word access. However, assertion of any three DCS[3:0]# inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCs[n:0]# are set to HIGH during control word access.

The SSTE32882 allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be LOW and at least one DCKEn input must be HIGH for a valid access. During control word write, at least one DCKEn must be asserted. If register CKE power down feature is disabled, DCKEn input is a don't care (either HIGH or LOW). The inputs on DRAS#, DCAS#, DWE# and DODT[1:0] can be either HIGH or LOW and are ignored by the register during control word access. In all cases Address and command parity is checked during control word write operations. ERROUT# is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the SSTE32882 to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3...DA15, DBA0, DBA1, DRAS#, DCAS#, and DWE# are kept HIGH.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

2.3 Pinout Configuration

Package options include 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65 mm ball pitch, 11 x 20 grid, 8.0 mm x 13.5 mm. It is using the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing.

Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65 mm ball pitch.

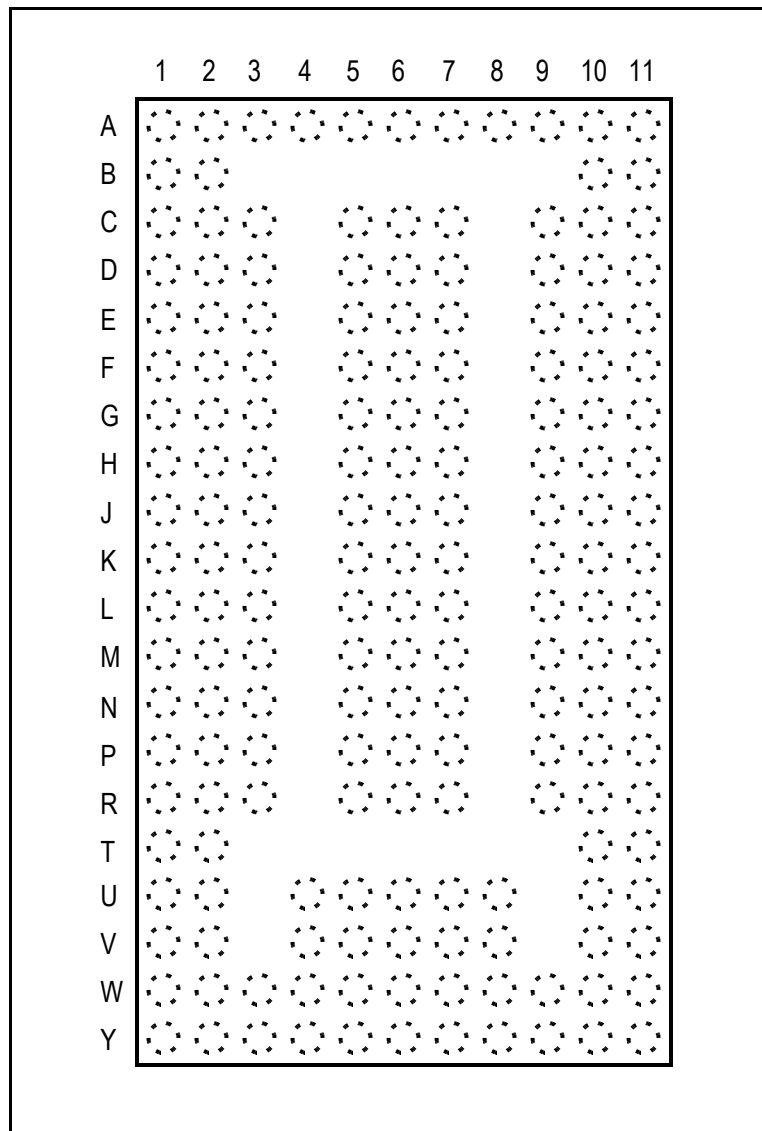


Figure 17 — Pinout Configuration

2.3.1 Pinout Top View for 176-ball TFBGA (Front Configuration, QuadCS Mode Disabled)

176-ball, 11 × 20 grid, TOP VIEW

Table 3 specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 3 — Ball Assignment; MIRROR=LOW, QCSSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSSEN#	VSS	RESET#	MIRROR	ERRROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAW#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	VDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1
NOTE 1 Pins A9 and W7 are reserved for future functions -- must not be connected on system											
NOTE 2 Pins Y2 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin											
NOTE 3 Blank space indicates no ball is populated at that gridpoint -- vias on the module may be located in these areas											