

JEDEC STANDARD

LRDIMM DDR3 Memory Buffer (MB) Version 1.0

JESD82-30.01

(Editorial Revision of JESD82-30, October 2014)

JANUARY 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by

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LRDIMM DDR3 Memory Buffer (MB)

(From JEDEC BoD Ballot JCB-11-85, formulated under the cognizance of the JC-40.4 Subcommittee on FBDIMM Support Components.)

1 Introduction

1.1 LRDIMM Memory Buffer Overview

The Load Reduced DIMM (LRDIMM) Memory Buffer (MB) supports DDR3 SDRAM main memory. The Memory Buffer allows buffering of memory traffic to support large memory capacities. Unlike DDR3 Register Buffer (SSTE32882), which only buffers Command, Address, Control and Clock, the LRDIMM Memory Buffer also buffers the Data (DQ) interface between the Memory Controller and the DRAM components. As the data electrical load is reduced for the Memory Controller interface, the system can now support more DIMMs per channel at a faster speed and higher density. All memory control for the DRAM resides in the host, including memory request initiation, timing, scrubbing, sparing, and power management. The Memory Buffer interface is responsible for memory requests to and from the local DIMM.

LRDIMM provides a high memory bandwidth, large capacity channel solution for DDR3 main memory systems. LRDIMM uses commodity DRAMs isolated from the channel behind the Memory Buffer on the DIMM. The supported capacity exceeds 144 devices per channel (depends on channel and individual system design) and total memory capacity scales with DRAM bit density.

1.2 Memory Buffer Functionality

1.2.1 Memory Buffer Key Features

- Acts as DRAM memory buffer for all read and write accesses addressed to the DIMM.
- Provides logic to support MEMBIST and Transparent Mode design for DRAM Test Support.
- Built-in MEMBIST engine to support back side memory voltage and timing training.
- Uses external supply VREFCA and VREFDQ as CA and DQ input buffer reference voltage. Support VREF WRITE margining capability for Host and DRAM interface. Supports internally generated VREFCA and VREFDQ for MB and DRAM CA and DQ input buffer reference voltage. Even though VREF level is internally generated by MB, it is still controlled by the host through configuration registers.
- Supports parity checking function to ensure the correct command and address signals are propagating correctly through the Memory Buffer.
- Supports an SMBus protocol interface for access to the MB configuration registers.
- Supports Control Word and Output Inversion features as used in SSTE32882.
- Supports built-in Temperature Sensor with T_{case} readout and three thermal trip point settings (accessed through MB configuration registers).
- Optional Logic Analyzer Interface (LAI) support for Failure Analysis (FA) and debug.

1.2.2 DDR SDRAM

DDR3 SDRAM support:

- Supports DDR3/DDR3L
- Supports 1Gb, 2Gb and 4Gb devices in x4 and x8 configurations
- 576 devices/channel (4 DIMMs/channel, 1, 2, 4 and 8 ranks/DIMM) - actual support varies by channel and individual system design
- 72-bit DDR3 SDRAM buffered memory interface

1.2.3 Byte Group Signal Mapping

The Memory Buffer (MB) HOST interface and DRAM interface DQ/MDQ and DQS/MDQS buses are divided into byte groups, according to Table 1 and Table 2.

Table 1 — DQ and DQS Mapping

		DQ								DQS			
		0	1	2	3	4	5	6	7				
Byte Group	0	DQ[0]	DQ[1]	DQ[2]	DQ[3]	DQ[4]	DQ[5]	DQ[6]	DQ[7]	DQS[0]_t	DQS[0]_c	DQS[9]_t	DQS[9]_c
	1	DQ[8]	DQ[9]	DQ[10]	DQ[11]	DQ[12]	DQ[13]	DQ[14]	DQ[15]	DQS[1]_t	DQS[1]_c	DQS[10]_t	DQS[10]_c
	2	DQ[16]	DQ[17]	DQ[18]	DQ[19]	DQ[20]	DQ[21]	DQ[22]	DQ[23]	DQS[2]_t	DQS[2]_c	DQS[11]_t	DQS[11]_c
	3	DQ[24]	DQ[25]	DQ[26]	DQ[27]	DQ[28]	DQ[29]	DQ[30]	DQ[31]	DQS[3]_t	DQS[3]_c	DQS[12]_t	DQS[12]_c
	4	DQ[32]	DQ[33]	DQ[34]	DQ[35]	DQ[36]	DQ[37]	DQ[38]	DQ[39]	DQS[4]_t	DQS[4]_c	DQS[13]_t	DQS[13]_c
	5	DQ[40]	DQ[41]	DQ[42]	DQ[43]	DQ[44]	DQ[45]	DQ[46]	DQ[47]	DQS[5]_t	DQS[5]_c	DQS[14]_t	DQS[14]_c
	6	DQ[48]	DQ[49]	DQ[50]	DQ[51]	DQ[52]	DQ[53]	DQ[54]	DQ[55]	DQS[6]_t	DQS[6]_c	DQS[15]_t	DQS[15]_c
	7	DQ[56]	DQ[57]	DQ[58]	DQ[59]	DQ[60]	DQ[61]	DQ[62]	DQ[63]	DQS[7]_t	DQS[7]_c	DQS[16]_t	DQS[16]_c
	8	DQ[64]	DQ[65]	DQ[66]	DQ[67]	DQ[68]	DQ[69]	DQ[70]	DQ[71]	DQS[8]_t	DQS[8]_c	DQS[17]_t	DQS[17]_c

Table 2 — MDQ and MDQS Mapping

		MDQ								MDQS			
		0	1	2	3	4	5	6	7				
Byte Group	0	MDQ[0]	MDQ[1]	MDQ[2]	MDQ[3]	MDQ[4]	MDQ[5]	MDQ[6]	MDQ[7]	MDQS[0]_t	MDQS[0]_c	MDQS[9]_t	MDQS[9]_c
	1	MDQ[8]	MDQ[9]	MDQ[10]	MDQ[11]	MDQ[12]	MDQ[13]	MDQ[14]	MDQ[15]	MDQS[1]_t	MDQS[1]_c	MDQS[10]_t	MDQS[10]_c
	2	MDQ[16]	MDQ[17]	MDQ[18]	MDQ[19]	MDQ[20]	MDQ[21]	MDQ[22]	MDQ[23]	MDQS[2]_t	MDQS[2]_c	MDQS[11]_t	MDQS[11]_c
	3	MDQ[24]	MDQ[25]	MDQ[26]	MDQ[27]	MDQ[28]	MDQ[29]	MDQ[30]	MDQ[31]	MDQS[3]_t	MDQS[3]_c	MDQS[12]_t	MDQS[12]_c
	4	MDQ[32]	MDQ[33]	MDQ[34]	MDQ[35]	MDQ[36]	MDQ[37]	MDQ[38]	MDQ[39]	MDQS[4]_t	MDQS[4]_c	MDQS[13]_t	MDQS[13]_c
	5	MDQ[40]	MDQ[41]	MDQ[42]	MDQ[43]	MDQ[44]	MDQ[45]	MDQ[46]	MDQ[47]	MDQS[5]_t	MDQS[5]_c	MDQS[14]_t	MDQS[14]_c
	6	MDQ[48]	MDQ[49]	MDQ[50]	MDQ[51]	MDQ[52]	MDQ[53]	MDQ[54]	MDQ[55]	MDQS[6]_t	MDQS[6]_c	MDQS[15]_t	MDQS[15]_c
	7	MDQ[56]	MDQ[57]	MDQ[58]	MDQ[59]	MDQ[60]	MDQ[61]	MDQ[62]	MDQ[63]	MDQS[7]_t	MDQS[7]_c	MDQS[16]_t	MDQS[16]_c
	8	MDQ[64]	MDQ[65]	MDQ[66]	MDQ[67]	MDQ[68]	MDQ[69]	MDQ[70]	MDQ[71]	MDQS[8]_t	MDQS[8]_c	MDQS[17]_t	MDQS[17]_c

1.3 LRDIMM DDR3 Memory Buffer Block Diagram

Figure 1 is a conceptual block diagram of the LRDIMM Memory Buffer's data flow and its interfaces.

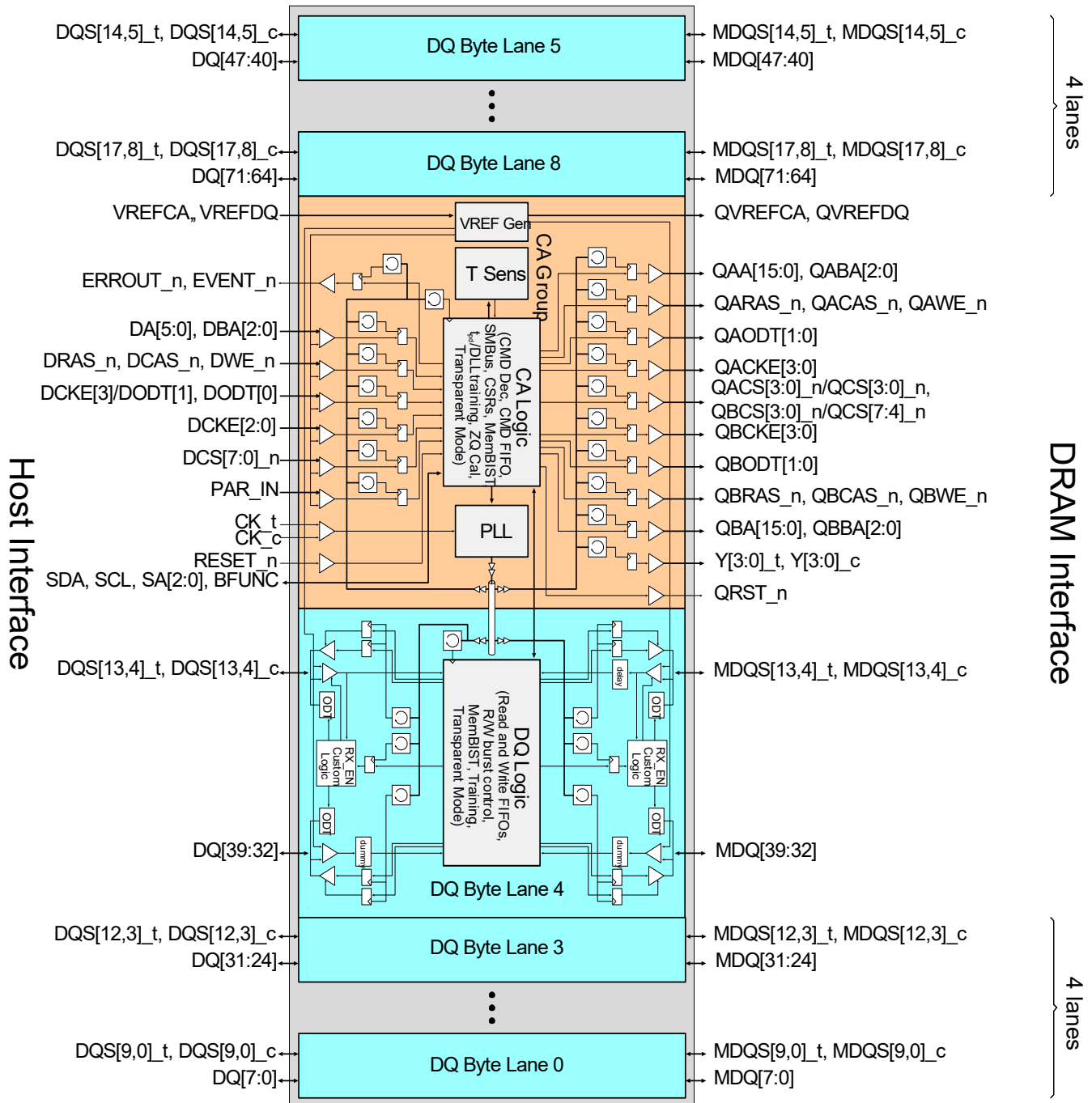


Figure 1 — LRDIMM DDR3 Memory Buffer Block Diagram

1.4 Interfaces

Figure 1 illustrates the LRDIMM Memory Buffer and all of its interfaces. They consist of one HOST interface, one DDR3 DRAM interface and an SMBus interface. The HOST interface connects the LRDIMM Memory Buffer to a host memory controller. The DDR3 DRAM interface supports direct connection to the DDR3 SDRAMs on a Load Reduced DIMM (LRDIMM)

1.4.1 HOST Interface

The LRDIMM Memory Buffer supports one HOST interface, which consists of Command, Address, Control, Clock, Data Strobe and Data. It also supports PAR_IN input as used in SSTE32882.

For the actual pin name and function description of the HOST Interface, please refer to Chapter 3 Pin Description.

1.4.2 DDR3 DRAM Interface

The DDR3 DRAM interface on the LRDIMM Memory Buffer supports direct connection to DDR3 SDRAMs. The DDR3 DRAM interface supports up to 8 ranks of eight banks with 16 row/column address signals, 64 data signals, and eight check-bit signals. There are two copies (A and B) of address and command signals to support DIMM routing and electrical requirements. Either a burst length of eight or a ‘chopped’ burst of four transfers are driven on the data and check-bit lines.

For the actual pin name and function description of the DRAM Interface, please refer to Chapter 3 Pin Description.

1.4.3 SMBus Target Interface

The LRDIMM Memory Buffer supports an SMBus interface to allow system access to configuration registers and temperature sensor. The Memory Buffer will never be a controller on the SMBus, only a Target. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to Memory Buffer may be required to boot a system. It is also required for system diagnostic and debug support.

More information is available in this standard, see clause 13, SMBus.

1.5 References

This Standard is consistent with the following documents:

- JEDEC JESD79-3D, *DDR3 SDRAM Standard*, [1]
- JEDEC JESD82-29, *Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3/DDR3L/DDR3U RDIMM 1.5 V/1.35 V/1.25 V Applications* [2]
- JEDEC JESD21C, *JEDEC Configurations for Solid State Memories* (DDR3 SDRAM Registered DIMM Design Specification), [3]
- *System Management Bus (SMBus) Specification Version 2.0*, published by www.smbus.org [4]
- JEDEC JESD8-11, *Addendum No. 11 to JESD8 - 1.5 V +/- 0.1 V (Normal Range) and 0.9 V - 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits* [5]

1.6 Glossary

Term	Definition
MB	Memory Buffer
CA	Command/Address; RAS#, CAS#, WE#, BA[2:0], and A[15:0] signals to the DRAM, or associated I/O pins and wires
CSR	Control and Status Register
DDR	Double Data Rate: a description of contemporary synchronous DRAM characterized by data communications at a rate of two bits per clock cycle per wire
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an ADDR/CNTRL channel
DLL	Delay-Locked Loop
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
Host	Memory controller agent on a DDR channel
IBT	Input Bus Termination; termination for input-only memory buffer pins, specifically command/address and control signal pins
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, <i>DDR SDRAM Specification</i>
LRDIMM	Load Reduced DIMM
LA	Logic Analyzer
LAI	Logic Analyzer Interface
MRS	Mode Register Set; mode control registers in DDR SDRAM devices
ODT	On-Die Termination; termination for input-output memory buffer pins, specifically data and strobe signal pins
PLL	Phase Locked Loop
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one, two, four or eight physical sets of memory, called ranks.
RAS	When not used in reference to a SDRAM signal, RAS is the short form for “Reliability, Availability, Serviceability”
RDIMM	Registered DIMM; contemporary buffered DIMM technology using a registering clock driver to buffer clock, command/address, and control signals to the DRAM devices
SDRAM	Synchronous Dynamic Random Access Memory
SI	Signal Integrity
SMBus	System Management Bus. Controlled by a system management controller to read and write configuration registers. Limited to 100 kHz.
SSC	Spread Spectrum Clocking; a technique for reducing EMI in a clocked digital system by frequency modulating the clock, reducing the peak radiated energy by spreading radiated energy over a frequency band

Term	Definition
SSO	Simultaneously Switching Outputs
Transparent Mode	A mode to provide “pass through” access from ATE tester through the DDR3 Memory Buffer to the SDRAM on LRDIMM
UI	Unit Interval: average time interval between voltage transitions of a signal
V_{SS}	Ground (0V)
V_{DDQ}	I/O buffer voltage for DDR3/DDR3L buffers. Nominally 1.5/1.35V

2 Ballout and Package Information

2.1 588-Ball FBGA (20x38 Array, 25.2x13.5 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) Pin configuration

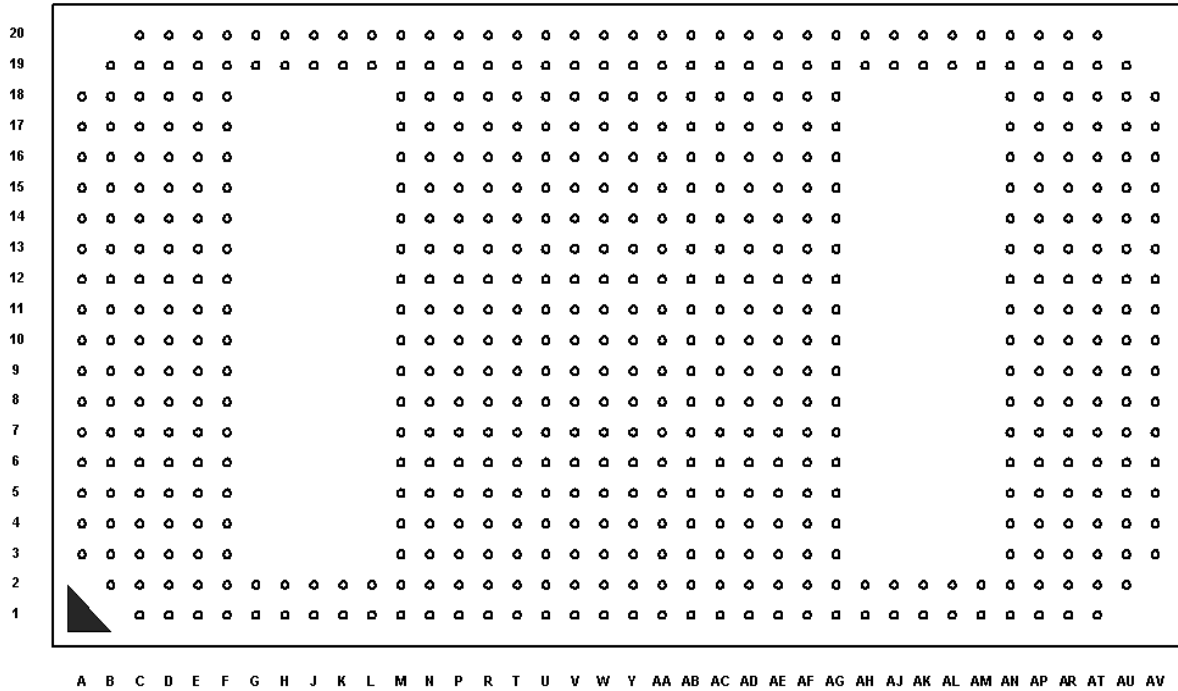


Figure 2 — Pinout Configuration

2.2 Pin Assignments for the LR-DIMM DDR3 Memory Buffer (MB)

**Table 3 — 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A)
(Transparent, Top View) - Left Side**

20	NB	NB	VSS	DQ7	DQS9_t	DQ2	DQ3	VDD	DQ68	DQS17_t	DQ70	VSS	DQ66	VDD	Y3_c	Y3_t	Y1_t	Y1_c	Y2_c
19	NB	VSS	DQ4	DQ6	DQS9_c	VSS	DQ1	VSS	DQ69	DQS17_c	DQ71	VSS	DQ67	VDD	VSS	PVDD	VSS	PVDD	VSS
18	VSS	VDD	VSS	DQ5	DQS0_c	DQ0	NB	NB	NB	NB	NB	DQS8_t	DQ64	VSS	MDQ68	MDQS17_t	MDQ70	MDQ64	MDQS8_c
17	MDQ5	MDQ4	MDQ0	VSS	DQS0_t	VSS	NB	NB	NB	NB	NB	DQS8_c	DQ65	VSS	MDQ69	MDQS17_c	MDQ71	MDQ65	MDQS8_t
16	MDQS9_t	MDQS9_c	MDQS0_c	MDQS0_t	VDD	QACAS_n	NB	NB	NB	NB	NB	VDD	VDD	VDD	VSS	VDD	VSS	VDD	VSS
15	MDQ6	MDQ7	MDQ2	MDQ1	VDD	QARAS_n	NB	NB	NB	NB	NB	RFU	RFU	VSS	VDD	VSS	VDD	VSS	VDD
14	VSS	VSS	VSS	MDQ3	VDD	QAA15	NB	NB	NB	NB	NB	VDD	VDD	RFU	VSS	VDD	VSS	VDD	VSS
13	DQS1_t	DQS1_c	VSS	VDD	QAA10	QACKE1	NB	NB	NB	NB	NB	QAWEN	VDD	QAODT1	VDD	VSS	VDD	VSS	VDD
12	VDD	VSS	DQ8	VDD	QACKE0	QAA12	NB	NB	NB	NB	NB	QABA0	QABA2	QAODT0	VSS	RESET_n	VSS	VDD	VSS
11	DQ11	DQ10	DQ9	VDD	QABA1	QACKE2	NB	NB	NB	NB	NB	QAA0	VDD	VSS	VDD	DCKE2	VDD	DA1	VDD
10	DQ15	DQ14	DQ13	VDD	QACKE3	QAA4	NB	NB	NB	NB	NB	QAA3	QACS0_n/QCS0_n	QACS1_n/QCS1_n	QRST_n	DCKE1	DA12	DA6	DA4
9	VDD	VSS	DQ12	VDD	QAA1	QAA6	NB	NB	NB	NB	NB	QACS3_n/QCS3_n	QACS2_n/QCS2_n	VDD	DCKE0	DBA2	DA11	DA3	DA5
8	DQS10_t	DQS10_c	VSS	VDD	VDD	QAA11	NB	NB	NB	NB	NB	QAA5	QAA2	VDD	DA15	DA14	DA9	DA8	DA7
7	VSS	VSS	VSS	MDQ9	VDD	QAA8	NB	NB	NB	NB	NB	QAA13	QAA9	VDD	VDD	ERROUT_n	VDD	VDD	VDD
6	MDQ12	MDQ13	MDQ8	MDQ11	VDD	QAA14	NB	NB	NB	NB	NB	QAA7	VDD	DQ24	DQ25	VSS	MDQ29	MDQS12_t	VSS
5	MDQS10_t	MDQS10_c	MDQS1_c	MDQS1_t	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	DQS3_t	DQS3_c	VSS	MDQ30	MDQS12_c	MDQ28
4	MDQ14	MDQ15	MDQ10	VSS	DQS2_t	DQ16	NB	NB	NB	NB	NB	MDQS2_c	VSS	DQ26	DQ27	VSS	MDQ31	MDQS3_c	VSS
3	VSS	VDD	VSS	DQ19	DQS2_c	DQ17	NB	NB	NB	NB	NB	MDQS2_t	VSS	VDD	DQ28	DQ29	VSS	MDQS3_t	MDQ24
2	NB	VSS	DQ18	DQ22	DQS11_c	DQ20	VSS	MDQ20	MDQS11_c	MDQ22	VSS	MDQ16	MDQ18	VSS	DQS12_t	DQS12_c	VSS	MDQ25	VSS
1	NB	NB	VSS	DQ23	DQS11_t	DQ21	VSS	MDQ21	MDQS11_t	MDQ23	VSS	MDQ17	MDQ19	VSS	DQ30	DQ31	VSS	MDQ26	MDQ27
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

Table 4 — 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) (Transparent, Top View) - Right Side

Y2_t	Y0_t	Y0_c	VDD	ZQ	SCL	SA[2]	SA[0]	QVREF CA	VDD	QVREF DQ	VDD	DQ59	DQ58	DQS7_t	DQ63	VSS	NB	NB	20
PVDD	VSS	PVDD	VSS	ZQVSS	SDA	VCCSP D	SA[1]	VREFC A	VSS	VREFD Q	VSS	DQ57	VSS	DQS7_c	DQ62	DQ60	VSS	NB	19
MDQ6_6	VSS	CK_t	CK_c	VSS	VDD	EVENT _n	BFUNC	NB	NB	NB	NB	NB	DQ56	DQS16_c	DQ61	VSS	VDD	VSS	18
MDQ6_7	TEST[0] _j	AVSS	AVDD	AOUT	TEST[2] _j	VSS	VDD	NB	NB	NB	NB	NB	VSS	DQS16_t	VSS	MDQ58	MDQ63	MDQ62	17
VDD	TEST[1] _j	VDD	VSS	VDD	VSS	VDD	VSS	NB	NB	NB	NB	NB	QBWE _n	VDD	MDQS7_t	MDQS7_c	MDQS16_c	MDQS16_t	16
VSS	VDD	VSS	VDD	VSS	VDD	QBCAS _n	QBRAS _n	NB	NB	NB	NB	NB	QBBA0	VDD	MDQ59	MDQ57	MDQ61	MDQ60	15
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDD	NB	NB	NB	NB	NB	QBA0	VDD	MDQ56	VSS	VSS	VSS	14
VSS	VDD	VSS	VDD	VSS	QBCKE 1	QBA10	QBA15	NB	NB	NB	NB	NB	QBA3	QBODT 1	VDD	VSS	DQS6_c	DQS6_t	13
VDD	VSS	VDD	VSS	VDD	QBCKE 0	VDD	VDD	NB	NB	NB	NB	NB	QBA2	QBBA2	VDD	DQ48	VSS	VDD	12
VSS	DCS2_n	DCS4_n	DCS3_n	VSS	QBCKE 3	QBBA1	QBA12	NB	NB	NB	NB	NB	QBA5	QBODT 0	VDD	DQ49	DQ50	DQ51	11
DA2	DA13	DCS0_n	DCS5_n	DBA1	VDD	QBCKE 2	QBA4	NB	NB	NB	NB	NB	QBCS1_n/ QCS5_n	QBCS0_n/ QCS4_n	VDD	DQ53	DQ54	DQ55	10
PAR_I _N	DODT0	DA0	DBA0	DODT1/ DCKE3	VSS	QBA1	QBA6	NB	NB	NB	NB	NB	QBCS3_n/ QCS7_n	QBCS2_n/ QCS6_n	VDD	DQ52	VSS	VDD	9
DCS1_n	DCAS_n	DRAS_n	DA10	DCS6_n	DCS7_n	VDD	VDD	NB	NB	NB	NB	NB	QBA9	VDD	VDD	VSS	DQS15_c	DQS15_t	8
VDD	VDD	VDD	DWE_n	VDD	VDD	QBA11	QBA8	NB	NB	NB	NB	NB	QBA13	VDD	MDQ51	VSS	VSS	VSS	7
MDQ3_6	MDQS13_t	MDQ37	VSS	DQ32	DQ33	VDD	QBA14	NB	NB	NB	NB	NB	QBA7	VDD	MDQ49	MDQ50	MDQ55	MDQ54	6
VSS	MDQS13_c	MDQ38	VSS	DQS4_t	DQS4_c	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	MDQS6_t	MDQS6_c	MDQS15_c	MDQS15_t	5
MDQ3_2	MDQS4_c	MDQ39	VSS	DQ34	DQ35	VSS	MDQS5_c	NB	NB	NB	NB	NB	DQ40	DQS5_t	VSS	MDQ48	MDQ53	MDQ52	4
VSS	MDQS4_t	VSS	DQ36	DQ37	VDD	VSS	MDQS5_t	NB	NB	NB	NB	NB	DQ41	DQS5_c	DQ45	VSS	VDD	VSS	3
MDQ3_3	MDQ34	VSS	DQS13_t	DQS13_c	VSS	MDQ40	MDQ43	VSS	MDQ44	MDQS14_t	MDQ47	VSS	DQ42	DQS14_c	DQ46	DQ44	VSS	NB	2
VSS	MDQ35	VSS	DQ38	DQ39	VSS	MDQ41	MDQ42	VSS	MDQ45	MDQS14_c	MDQ46	VSS	DQ43	DQS14_t	DQ47	VSS	NB	NB	1
Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV	

Table 5 — Memory Buffer Signals By Ball Number (Sheet 1 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	NB	B1	NB	C1	VSS
A2	NB	B2	VSS	C2	DQ18
A3	VSS	B3	VDD	C3	VSS
A4	MDQ14	B4	MDQ15	C4	MDQ10
A5	MDQS10_t	B5	MDQS10_c	C5	MDQS1_c
A6	MDQ12	B6	MDQ13	C6	MDQ8
A7	VSS	B7	VSS	C7	VSS
A8	DQS10_t	B8	DQS10_c	C8	VSS
A9	VDD	B9	VSS	C9	DQ12
A10	DQ15	B10	DQ14	C10	DQ13
A11	DQ11	B11	DQ10	C11	DQ9
A12	VDD	B12	VSS	C12	DQ8
A13	DQS1_t	B13	DQS1_c	C13	VSS
A14	VSS	B14	VSS	C14	VSS
A15	MDQ6	B15	MDQ7	C15	MDQ2
A16	MDQS9_t	B16	MDQS9_c	C16	MDQS0_c
A17	MDQ5	B17	MDQ4	C17	MDQ0
A18	VSS	B18	VDD	C18	VSS
A19	NB	B19	VSS	C19	DQ4
A20	NB	B20	NB	C20	VSS
D1	DQ23	E1	DQS11_t	F1	DQ21
D2	DQ22	E2	DQS11_c	F2	DQ20
D3	DQ19	E3	DQS2_c	F3	DQ17
D4	VSS	E4	DQS2_t	F4	DQ16
D5	MDQS1_t	E5	VSS	F5	VDD
D6	MDQ11	E6	VDD	F6	QAA14
D7	MDQ9	E7	VDD	F7	QAA8
D8	VDD	E8	VDD	F8	QAA11
D9	VDD	E9	QAA1	F9	QAA6
D10	VDD	E10	QACKE3	F10	QAA4
D11	VDD	E11	QABA1	F11	QACKE2
D12	VDD	E12	QACKE0	F12	QAA12
D13	VDD	E13	QAA10	F13	QACKE1
D14	MDQ3	E14	VDD	F14	QAA15
D15	MDQ1	E15	VDD	F15	QARAS_n
D16	MDQS0_t	E16	VDD	F16	QACAS_n
D17	VSS	E17	DQS0_t	F17	VSS
D18	DQ5	E18	DQS0_c	F18	DQ0
D19	DQ6	E19	DQS9_c	F19	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 2 of 7)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
D20	DQ7		E20	DQS9_t		F20	DQ2
G1	VSS		H1	MDQ21		J1	MDQS11_t
G2	VSS		H2	MDQ20		J2	MDQS11_c
G3	NB		H3	NB		J3	NB
G4	NB		H4	NB		J4	NB
G5	NB		H5	NB		J5	NB
G6	NB		H6	NB		J6	NB
G7	NB		H7	NB		J7	NB
G8	NB		H8	NB		J8	NB
G9	NB		H9	NB		J9	NB
G10	NB		H10	NB		J10	NB
G11	NB		H11	NB		J11	NB
G12	NB		H12	NB		J12	NB
G13	NB		H13	NB		J13	NB
G14	NB		H14	NB		J14	NB
G15	NB		H15	NB		J15	NB
G16	NB		H16	NB		J16	NB
G17	NB		H17	NB		J17	NB
G18	NB		H18	NB		J18	NB
G19	DQ1		H19	VSS		J19	DQ69
G20	DQ3		H20	VDD		J20	DQ68
K1	MDQ23		L1	VSS		M1	MDQ17
K2	MDQ22		L2	VSS		M2	MDQ16
K3	NB		L3	NB		M3	MDQS2_t
K4	NB		L4	NB		M4	MDQS2_c
K5	NB		L5	NB		M5	VDD
K6	NB		L6	NB		M6	QAA7
K7	NB		L7	NB		M7	QAA13
K8	NB		L8	NB		M8	QAA5
K9	NB		L9	NB		M9	QACS3_n/ QCS3_n
K10	NB		L10	NB		M10	QAA3
K11	NB		L11	NB		M11	QAA0
K12	NB		L12	NB		M12	QABA0
K13	NB		L13	NB		M13	QAWEn
K14	NB		L14	NB		M14	VDD
K15	NB		L15	NB		M15	RFU
K16	NB		L16	NB		M16	VDD
K17	NB		L17	NB		M17	DQS8_c
K18	NB		L18	NB		M18	DQS8_t
K19	DQS17_c		L19	DQ71		M19	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 3 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
K20	DQS17_t	L20	DQ70	M20	VSS
N1	MDQ19	P1	VSS	R1	DQ30
N2	MDQ18	P2	VSS	R2	DQS12_t
N3	VSS	P3	VDD	R3	DQ28
N4	VSS	P4	DQ26	R4	DQ27
N5	VSS	P5	DQS3_t	R5	DQS3_c
N6	VDD	P6	DQ24	R6	DQ25
N7	QAA9	P7	VDD	R7	VDD
N8	QAA2	P8	VDD	R8	DA15
N9	QACS2_n/ QCS2_n	P9	VDD	R9	DCKE0
N10	QACS0_n/ QCS0_n	P10	QACS1_n/ QCS1_n	R10	QRST_n
N11	VDD	P11	VSS	R11	VDD
N12	QABA2	P12	QAODT0	R12	VSS
N13	VDD	P13	QAODT1	R13	VDD
N14	VDD	P14	RFU	R14	VSS
N15	RFU	P15	VSS	R15	VDD
N16	VDD	P16	VDD	R16	VSS
N17	DQ65	P17	VSS	R17	MDQ69
N18	DQ64	P18	VSS	R18	MDQ68
N19	DQ67	P19	VDD	R19	VSS
N20	DQ66	P20	VDD	R20	Y3_c
T1	DQ31	U1	VSS	V1	MDQ26
T2	DQS12_c	U2	VSS	V2	MDQ25
T3	DQ29	U3	VSS	V3	MDQS3_t
T4	VSS	U4	MDQ31	V4	MDQS3_c
T5	VSS	U5	MDQ30	V5	MDQS12_c
T6	VSS	U6	MDQ29	V6	MDQS12_t
T7	ERROUT_n	U7	VDD	V7	VDD
T8	DA14	U8	DA9	V8	DA8
T9	DBA2	U9	DA11	V9	DA3
T10	DCKE1	U10	DA12	V10	DA6
T11	DCKE2	U11	VDD	V11	DA1
T12	RESET_n	U12	VSS	V12	VDD
T13	VSS	U13	VDD	V13	VSS
T14	VDD	U14	VSS	V14	VDD
T15	VSS	U15	VDD	V15	VSS
T16	VDD	U16	VSS	V16	VDD
T17	MDQS17_c	U17	MDQ71	V17	MDQ65
T18	MDQS17_t	U18	MDQ70	V18	MDQ64

Table 5 — Memory Buffer Signals By Ball Number (Sheet 4 of 7)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
T19	PVDD		U19	VSS		V19	PVDD
T20	Y3_t		U20	Y1_t		V20	Y1_c
W1	MDQ27		Y1	VSS		AA1	MDQ35
W2	VSS		Y2	MDQ33		AA2	MDQ34
W3	MDQ24		Y3	VSS		AA3	MDQS4_t
W4	VSS		Y4	MDQ32		AA4	MDQS4_c
W5	MDQ28		Y5	VSS		AA5	MDQS13_c
W6	VSS		Y6	MDQ36		AA6	MDQS13_t
W7	VDD		Y7	VDD		AA7	VDD
W8	DA7		Y8	DCS1_n		AA8	DCAS_n
W9	DA5		Y9	PAR_IN		AA9	DODT0
W10	DA4		Y10	DA2		AA10	DA13
W11	VDD		Y11	VSS		AA11	DCS2_n
W12	VSS		Y12	VDD		AA12	VSS
W13	VDD		Y13	VSS		AA13	VDD
W14	VSS		Y14	VDD		AA14	VSS
W15	VDD		Y15	VSS		AA15	VDD
W16	VSS		Y16	VDD		AA16	TEST[1]
W17	MDQS8_t		Y17	MDQ67		AA17	TEST[0]
W18	MDQS8_c		Y18	MDQ66		AA18	VSS
W19	VSS		Y19	PVDD		AA19	VSS
W20	Y2_c		Y20	Y2_t		AA20	Y0_t
AB1	VSS		AC1	DQ38		AD1	DQ39
AB2	VSS		AC2	DQS13_t		AD2	DQS13_c
AB3	VSS		AC3	DQ36		AD3	DQ37
AB4	MDQ39		AC4	VSS		AD4	DQ34
AB5	MDQ38		AC5	VSS		AD5	DQS4_t
AB6	MDQ37		AC6	VSS		AD6	DQ32
AB7	VDD		AC7	DWE_n		AD7	VDD
AB8	DRAS_n		AC8	DA10		AD8	DCS6_n
AB9	DA0		AC9	DBA0		AD9	DODT1/ DCKE3
AB10	DCS0_n		AC10	DCS5_n		AD10	DBA1
AB11	DCS4_n		AC11	DCS3_n		AD11	VSS
AB12	VDD		AC12	VSS		AD12	VDD
AB13	VSS		AC13	VDD		AD13	VSS
AB14	VDD		AC14	VSS		AD14	VDD
AB15	VSS		AC15	VDD		AD15	VSS
AB16	VDD		AC16	VSS		AD16	VDD
AB17	AVSS		AC17	AVDD		AD17	AOUT
AB18	CK_t		AC18	CK_c		AD18	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 5 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
AB19	PVDD	AC19	VSS	AD19	ZQVSS
AB20	Y0_c	AC20	VDD	AD20	ZQ
AE1	VSS	AF1	MDQ41	AG1	MDQ42
AE2	VSS	AF2	MDQ40	AG2	MDQ43
AE3	VDD	AF3	VSS	AG3	MDQS5_t
AE4	DQ35	AF4	VSS	AG4	MDQS5_c
AE5	DQS4_c	AF5	VSS	AG5	VDD
AE6	DQ33	AF6	VDD	AG6	QBA14
AE7	VDD	AF7	QBA11	AG7	QBA8
AE8	DCS7_n	AF8	VDD	AG8	VDD
AE9	VSS	AF9	QBA1	AG9	QBA6
AE10	VDD	AF10	QBCKE2	AG10	QBA4
AE11	QBCKE3	AF11	QBBA1	AG11	QBA12
AE12	QBCKE0	AF12	VDD	AG12	VDD
AE13	QBCKE1	AF13	QBA10	AG13	QBA15
AE14	VSS	AF14	VDD	AG14	VDD
AE15	VDD	AF15	QBCAS_n	AG15	QBRAS_n
AE16	VSS	AF16	VDD	AG16	VSS
AE17	TEST[2]	AF17	VSS	AG17	VDD
AE18	VDD	AF18	EVENT_n	AG18	BFUNC
AE19	SDA	AF19	VCCSPD	AG19	SA[1]
AE20	SCL	AF20	SA[2]	AG20	SA[0]
AH1	VSS	AJ1	MDQ45	AK1	MDQS14_c
AH2	VSS	AJ2	MDQ44	AK2	MDQS14_t
AH3	NB	AJ3	NB	AK3	NB
AH4	NB	AJ4	NB	AK4	NB
AH5	NB	AJ5	NB	AK5	NB
AH6	NB	AJ6	NB	AK6	NB
AH7	NB	AJ7	NB	AK7	NB
AH8	NB	AJ8	NB	AK8	NB
AH9	NB	AJ9	NB	AK9	NB
AH10	NB	AJ10	NB	AK10	NB
AH11	NB	AJ11	NB	AK11	NB
AH12	NB	AJ12	NB	AK12	NB
AH13	NB	AJ13	NB	AK13	NB
AH14	NB	AJ14	NB	AK14	NB
AH15	NB	AJ15	NB	AK15	NB
AH16	NB	AJ16	NB	AK16	NB
AH17	NB	AJ17	NB	AK17	NB
AH18	NB	AJ18	NB	AK18	NB

Table 5 — Memory Buffer Signals By Ball Number (Sheet 6 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
AH19	VREFCA	AJ19	VSS	AK19	VREFDQ
AH20	QVREFCA	AJ20	VDD	AK20	QVREFDQ
AL1	MDQ46	AM1	VSS	AN1	DQ43
AL2	MDQ47	AM2	VSS	AN2	DQ42
AL3	NB	AM3	NB	AN3	DQ41
AL4	NB	AM4	NB	AN4	DQ40
AL5	NB	AM5	NB	AN5	VDD
AL6	NB	AM6	NB	AN6	QBA7
AL7	NB	AM7	NB	AN7	QBA13
AL8	NB	AM8	NB	AN8	QBA9
AL9	NB	AM9	NB	AN9	QBCS3_n/ QCS7_n
AL10	NB	AM10	NB	AN10	QBCS1_n/ QCS5_n
AL11	NB	AM11	NB	AN11	QBA5
AL12	NB	AM12	NB	AN12	QBA2
AL13	NB	AM13	NB	AN13	QBA3
AL14	NB	AM14	NB	AN14	QBA0
AL15	NB	AM15	NB	AN15	QBBA0
AL16	NB	AM16	NB	AN16	QBWE_n
AL17	NB	AM17	NB	AN17	VSS
AL18	NB	AM18	NB	AN18	DQ56
AL19	VSS	AM19	DQ57	AN19	VSS
AL20	VDD	AM20	DQ59	AN20	DQ58
AP1	DQS14_t	AR1	DQ47	AT1	VSS
AP2	DQS14_c	AR2	DQ46	AT2	DQ44
AP3	DQS5_c	AR3	DQ45	AT3	VSS
AP4	DQS5_t	AR4	VSS	AT4	MDQ48
AP5	VSS	AR5	MDQS6_t	AT5	MDQS6_c
AP6	VDD	AR6	MDQ49	AT6	MDQ50
AP7	VDD	AR7	MDQ51	AT7	VSS
AP8	VDD	AR8	VDD	AT8	VSS
AP9	QBCS2_n/ QCS6_n	AR9	VDD	AT9	DQ52
AP10	QBCS0_n/ QCS4_n	AR10	VDD	AT10	DQ53
AP11	QBODT0	AR11	VDD	AT11	DQ49
AP12	QBBA2	AR12	VDD	AT12	DQ48
AP13	QBODT1	AR13	VDD	AT13	VSS
AP14	VDD	AR14	MDQ56	AT14	VSS
AP15	VDD	AR15	MDQ59	AT15	MDQ57
AP16	VDD	AR16	MDQS7_t	AT16	MDQS7_c

Table 5 — Memory Buffer Signals By Ball Number (Sheet 7 of 7)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
AP17	DQS16_t		AR17	VSS		AT17	MDQ58
AP18	DQS16_c		AR18	DQ61		AT18	VSS
AP19	DQS7_c		AR19	DQ62		AT19	DQ60
AP20	DQS7_t		AR20	DQ63		AT20	VSS
AU1	NB		AV1	NB			
AU2	VSS		AV2	NB			
AU3	VDD		AV3	VSS			
AU4	MDQ53		AV4	MDQ52			
AU5	MDQS15_c		AV5	MDQS15_t			
AU6	MDQ55		AV6	MDQ54			
AU7	VSS		AV7	VSS			
AU8	DQS15_c		AV8	DQS15_t			
AU9	VSS		AV9	VDD			
AU10	DQ54		AV10	DQ55			
AU11	DQ50		AV11	DQ51			
AU12	VSS		AV12	VDD			
AU13	DQS6_c		AV13	DQS6_t			
AU14	VSS		AV14	VSS			
AU15	MDQ61		AV15	MDQ60			
AU16	MDQS16_c		AV16	MDQS16_t			
AU17	MDQ63		AV17	MDQ62			
AU18	VDD		AV18	VSS			
AU19	VSS		AV19	NB			
AU20	NB		AV20	NB			

2.3 Package Information

Refer to Registered Outline MO-301A published by JC-11 committee for LR-DIMM DDR3 MB package info.

3 Pin Descriptions

3.1 Pin Description

Table 6 — Memory Buffer Signal Types

Buffer Direction	Description
I	Input signal
O	Output signal
A	Analog
I/O	Bidirectional (input/output) signal
NC	No Connect

Table 7 — Pin Description (Sheet 1 of 3)

Signal	Type	Count	Description
Host Interface			
DQ[71:64]	I/O	8	Check bits (re: DQ for ECC DRAM)
DQ[63:0]	I/O	64	Data
DQS[17:0]_t	I/O	18	Data Strobe: DDR3 data and check-bit strobe.
DQS[17:0]_c	I/O	18	Data Strobe Complement: DDR3 data and check-bit strobe complements.
DA[15:0]	I	16	Address: Used for providing multiplexed row and column address to SDRAM.
DBA[2:0]	I	3	Bank Active: Used to select the bank within a rank.
DRAS_n	I	1	Row Address Strobe: Used with DCS_n, DCAS_n, and DWE_n to specify the SDRAM command.
DCAS_n	I	1	Column Address Strobe: Used with DCS_n, DRAS_n, and DWE_n to specify the SDRAM command.
DWE_n	I	1	Write Enable: Used with DCS_n, DCAS_n, and DRAS_n to specify the SDRAM command.
DCS[7:0]_n	I	8	Chip Select: Used with DCAS_n, DRAS_n, and DWE_n to specify the SDRAM command. These signals are used for selecting one of eight SDRAM ranks. DCS0_n is used to select the first rank, DCS1_n is used to select the second rank..., and DCS7_n is used to select the 8 th rank
DCKE[2:0]	I	3	Clock Enable
DCKE[3]/DODT[1]	I	1	Clock Enable or On-Die-Termination (selection controlled by Control Word F0RC6)
DODT[0]	I	1	On-Die-Termination: Dynamic ODT enables for each DIMM on the channel
CK_t/CK_c	I	2	Differential clock input

Table 7 — Pin Description (Sheet 2 of 3)

Signal	Type	Count	Description
PAR_IN	I	1	Parity Input
ERROUT_n	O	1	Parity error output: An Open Drain output. When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs
DRAM Interface			
MDQ[71:64]	I/O	8	Check bits (re: DQ for ECC DRAM)
MDQ[63:0]	I/O	64	Data
MDQS[17:0]_t	I/O	18	DRAM Data Strobe: DDR3 data and check-bit strobe.
MDQS[17:0]_c	I/O	18	DRAM Data Strobe Complement: DDR3 data and check-bit strobe complements.
QAA[15:0], QBA[15:0]	O	32	Address (A, B Copy): Used for providing multiplexed row and column address to SDRAM.
QABA[2:0], QBBA[2:0]	O	6	Bank Active (A, B Copy): Used to select the bank within a rank.
QARAS_n, QBRAS_n	O	2	Row Address Strobe (A, B Copy): Used with CS_n, CAS_n, and WE_n to specify the SDRAM command.
QACAS_n, QBCAS_n	O	2	Column Address Strobe (A, B Copy): Used with CS_n, RAS_n, and WE_n to specify the SDRAM command.
QAWEn, QBWE_n	O	2	Write Enable (A, B Copy): Used with DCS_n, DCAS_n, and DRAS_n to specify the SDRAM command.
QACS[3:0]_n/ QCS[3:0]_n	O	4	Chip select (A copy)/(Single copy) lower 4 chip-selects for 8-rank case: Used with CAS_n, RAS_n, and WE_n to specify the SDRAM command. These signals are used for selecting one of eight physical ranks. CS0_n is used to select the 1st rank, CS1_n is used to select the 2nd rank, CS2_n is used to select the 3rd rank, and CS3_n is used to select the 4th rank.
QBCS[3:0]_n/ QCS[7:4]_n	O	4	Chip select (B copy)/(Single copy) upper 4 chip-selects for 8-rank case: Used with CAS_n, RAS_n, and WE_n to specify the SDRAM command. These signals are used for selecting one of eight physical ranks. CS0_n is used to select the 1st rank (or 5th rank in the 8R case), CS1_n is used to select the 2nd rank (or 6th rank in the 8R case), CS2_n is used to select the 3rd rank (or 7th rank in the 8R case), and CS3_n is used to select the 4th rank (or 8th rank in the 8R case).
QACKE[3:0], QBCKE[3:0]	O	8	Clock Enable (A, B Copy)
QAODT[1:0], QBODT[1:0]	O	4	DRAM On-Die-Termination Control (A, B Copy)
Y[3:0]_t/Y[3:0]_c	O	8	Differential DRAM clock.
System Management			
SCL	I/O	1	SMBus Clock
SDA	I/O	1	SMBus Address/Data
SA[2:0]	I	3	DIMM Select ID (SMBus device address)
EVENT_n	O	1	Temperature trip point event pin
Reset			

Table 7 — Pin Description (Sheet 3 of 3)

Signal	Type	Count	Description
RESET_n	I	1	Asynchronous Power Good Reset
QRST_n	O	1	Buffered Reset to DRAM (if used on DIMM)
Miscellaneous Test			
TEST[2:0]	NC	3	Pin for debug and test. Must be floated on DIMM.
AOUT	NC	1	Test output pin. Must be floated on DIMM
ZQ	A	1	ZQ Calibration resistor
ZQVSS	A	1	ZQ Calibration resistor ground reference
CA and DQ Reference Supplies			
VREFCA	A	1	CA receiver reference voltage input from Host
QVREFCA	A	1	CA receiver reference voltage output to DRAM
VREFDQ	A	1	DQ receiver reference voltage input from Host
QVREFDQ	A	1	DQ receiver reference voltage output to DRAM
Power Supplies			
VDD	A	103	Nominal supply for DDR I/O (or Core if apply)
VSS	A	129	Ground
AVDD	A	1	Analog Power Supply
AVSS	A	1	Analog Ground
PVDD	A	4	PLL Clock driver supply
VCCSPD	A	1	SPD Power Supply
Other pins			
BFUNC	I	1	Buffer Function Bit: When BFUNC = 0, MB is used as a regular buffer on LR-DIMM. When BFUNC = 1, MB is used as a buffer for LAI function. On LR-DIMM, BFUNC is tied to Ground
RFU	NC	3	Reserved for Future Use. Must be floated on DIMM.
No Ball		172	
SUM of all pins		588	

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4 Host Interface Protocol and Requirement

4.1 MB Modes of operation

The MB operates in one of two modes: Direct Rank Addressing and Rank Multiplication. The mode of operation is based on both the DIMM configuration and the configuration register programming. In most cases a DIMM can be programmed to operate in either mode, although there are DIMM types where the specific configuration allows for only one mode. For instance a 2 rank LRDIMM can only operate in Direct Rank Addressing mode.

For DIMMs which can operate in either mode the host controller determines which mode will be used and programs the DIMM accordingly. This determination is up the host and may involve the platform configuration (i.e. the number of chip selects supplied to the DIMM socket), performance trade-offs, and the capabilities of the host.

Within the Rank Multiplication mode there may be sub-modes which the host can choose. An 8 rank DIMM could be addressed as two logical ranks of 4 sub-ranks each (RM=4), or 4 logical ranks of 2 sub-ranks each (RM=2). The former would use two chip selects from the host while the latter would use four.

Table 8 — Modes of operation for each DIMM type

Physical Ranks	Mode (Direct or RM)	Host DCS_n signals used	RM Factor	Comments
1	Direct	1	NA	Direct Rank Addressing is the only choice
2	Direct	2	NA	Direct Rank Addressing is the only choice
4	Direct	4	NA	Available on a platform which supplies 4 chip selects to the DIMM socket.
4	RM	2	RM=2	
8	Direct	8	NA	The 8 DCS mode may not be supported on the DIMM.
8	RM	4	RM=2	Available on a platform which supplies 4 chip selects to the DIMM socket. Not available for 4Gbit DRAM devices since this would require A16 from the host, which is muxed with DCS2_n.
8	RM	2	RM=4	

4.1.1 Direct Rank Addressing Mode

Direct Rank Addressing works like a standard RDIMM. The host controller provides a chip select for each physical rank on the DIMM. Like the SSTE32882 register the MB will pass the DCS_n input from the host to the appropriate QCS_n outputs to the DRAMs. The DCS_n is not passed through under the following conditions:

- A Register Control Word is being written (chip selects 0 & 1 are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

There is no special handling of refresh commands in Direct Rank Addressing mode. Any of the three CKE modes may be used with Direct Rank Addressing Mode.

As with RDIMMs, all 8 banks of each physical rank are exposed to the host controller, and may be all opened, adhering to the DRAM specifications.

4.1.2 Rank Multiplication Mode

In the Rank Multiplication Mode, multiple (2 or 4) physical ranks appear to the host controller as a single logical rank of a larger size. This is done by utilizing additional row address bits during the activate command as sub-rank select bits. The read and write commands do not require additional sub-rank select bits from the host since the sub-rank information is stored in the MB from the Activate command. Other commands such as Refresh may optionally use rank select bits based on configuration register settings. See the Rank Multiplication Command Details below.

The basic operation is as follows, assuming an 8 rank DIMM with 1Gbit x4 DRAMs using two host chip selects. Each host chip select will address 4 physical ranks of memory (RM=4). 1Gbit x4 DRAMs use A13:0 as row address bits, so A15 and A14 will be the two sub-rank select bits, or RM bits. DCS0_n will address physical ranks 0, 2, 4, and 6, while DCS1_n will address ranks 1, 3, 5, and 7.

Table 9 — Rank Multiplication Command Details

	Command	DCS_n	A15:14 (RM bits)	BA2:0	Physical Rank	Comment
1	Activate	0	01	100	2	MB registers that bank 4 for DCS0_n is open in Rank 2
2	Read	0	NA	100	2	Goes to Rank 2 since most recent Activate for Bank 4 DCS0_n was to Rank 2 (Uses RM bits stored above).
3	Activate	0	11	011	6	
4	Activate	1	00	011	1	This is legal since bank 3 can be opened independently in different logical ranks.
5	Write	0	NA	100	2	Again uses RM bits from the first step.
6	Read	0	NA	011	6	Most recent activate for bank 3 of DCS0 was to Rank 6
7	Read	1	NA	011	1	Most recent activate for bank 3 of DCS1 was to Rank 1
8	Precharge Single	0	NA	100	0, 2, 4, 6	Precharge is broadcast to all sub-ranks (this assumes MB is configured to broadcast precharges). Only rank 2 has a page open in bank 4. The other ranks do nothing since bank 4 is already closed.

Even though each physical rank has 8 banks which may be opened, only 8 banks in total are exposed to the host controller for each logical rank. At any given time a specific bank number can be open in only one of the sub-ranks. Effectively this increases the number of rows in each bank, which is what is done in a larger DRAM technology. A total of 8 banks per logical rank can be open at once. These open banks could all be in the same sub-rank, or scattered throughout the sub-ranks. This is solely based on the RM bits (A15:14 in the example above) during the activates.

Logical ranks are independent of each other. Each logical rank exposes 8 banks to the host. So in steps 3 and 4 above, bank 3 is open in two different physical ranks simultaneously because they are part of different logical ranks.

The MB is required to store the RM bits on each activate. They must be stored separately for each bank within each logical rank.

For two logical ranks this is 2 RM bits times 8 banks times 2 logical ranks.

For four logical ranks this is 1 RM bit times 8 banks times 4 logical ranks.

Both cases support the max 8 physical ranks.

4.1.2.1 RM bits for each configuration

Table 10 lists the rank multiplication bits used for each configuration.

Table 10 — RM bits for each DIMM type.

DRAM Tech	Physical ranks	Logical Ranks	RM Factor	Host Row Address Bits	RM bit(s)	Row address bits used by DRAM	Logical Rank size	DIMM size, x4 DRAMs	DIMM size, x8 DRAMs
1 Gbit	4	2	2	A14:0	A14	A13:0	2 Gbit	8 Gbytes	4 Gbytes
1 Gbit	8	2	4	A15:0	A15:14	A13:0	4 Gbit	16 Gbytes	8 Gbytes
1 Gbit	8	4	2	A14:0	A14	A13:0	2 Gbit	16 Gbytes	8 Gbytes
2 Gbit	4	2	2	A15:0	A15	A14:0	4 Gbit	16 Gbytes	8 Gbytes
2 Gbit	8	2	4	A16:0	A16:15	A14:0	8 Gbit	32 Gbytes	16 Gbytes
2 Gbit	8	4	2	A15:0	A15	A14:0	4 Gbit	32 Gbytes	16 Gbytes
4 Gbit	4	2	2	A16:0	A16	A15:0	8 Gbit	32 Gbytes	16 Gbytes
4 Gbit	8	2	4	A17:0	A17:16	A15:0	16 Gbit	64 Gbytes	32 Gbytes
4 Gbit	8	4	2	Not Possible - A16 shared with DCS2_n					

All combinations using Rank Multiplication are listed in Table 10. x4 and x8 DRAMs use the same row address bits, so the RM bits are the same for both.

Since A17 and A16 on the DIMM are muxed with DCS3_n and DCS2_n, the final row in Table 10 is not possible as A16 and CS2_n cannot be used at the same time.

4.1.2.2 Rank Decoding

Table 11, Table 12, Table 13, and Table 14 show the rank decoding for each mode of operation, as well as the matching of the QCS_n signals to the DCKE inputs and QCKE outputs.

Table 11 — Normal and Rank Multiplication Control Signal Connectivity without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

Description	# Physical Ranks	DIMM Physical Rank #	Host DCS[0]_n	Buffer Logical QCS Assertion	Buffer QACS[0]_n	Buffer QBCS[0]_n	Host CKE F[0]RC6[DA4, DA3] = 00 or 10	Host CKE F[0]RC6 [DA4, DA3] = 01	Buffer QACKE assertion	Buffer QBCKE assertion
Normal Mode (No Rank Multiplication)	1	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
	2	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		2	DCS[2]_n	QCS2	QACS[2]_n	QBCS[2]_n	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	QBCS[3]_n	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
2 Way Rank Multiplication	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]
	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		4		QCS4	-	QBCS[0]_n				
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		5 (m)		QCS5	-	QBCS[1]_n				
		2	DCS[2]_n	QCS2	QACS[2]_n	-	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		6		QCS6	-	QBCS[2]_n				
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	-	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
		7 (m)		QCS7	-	QBCS[3]_n				
4 Way Rank Multiplication	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	-		DCKE[2]	QACKE[2]	QBCKE[2]
		4		QCS4	-	QBCS[0]_n		DCKE[0]	QACKE[0]	QBCKE[0]
		6		QCS6	-	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	-		DCKE[3]	QACKE[3]	QBCKE[3]
		5 (m)		QCS5	-	QBCS[1]_n		DCKE[1]	QACKE[1]	QBCKE[1]
		7 (m)		QCS7	-	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]

NOTE For 4 Rank x4 QDP DIMM (one row) Raw Card, QxCKE[0] is connected to DIMM physical Rank 0 and Rank 2. QxCKE[1] is connected to DIMM physical Rank 1 and Rank 3.

**Table 12 — Normal and Rank Multiplication Control Signal Connectivity with Rank 1 and Rank 5 Swap
(F[0]RC2 DA4 = 0b)**

Description	# Physical Ranks	DIMM Physical Rank #	Host DCS[0]_n	Buffer Logical QCS Assertion	Buffer QACS[0]_n	Buffer QBCS[0]_n	Host CKE F[0]RC6[DA4, DA3] = 00 or 10	Host CKE F[0]RC6 [DA4, DA3] = 01	Buffer QACKE assertion	Buffer QBCKE assertion
Normal Mode (No Rank Multiplication)	1	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
	2	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		2	DCS[2]_n	QCS2	QACS[2]_n	QBCS[2]_n	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	QBCS[3]_n	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
2 Way Rank Multiplication	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]
	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		4		QCS4	-	QBCS[0]_n				
		1 (m)	DCS[1]_n	QCS1	QBCS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		5 (m)		QCS5	-	QACS[1]_n				
		2	DCS[2]_n	QCS2	QACS[2]_n	-	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		6		QCS6	-	QBCS[2]_n				
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	-	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
		7 (m)		QCS7	-	QBCS[3]_n				
4 Way Rank Multiplication	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	-		DCKE[2]	QACKE[2]	QBCKE[2]
		4		QCS4	-	QBCS[0]_n		DCKE[0]	QACKE[0]	QBCKE[0]
		6		QCS6	-	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QBCS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	-		DCKE[3]	QACKE[3]	QBCKE[3]
		5 (m)		QCS5	-	QACS[1]_n		DCKE[1]	QACKE[1]	QBCKE[1]
		7 (m)		QCS7	-	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]

NOTE For 4 Rank x4 QDP DIMM (one row) Raw Card, QxCKE[0] is connected to DIMM physical Rank 0 and Rank 2. QxCKE[1] is connected to DIMM physical Rank 1 and Rank 3.

Host to DRAM CS Mapping

DCS[0]_n only goes to EVEN numbered QCS[x]_n ranks

DCS[1]_n only goes to ODD numbered QCS[x]_n ranks

Table 13 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS[3: 0]_n	8 Rank QACS[3: 0]_n	1,2,4 Rank QBCS[3: 0]_n	1,2,4 Rank QACS[3:0] _n	Comment
0000	Normal Mode (No Rank Multiplication)	1, 2 or 4	0	1	0	1	x	x	1, 3	-	-	0101	0101	
			0	1	1	0	x	x	1, 2	-	-	1001	1001	
			0	1	1	1	x	x	1	-	-	1101	1101	
			1	0	0	1	x	x	0, 3	-	-	0110	0110	
			1	0	1	0	x	x	0, 2	-	-	1010	1010	
			1	0	1	1	x	x	0	-	-	1110	1110	
			1	1	0	0	x	x	2, 3	-	-	0011	0011	
			1	1	0	1	x	x	3	-	-	0111	0111	
			1	1	1	0	x	x	2	-	-	1011	1011	
			1	1	1	1	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	-	-	1111	1111	RCW
0001	2 Way Rank Multiplication using A[14]	2	1	0	x	x	x	0	0	-	-	1110	1110	1 Gbit DDR3 SDRAM
			1	0	x	x	x	1	2	-	-	1011	1011	
			0	1	x	x	x	0	1	-	-	1101	1101	
			0	1	x	x	x	1	3	-	-	0111	0111	
		4	1	0	1	1	x	0	0	1111	1110	-	-	
			1	0	1	1	x	1	4	1110	1111	-	-	
			0	1	1	1	x	0	1	1111	1101	-	-	
			0	1	1	1	x	1	5	1101	1111	-	-	
			1	1	1	0	x	0	2	1111	1011	-	-	
			1	1	1	0	x	1	6	1011	1111	-	-	
			1	1	0	1	x	0	3	1111	0111	-	-	
			1	1	0	1	x	1	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0010	2 Way Rank Multiplication using A[15]	2	1	0	x	x	0	x	0	-	-	1110	1110	2 Gbit DDR3 SDRAM
			1	0	x	x	1	x	2	-	-	1011	1011	
			0	1	x	x	0	x	1	-	-	1101	1101	
			0	1	x	x	1	x	3	-	-	0111	0111	
		4	1	0	1	1	0	x	0	1111	1110	-	-	
			1	0	1	1	1	x	4	1110	1111	-	-	
			0	1	1	1	0	x	1	1111	1101	-	-	
			0	1	1	1	1	x	5	1101	1111	-	-	
			1	1	1	0	0	x	2	1111	1011	-	-	
			1	1	1	0	1	x	6	1011	1111	-	-	
			1	1	0	1	0	x	3	1111	0111	-	-	
			1	1	0	1	1	x	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW

Table 13 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS[3: 0]_n	8 Rank QACS[3: 0]_n	1,2,4 Rank QBCS[3: 0]_n	1,2,4 Rank QACS[3:0] _n	Comment
0011	2 Way Rank Multi- plication using A[16]	2	1	0	x	0	x	x	0	-	-	1110	1110	4 Gbit DDR3 SDRAM
			1	0	x	1	x	x	2	-	-	1011	1011	
			0	1	x	0	x	x	1	-	-	1101	1101	
			0	1	x	1	x	x	3	-	-	0111	0111	
		4	Not Supported							N/A	N/A	N/A	N/A	RCW
		2 or 4	1	1	1	x	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	
0101	4 Way Rank Multi- plication using A[15:14]	2	1	0	x	x	0	0	0	1111	1110	-	-	1 Gbit DDR3 SDRAM
			1	0	x	x	0	1	2	1111	1011	-	-	
			1	0	x	x	1	0	4	1110	1111	-	-	
			1	0	x	x	1	1	6	1011	1111	-	-	
			0	1	x	x	0	0	1	1111	1101	-	-	
			0	1	x	x	0	1	3	1111	0111	-	-	
			0	1	x	x	1	0	5	1101	1111	-	-	
			0	1	x	x	1	1	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0110	4 Way Rank Multi- plication using A[16:15]	2	1	0	x	0	0	x	0	1111	1110	-	-	2 Gbit DDR3 SDRAM
			1	0	x	0	1	x	2	1111	1011	-	-	
			1	0	x	1	0	x	4	1110	1111	-	-	
			1	0	x	1	1	x	6	1011	1111	-	-	
			0	1	x	0	0	x	1	1111	1101	-	-	
			0	1	x	0	1	x	3	1111	0111	-	-	
			0	1	x	1	0	x	5	1101	1111	-	-	
			0	1	x	1	1	x	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0111	4 Way Rank Multi- plication using A[17:16]	2	1	0	0	0	x	x	0	1111	1110	-	-	4 Gbit DDR3 SDRAM
			1	0	0	1	x	x	2	1111	1011	-	-	
			1	0	1	0	x	x	4	1110	1111	-	-	
			1	0	1	1	x	x	6	1011	1111	-	-	
			0	1	0	0	x	x	1	1111	1101	-	-	

Table 14 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS [3:0]_n	8 Rank QACS[3: 0]_n	1,2,4 Rank QBCS[3: 0]_n	1,2,4 Rank QACS[3:0] _n	Comment
0000	Normal Mode (No Rank Multiplication)	1, 2 or 4	0	1	0	1	x	x	1, 3	-	-	0101	0101	
			0	1	1	0	x	x	1, 2	-	-	1001	1001	
			0	1	1	1	x	x	1	-	-	1101	1101	
			1	0	0	1	x	x	0, 3	-	-	0110	0110	
			1	0	1	0	x	x	0, 2	-	-	1010	1010	
			1	0	1	1	x	x	0	-	-	1110	1110	
			1	1	0	0	x	x	2, 3	-	-	0011	0011	
			1	1	0	1	x	x	3	-	-	0111	0111	
			1	1	1	0	x	x	2	-	-	1011	1011	
			1	1	1	1	x	x	x	-	-	1111	1111	
0001	2 Way Rank Multiplication using A[14]	2	0	0	x	x	x	x	RCW	-	-	1111	1111	RCW
			1	0	x	x	x	0	0	-	-	1110	1110	1 Gbit DDR3 SDRAM
			1	0	x	x	x	1	2	-	-	1011	1011	
			0	1	x	x	x	0	1	-	-	1101	1101	
			0	1	x	x	x	1	3	-	-	0111	0111	
		4	1	0	1	1	x	0	0	1111	1110	-	-	
			1	0	1	1	x	1	4	1110	1111	-	-	
			0	1	1	1	x	0	1	1101	1111	-	-	
			0	1	1	1	x	1	5	1111	1101	-	-	
			1	1	1	0	x	0	2	1111	1011	-	-	
			1	1	1	0	x	1	6	1011	1111	-	-	
			1	1	0	1	x	0	3	1111	0111	-	-	
			1	1	0	1	x	1	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0010	2 Way Rank Multiplication using A[15]	2	1	0	x	x	0	x	0	-	-	1110	1110	2 Gbit DDR3 SDRAM
			1	0	x	x	1	x	2	-	-	1011	1011	
			0	1	x	x	0	x	1	-	-	1101	1101	
			0	1	x	x	1	x	3	-	-	0111	0111	
		4	1	0	1	1	0	x	0	1111	1110	-	-	
			1	0	1	1	1	x	4	1110	1111	-	-	
			0	1	1	1	0	x	1	1101	1111	-	-	
			0	1	1	1	1	x	5	1111	1101	-	-	
			1	1	1	0	0	x	2	1111	1011	-	-	
			1	1	1	0	1	x	6	1011	1111	-	-	
			1	1	0	1	0	x	3	1111	0111	-	-	
			1	1	0	1	1	x	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW

Table 14 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS [3:0]_n	8 Rank QACS[3: 0]_n	1,2,4 Rank QBCS[3: 0]_n	1,2,4 Rank QACS[3:0] _n	Comment
0011	2 Way Rank Multi- plication using A[16]	2	1	0	x	0	x	x	0	-	-	1110	1110	4 Gbit DDR3 SDRAM
			1	0	x	1	x	x	2	-	-	1011	1011	
			0	1	x	0	x	x	1	-	-	1101	1101	
			0	1	x	1	x	x	3	-	-	0111	0111	
		4	Not Supported							N/A	N/A	N/A	N/A	
		2 or 4	1	1	1	x	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0101	4 Way Rank Multi- plication using A[15:14]	2	1	0	x	x	0	0	0	1111	1110	-	-	1 Gbit DDR3 SDRAM
			1	0	x	x	0	1	2	1111	1011	-	-	
			1	0	x	x	1	0	4	1110	1111	-	-	
			1	0	x	x	1	1	6	1011	1111	-	-	
			0	1	x	x	0	0	1	1101	1111	-	-	
			0	1	x	x	0	1	3	1111	0111	-	-	
			0	1	x	x	1	0	5	1111	1101	-	-	
			0	1	x	x	1	1	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0110	4 Way Rank Multi- plication using A[16:15]	2	1	0	x	0	0	x	0	1111	1110	-	-	2 Gbit DDR3 SDRAM
			1	0	x	0	1	x	2	1111	1011	-	-	
			1	0	x	1	0	x	4	1110	1111	-	-	
			1	0	x	1	1	x	6	1011	1111	-	-	
			0	1	x	0	0	x	1	1101	1111	-	-	
			0	1	x	0	1	x	3	1111	0111	-	-	
			0	1	x	1	0	x	5	1111	1101	-	-	
			0	1	x	1	1	x	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0111	4 Way Rank Multi- plication using A[17:16]	2	1	0	0	0	x	x	0	1111	1110	-	-	4 Gbit DDR3 SDRAM
			1	0	0	1	x	x	2	1111	1011	-	-	
			1	0	1	0	x	x	4	1110	1111	-	-	
			1	0	1	1	x	x	6	1011	1111	-	-	
			0	1	0	0	x	x	1	1101	1111	-	-	

4.1.2.3 Rank Multiplication Command Details

This section provides the operational details for each command which the host can send to the DIMM when in Rank Multiplication mode.

“RM bits” refer to the one (RM=2) or two (RM=4) address bits that are used for rank multiplication. These can be address bits A17 through A14, based the physical rank density. See the RM bit table above.

4.1.2.3.1 Activate Command

The activate command is sent a single sub-rank (physical rank), as determined by the RM bit(s). Decoding is done based on the Rank Decoding section above. It is the host’s responsibility to assure that no other pages are open in this logical rank / bank combination before issuing the Activate command. The RM bit(s) are stored by the MB for this logical rank / bank combination for later use by read and write commands.

4.1.2.3.2 Read or Write commands

Read and write commands are handled in the same manner. This also includes the Autoprecharge options (as determined by A10) and the burst length options (as determined by A12 and an MR bit).

The read and write commands are sent to a single sub-rank, as determined by the stored RM bits from the most recent Activate command to this logical rank / bank combination. For instance, if the most recent Activate command to logical rank 0, bank 2 targeted physical rank 4, then the read and write commands to logical rank 0 bank 2 will also target physical rank 4.

Unlike DRAMs, where the read data is always aligned to the edges of the incoming clock, the read data from the MB on the Host Bus is aligned to an internal clock phase based on the Receiver Enable training results of the MB to the DRAMs.

In Minimum latency mode (F3RC6 DA3,DA4=’00’) for speeds up to and including 1600 MT/s, each byte / nibble lane independently determines the internal Host side read data clock phase based on the longest read round trip latency from all the DRAMs attached to that particular byte / nibble lane. The result of this is that each byte/nibble lane will have different read timing as seen by the Host controller, but no matter which physical rank is read, the MB will have constant timing for that particular byte/nibble lane.

In Minimum latency mode (F3RC6 DA3,DA4=’00’) for speeds greater than 1600 MT/s (i.e., 1866 MT/s and 2133 MT/s), each byte lane independently determines the internal Host side read data clock phase based on the longest read round trip latency from all the DRAMs attached to that particular byte lane. The result of this is that each byte lane will have different read timing as seen by the Host controller, but no matter which physical rank is read, the MB will have constant timing for that particular byte lane.

In Minimum skew mode (F3RC6 DA3,DA4=’10’), the MB uses the longest read round trip latency from all of the byte/nibble lanes to derive the common internal read clock phase for all of the byte/nibble lanes. This result of this is that all 72 bits of the MB are driven in unison based on this common internal read clock no matter which physical rank is read.

4.1.2.3.3 Precharge Single and Precharge All Commands

The Precharge Single command operation is based on the Precharge Control configuration bit (F0RC14 bit DA4).

A configuration bit and address bit determine the operation of the Precharge Single and Precharge All commands.

Table 15 — Precharge Single and Precharge All Command Control

Refresh/ Precharge Control bit (F0RC14 DA4)	A0 of the command	Command action
0	X	Broadcast to all sub-ranks
1	0	Send to sub-rank specified by RM bits
1	1	Broadcast to all sub-ranks

When Broadcast to All Sub-ranks is specified, the Precharge command will be sent to all sub-ranks of the logical rank. A Precharge Single command targets only one bank, as specified by BA[2:0]. There can only be a page open in one sub-rank of a given bank. The other sub-ranks will not perform any operation. A Precharge All command affects all 8 banks of the logical rank. Different banks may have a page open in different sub-ranks. The Precharge All will close all banks in all sub-ranks associated with the logical rank.

When the Precharge command targets a single sub-rank, the RM bits from the host are used to specify the sub-rank. Note that it does NOT use the stored RM bits like the read and write commands, but uses the RM bit(s) sent by the host along with the Precharge Single Command. The RM bits are in the same location as they are for the Activate command, which is based on the physical DRAM density. The primary purpose of this mode is to allow the pages to be closed in an individual rank in preparation for a targeted refresh without closing pages in physical ranks that will not be targeted by the refresh. It also allows activity to some physical ranks while others are being refreshed. A rank being refreshed cannot accept a Precharge command.

4.1.2.3.4 Refresh Command

The Refresh Command has three modes of operation based on the Refresh Control bit and the Refresh_Stagger register.

4.1.2.3.4.1 Refresh Broadcast without Stagger

Refresh Broadcast without stagger is the default mode. In this mode the refresh command is sent to all sub-ranks associated with the logical rank. The refresh is sent at the same time to all of these ranks. This mode is selected when the Refresh control bit is set to a 0 and the Refresh_Stagger register is set to all 0s.

4.1.2.3.4.2 Refresh Broadcast with Stagger

Refresh Broadcast with Stagger is selected when the Refresh Control bit is set to a 0 and the Refresh_Stagger is non-zero. In this mode the refresh will be immediately sent to one of the sub-ranks, then sent to each successive sub-rank after a programmed amount of time. After the stagger time it is possible that the host controller is sending commands to other logical ranks on the DIMM, making the DRAM bus unavailable. The MB will wait for an available command slot by monitoring the command flow from the host. Following the 2nd sub-rank refresh the process is complete for RM=2. For RM=4 the stagger process repeats two more times.

The host controller must adjust its tRFC take into account the staggering of the refreshes, and the extra clocks that the controller may have to wait for an open command slot. In a very unusual case the number of extra clocks that the MB may have to wait for an empty slot could be very large. To avoid having to set a very large tRFC to accommodate this, a Refresh_Jitter_Limit is programmed. This limits the total number of extra clocks added due command slots being unavailable. If the limit is reached, the rest of the sub-rank refreshes are dropped. Dropping refreshes on very rare occasions is less hazardous than violating the tRFC of a DRAM.

4.1.2.3.4.2 Refresh Broadcast with Stagger (cont'd)

The following algorithm is used by the MB:

- 1) Host sends Refresh Command to MB
- 2) MB sends Refresh command to the physical rank pointed to by the Refresh_Subrank_Pointer for this logical rank. Refresh_Subrank_Pointer is incremented.
- 3) MB loads the Refresh_Jitter counter based on the Refresh_Jitter register setting.
- 4) MB loads the Refresh_Stagger counter based on the Refresh_Stagger register setting.
- 5) MB decrements the Refresh_Stagger counter on each DRAM clock. Refresh_Jitter_counter does NOT decrement.
- 6) When Refresh_Stagger counter reaches 0 the next Refresh is queued up and sent as soon as the DRAM command bus becomes available.
- 7) The Refresh_Jitter counter is decremented on each clock that the MB must wait on an unavailable DRAM command bus. If the Refresh_Jitter counter reaches 0, the refreshes for the rest of the sub-ranks, including the one queued up are cancelled. Go to step 10 in this case.
- 8) As soon as the DRAM bus becomes available the Refresh Command is sent to the sub-rank pointed to by the Refresh_Subrank_Pointer and the pointer is incremented.
- 9) If there are still subbanks to refresh, return to step 4 (Note that the Jitter_counter is NOT reset).
- 10) If the Refresh_Start_rank bit is set to 0, set the Refresh_Subrank_Pointer to 0, else leave it where it was.

The host's tRFC is set to the

$$\text{DRAM tRFC} + (\text{RM}-1) * \text{Refresh_Stagger} + \text{Refresh_Jitter_Limit}$$

Where RM = the Rank Multiplication factor (2 or 4). It is the host's responsibility to set the Refresh_Jitter_Limit based on the controller design, and the frequency of dropped refreshes that is acceptable.

4.1.2.3.4.3 Targeted Refresh

The Targeted Refresh mode is used if the Refresh Control bit is set to a 1. In this case the refresh command is sent to the sub-rank determined by the RM bits sent by the host. It is the host's responsibility to manage refresh to each subrank.

4.1.2.3.5 ZQ Cal Command

ZQ Cal commands are to all sub-ranks associated with a logical rank. Note that this requires that each physical rank have separate ZQ resistors.

4.1.2.3.6 Enter Self Refresh

Self Refresh is entered by sending a Refresh on the command signals at the same time as CKE is sampled low, with CKE having been high on the previous clock. All sub-ranks of a logical rank will be put in self refresh together. The command will be broadcast to all sub-ranks even if the Refresh Control bit is set to the target refresh mode.

When the number of DCKE inputs being used matches the number of logical ranks (DCS_n inputs being used) the host has individual control of which ranks are put into self refresh.

There are several special cases when the number of DCKEs and DQCS_ns do not match.

4.1.2.3.6.1 2 DCKE mode with 4 or 8 logical ranks

In this case all of the even numbered logical ranks must be put into self refresh together, asserting all of the even numbered DCS_n signals. Likewise all odd numbered logical ranks must be put into self refresh together, asserting all of the odd numbered DCS_n signals. This is required due to the sharing of the DCKE input. Putting one logical rank into self refresh by asserting only one DCS_n signal would put the other ranks associated with that DCKE input into one of the power down states (Precharge powerdown if all paged closed). Raising CKE again to attempt to put another rank into self refresh would cause the first rank to exit self refresh.

4.1.2.3.6.2 4 DCKE mode with 8 logical ranks

In this case ranks 0 & 4 must be put into self refresh together. Likewise with ranks 1 & 5, 2 & 6, and 3 & 7 as each of these rank pairs share a DCKE. Note that 8 logical rank mode may not be supported on the DIMM.

4.1.2.3.6.3 4 DCKE mode with 2 logical ranks

This mode is possible to allow sub-rank granularity for CKE control. DCKE0 and DCKE2 will both be associated with the DCS0_n logical ranks, but control the QCKE to different subranks. The entire logical rank must be put into self refresh at the same time, which means that DCKE0 and DCKE2 must both transition during the self refresh entry command. Likewise for DCKE1 and DCKE3. Taking just one DCKE from high to low at the self refresh entry is not defined, and MB operation is indeterminate.

4.1.2.3.6.4 Soft CKE

With soft CKE the QCKE outputs are controlled by host commands, not directly by the DCKE inputs. Since a soft CKE command cannot be sent at the same time as a refresh command, enter self refresh and exit self refresh are special cases where the DCKE inputs DO affect the QCKE outputs. Soft CKE will always use 2 DCKE inputs. Normally transitions on the DCKE inputs are not transferred to the QCKE outputs, but are used to control the MB power state. When the MB detects an Enter Self Refresh command by means of a DCKE0 being sampled high followed by sampled low with a refresh command on the even numbered DCS_n inputs, the associated QCKE0 and QCKE2 will be taken low with refresh command sent to the DRAMs in order to put all of those physical ranks into self refresh. Likewise with DCKE1 and the odd DCS_n inputs.

It is the host's responsibility to have all QCKE outputs high (via a soft refresh command) before the Self Refresh Entry command. If the host has one or more of the QCKE outputs low, the self refresh command will be ignored by the physical ranks associated with that QCKE output and the DRAMs will not enter self refresh.

Exiting self refresh is also a special case where the DCKE low to high transition is passed through to the appropriate QCKE outputs. An Exit Self Refresh command looks the same to the MB as an Exit Powerdown command (MB powerdown in this case), but the MB must be able to take different actions based on which command it is. The MB accomplishes this by storing whether the most recent high to low transition on each DCKE input was an Enter Self Refresh or not. If it was a self refresh entry, the subsequent low to high transition on that DCKE is considered an Exit Self Refresh, and passed onto the QCKE output. Otherwise the DCKE transition is not passed onto the QCKE outputs and only used for power control of the MB itself.

A common restriction for all cases is that logical ranks 0 and 1 cannot be put into self refresh on the same clock as this would activate CS0_n and CS1_n simultaneously. The MB would interpret this as a Control Word write and the command would not be sent to the DRAMs.

4.1.2.3.7 Exit Self Refresh

Taking a DCKE high will cause the associated QCKE(s) to go high taking the DRAMs out of self refresh mode. Any number of DCKE signals may go high at once. See the Enter Self Refresh section above for special handling of the Exit Self Refresh command.

Taking a QCKE output from low to high will take the associated ranks out of whatever power down mode (self refresh, precharge powerdown slow, precharge powerdown fast, or active powerdown) that they were in.

4.1.2.3.8 Mode Register Set

The operation of the Mode Register Set command is controlled by the MRS control bit. When a 0, MRS commands are sent to all sub-ranks. When a 1 it targets only the sub-rank selected by the RM bits. The targeted commands will be necessary to set different sub-ranks Rtt_nom values and Precharge Powerdown modes.

A configuration bit and address bit determine the operation of the MRS command.

Table 16 — MRS Control

MRS Control bit (F0RC14 DBA0)	A13 of the command	Command action
0	X	Broadcast to all sub-ranks
1	0	Send to sub-rank specified by RM bits
1	1	Broadcast to all sub-ranks

When Broadcast to All Sub-ranks is specified, the MRS command will be sent to all sub-ranks of the logical rank

When the MRS command targets a single sub-rank, the RM bits from the host are used to specify the sub-rank. Note that it does NOT use the stored RM bits like the read and write commands, but uses the RM bit(s) sent by the host along with the Mode Register Set Command. The RM bits are in the same location as they are for the Activate command, which is based on the physical DRAM density.

4.1.2.3.9 NOP

A NOP is when DRAS_n, DCAS_n, and DWE_n are all high, and one of the DCS_n inputs is low. The MB will pass a NOP onto the DRAM bus, broadcasting to all sub-ranks.

4.1.2.3.10 Control Word Write

The control word is written into the MB when DCS0_n and DCS1_n are both asserted. This case is treated as a Deselect as far as the DRAM interface is concerned. The command and address are not sent on to the DRAM bus and no QCS is asserted. The control register in the MB is written according to the address bits.

4.1.2.3.11 Deselect

Deselect is when all DCS_n inputs remain high. The command and address signals are not passed onto the Q outputs on a deselect.

4.2 Command, Address, and Control Signal usage

The MB handles the Command, Address and Control signals somewhat differently than a standard RDIMM.

4.2.1 Command Signals

The Command signals are RAS_n, CAS_n, and WE_n. They are used for the DRAM command encoding, although the state or actions on both address and control signals sometimes are used in the encoding of the command.

In most cases the command signals are passed directly through the MB to the DRAM busses. The table below lists each command and the actions of the MB.

Table 17 — Command and MB Action

Command	RAS _n	CAS _n	WE _n	Oth Conditions	MB Action.
Activate	L	H	H		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Read or Read with Auto Precharge	H	L	H		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Write or Write with Auto Precharge	H	L	L		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Precharge Single	L	H	L	A10=L	Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one.
Precharge All	L	H	L	A10=H	Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one.
Refresh	L	L	H	CKE=H	Pass through to DRAM bus. With Rank Multiplication, configuration bits determine whether it is broadcast, sent to sub-ranks with a stagger, or sent to a single sub-rank.
ZQ Calibration	H	H	L	A15:13=000 or Soft CKE disabled	Pass through to DRAM bus. Broadcast to all subranks.
Soft CKE	H	H	L	A15:13=001 and Soft CKE enabled	Command is not sent to DRAM bus. MB changes the QCKE outputs based on A3:0.
Reserved	H	H	L	A15:13 not 000 or 001 with soft CKE enabled	Command is not sent to the DRAM bus. Treated as NOP.
Enter Self Refresh	L	L	H	CKE transitions H to L	Pass through to DRAM bus. With Rank Multiplication, it is broadcast to all sub-ranks. See in previous section.
Exit Self Refresh				CMD is NOP or deselect, CKE transitions L to H.	See the CKE control section.
Mode Register Set	L	L	L		Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one. The MB will snoop the Mode Register Set commands, storing the MRS bits for its own usage.
NOP	H	H	H		Command is not passed to the DRAM bus. It is treated the same as a Deselect.
Deselect	X	X	X	All CS _n inputs = H	Command is not passed to the DRAM bus.

Table 17 does not differentiate all permutations of commands, such as ZQ Calibration Long or Short. The address bits which select these permutations are passed to the DRAMs.

Individual Command actions are discussed in a previous section.

4.2.2 Address Signals

The address signals consist of A15:0 and BA2:0. In the Rank Multiplication mode one or two address bits are used as sub-rank select bits which are decoded by the MB.

All address bits are passed through to the DRAM busses whenever any of the Chip Selects are active with the following exceptions:

- A Register Control Word is being written (chip selects 0 & 1 are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

4.2.3 Control Signals

Control Signals include the CS_n signals (anywhere from 2 to 8 inputs), CKE (2 or 4) and ODT (1 or 2).

4.2.3.1 Chip Select signals

The Chip Select signals are handled differently depending on whether Rank Multiplication or direct addressing is being used.

4.2.3.1.1 Chip Selects with Direct Addressing

The Chip Select inputs operate the same way in the MB as with LRDIMMs. Each DCS_n input is associated with one physical rank on the DIMM and is passed through the MB to the DRAM side QCS output(s) associated with that rank. The DCS_n is not passed through under the following conditions:

- A Register Control Word is being written (chip selects 0 & 1 are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

Direct addressing may be done with:

- Two physical ranks and two chip selects (DCS0_n and DCS1_n) with operation much like a dual rank RDIMM
- Four physical ranks and four chip selects (DCS[3:0]) with operation much like a quad rank RDIMM
- Eight physical ranks and eight chip selects (DCS[7:0]). A special non-JEDEC DIMM is required for eight chip select support.

4.2.3.1.2 Chip Selects with Rank Multiplication

In the Rank Multiplication mode, the MB will use one or two address bits to determine which sub-rank is targeted. The particular command, and configuration settings will determine how the CS is passed through.

See the Rank Multiplication section for more details.

4.2.3.2 CKE Signals

LRDIMMs have three modes of operation for CKE. These are summarized in Table 18.