

JEDEC STANDARD

DDR4 Registering Clock Driver Definition (DDR4RCD02)

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DDR4 REGISTER DEFINITION (DDR4RCD02)

(From JEDEC Board Ballot, JCB-17-02, formulated under the cognizance of the JC-40.4 Subcommittee on Registered and Fully Buffered Memory Support Logic.)

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR4 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR4 RDIMM and LRDIMM applications.

The terms 'Registering Clock Driver', 'RCD', 'register' or 'device' are used interchangeably to refer to this device in the remainder of this specification.

The purpose is to provide a standard for the DDR4RCD02 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR4RCD02 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 32-bit 1:2 registering clock driver with parity is designed for 1.2 V V_{DD} operation.

All inputs are pseudo-differential with an external or internal voltage reference. All outputs are full swing CMOS drivers optimized to drive single terminated 25 Ω to 50 Ω traces in DDR4 RDIMM and LRDIMM applications. Clock outputs Yn_t and Yn_c , and the control net outputs $QxCKEn$, $QxCSn$ and $QxODTn$ can be driven with a different strengths to compensate for different DIMM net topologies. By disabling unused outputs the power consumption is reduced.

The DDR4RCD02 operates from a differential clock (CK_t/CK_c). Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals could be either re-driven to the outputs or they could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in “Control Word Decoding” on page 69.

2.2 Features and Functions

The DDR4RCD02 has three basic modes of operation associated with the $DA[1:0]$ bits in the DIMM Configuration Control Word (F0RC0D):

- In **Direct DualCS mode** ($DA[1:0] = 00$) the component has two chip select inputs, $DCS0_n$ and $DCS1_n$, and two copies of each chip select output, $QACS0_n$, $QACS1_n$, $QBCS0_n$ and $QBCS1_n$. The inputs pins $DC[2:0]$ are forwarded to two sets of output pins, $QAC[2:0]$ and $QBC[2:0]$. This is the normal operating mode (“QuadCS disabled” and “Encoded CS disabled”).
- In **Direct QuadCS mode** ($DA[1:0] = 01$), the component has four chip select inputs, the two dedicated inputs $DCS[1:0]_n$ and the $DC[0]$ input pin functioning as $DCS2_n$ and the $DC[1]$ input pin functioning as $DCS3_n$, and two copies of each chip select output, $QACS[3:0]_n$ and $QBCS[3:0]_n$. The input pin $DC[2]$ is forwarded to two output pins, $QAC[2]$ and $QBC[2]$. The output pins $QAC[1:0]$ and $QBC[1:0]$ are used as $QACS[3:2]_n$ and $QBCS[3:2]_n$. This is the “QuadCS enabled” mode.

In the two modes above the DDR4RCD02 does not need to decode input signals to generate any chip select outputs.

- In **Encoded QuadCS mode** ($DA[1:0] = 11$), two copies of four output chip selects, i.e. $QACS[3:0]_n$ and $QBCS[3:0]_n$, are decoded out of two $DCS[1:0]_n$ inputs and the $DC[0]$ input. The input pin $DC[2]$ is forwarded to two output pins, $QAC[2]$ and $QBC[2]$. The output pins $QAC[1:0]$ and $QBC[1:0]$ are used as $QACS[3:2]_n$ and $QBCS[3:2]_n$. This is the “Encoded QuadCS” mode.

When the DCS encoding is changed (i.e. when the setting in F0RC0D $DA[1:0]$ is updated), it is necessary for the host to precondition the signals driven on the pins which will be turned into chip select inputs with the correct voltage levels. For example, it is necessary to drive $DCS[3:2]$ both HIGH before F0RC0D $DA[1:0]$ is updated from ‘00’ to ‘01’. This is necessary to prevent a violation of the t_{MRD} parameter.

Through the remainder of this specification, $DCS[n:0]_n$ will indicate all of the chip select inputs, where $n=1$ for

RCD0D DA0=0, and n=3 for RCD0D DA0=1. QxCS[n:0]_n will indicate all of the chip select outputs.

Table 1 — Generic DCS - QxCS Mapping

Input CS	Output CS		
	Direct DualCS mode	Direct QuadCS mode	Encoded QuadCS mode
DCS0_n	QxCS0_n	QxCS0_n	QxCS0_n, QxCS1_n
DCS1_n	QxCS1_n	QxCS1_n	QxCS2_n, QxCS3_n
DCS2_n/DC0	n/a	QxCS2_n	n/a
DCS3_n/DC1	n/a	QxCS3_n	n/a

2.2.1 Direct CS Modes

Commands are sent to a single rank or multiple ranks, as determined by the DCS[n:0]_n and DC[n:0] inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

The number of input chip selects is two (in Direct DualCS mode) or four (in Direct QuadCS mode).

Quad CS Modes

For DIMMs using dual-die packages there is a need for four CS signals rather than the standard two. For these modules two modes are available where four CS outputs are available. The memory controller can select by programming the CS mode control bits which of the two modes it wants to utilize.

There are two ways of accomplishing this:

- by using four CS inputs from the host (DCS[3:0]_n). This is the Direct QuadCS mode. See Chapter 2.2.1, “Direct CS Modes,” above.
- by using two CS inputs and one of the chip ID inputs from the host (DCS[1:0]_n and DC0). See Chapter 2.2.3, “Encoded QuadCS Mode,” below.

2.2.2 Encoded QuadCS Mode

When F0RC0D DA[1:0] = 11 the DDR4 register decodes two sets of four QxCS_n outputs from two DCS_n inputs by using the DC0 as the encoding input.

Table 2 — DCS, DC - QxCS, QxC Mapping in Encoded QuadCS mode

DCS1_n	DCS0_n	DC0	DC2	QxCS[3:0]_n	QxC2
H	H	X	0	HHHH	No change
		X	1		
H	L	0	0	HHHL	0
		0	1		1
		1	0	HHLH	0
		1	1		1
L	H	0	0	HLHH	0
		0	1		1
		1	0	LHHH	0
		1	1		1
L	L	0	0	HLHL ¹	0
		0	1		1
		1	0	LHLH ¹	0
		1	1		1

1. Only one DCSx_n input can be asserted for DRAM MRS and DRAM read commands

No additional address bits are used.

All commands including read, write, precharge, refresh and MRS commands are sent to the rank selected by the two chip selects and chip ID bit 0 coming from the host.

The memory controller needs to handle commands in the same way it would handle a DIMM with two times as many chip selects.

2.3 Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. After the voltage ramp, stable power is provided for a minimum of 200 μ s with DRST_n asserted. When the reset input DRST_n is LOW, all input receivers are disabled, and can be left floating. Since internally generated Vref is selected in F0RC0B DA3 for Input Receiver Vref source after DRST_n is driven LOW, the reference voltage (VrefCA) doesn't need to be stable. In addition, when DRST_n is LOW, all control registers are restored to their default states, which is all '0's unless explicitly stated otherwise. The outputs QRST_n, QACKE0, QACKE1, QBCKE0 and QBCKE1 and BCK_t/BCK_c must drive LOW and BCKE must drive HIGH during reset. All other Qx outputs must float. As long as the DRST_n input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the DRST_n input is pulled HIGH the clock input signal must be stable, the register inputs DCKE0 and DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register must meet the input Setup and Hold specification, as well as accept and transfer input signals to the corresponding outputs. The DRST_n input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on DRST_n while a stable clock signal is present on CK_t and CK_c. In the DDR4 RDIMM and LRDIMM applications, DRST_n is specified to be completely asynchronous with respect to CK_c and CK_t. Therefore, no timing relationship can be guaranteed between the two.

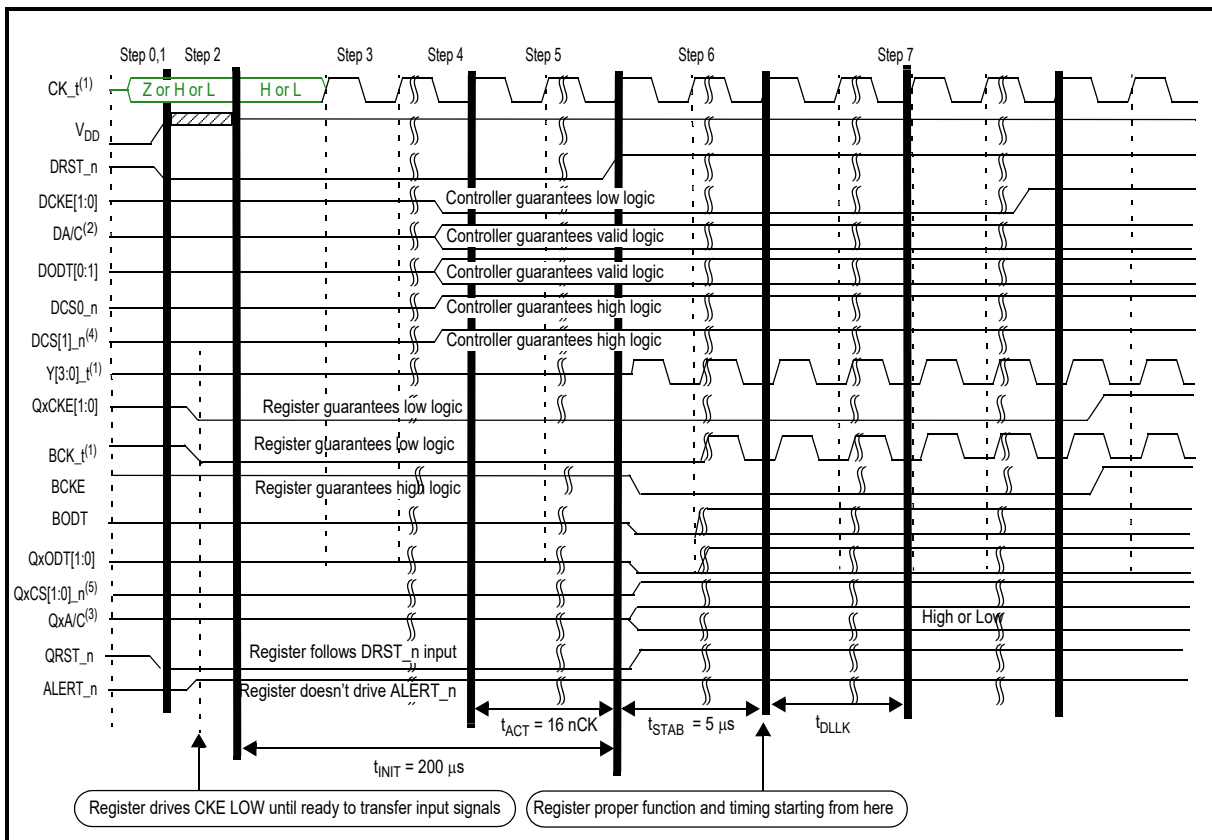


Figure 1 — Timing of Clock and Data During Initialization Sequence

1. CK_c, Y[3:0]_c and BCK_c left out for better visibility
2. DCKE0, DCKE1, DODT0, DODT1, DCS0_n and DCS1_n are not included in this range
3. QxCKEn, QxODTn, QxCsn_n are not included in this range.

4. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
5. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
- 6.) From step 6 onwards, the QxCS2_n and QxCS3_n outputs will initially be enabled and controlled directly by the DC0 and DC1 inputs, respectively, since Direct DualCS mode is enabled by default in F0RC0D. Therefore, it is required that the host always drives the DC0 and DC1 inputs with the correct levels needed for chip select signals during power on initialization for DIMMs utilizing QxCS2_n and QxCS3_n. This also applies in configurations using Encoded QuadCS mode.
7. The output pins QVrefCA and BVrefCA need to have valid $V_{DD}/2$ levels no later than at step 7.

From a device perspective, the initialization sequence must be as shown in Table 3.

Table 3 — DDR4RCD02 Device Initialization Sequence¹

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	V_{DD} , AV_{DD} , PV_{DD}	DRST_n	VrefCA	DCS[1:0]_n ²	DODT0, DODT1	DCKE0, DCKE1	DA/C	DPAR	CK_t, CK_c	QxCS[1:0]_n ³	QxODT0, QxODT1	QxCKE0, QxCKE1	QxA/C	ALERT_n	Y[3:0]_t, Y[3:0]_c
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0→ V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X	Z	Z	L ⁴	Z	H ⁴	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	X or Z	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	X or Z	H	X	L	X	X	running	H	L ⁵	L	X	H	running
7 ⁶	V_{DD}	H	X or Z	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 22, Table 23 and Table 24).					

1. X = Logic LOW or logic HIGH. Z = floating.
2. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
3. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
4. ALERT_n is pulled high externally and QxCKEn will be driven to this logic state by the register after DRST_n is driven LOW and V_{DD} is nominal.
5. This indicates the state of QxODTx after DRST_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge). After the first rising CK edge, within ($t_{STAB} - t_{ACT}$), the state of QxODTx is a function of DODTx (HIGH or LOW).
6. Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is “0”. After initialization, the Host must write to those control registers whose contents are required for frequency and DIMM configuration.

2.3.1 Reset Initialization with Stable Power

The timing diagram in Figure 2 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. DRST_n will be asserted for minimum 1 μ s. This DRST_n timing is based on DDR4 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual DRST_n timing can vary base on specific system requirement, but it cannot be less than 1 μ s as required by JESD79-4. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 and BCK_t/BCK_c must drive LOW and BCKE must drive HIGH during reset.

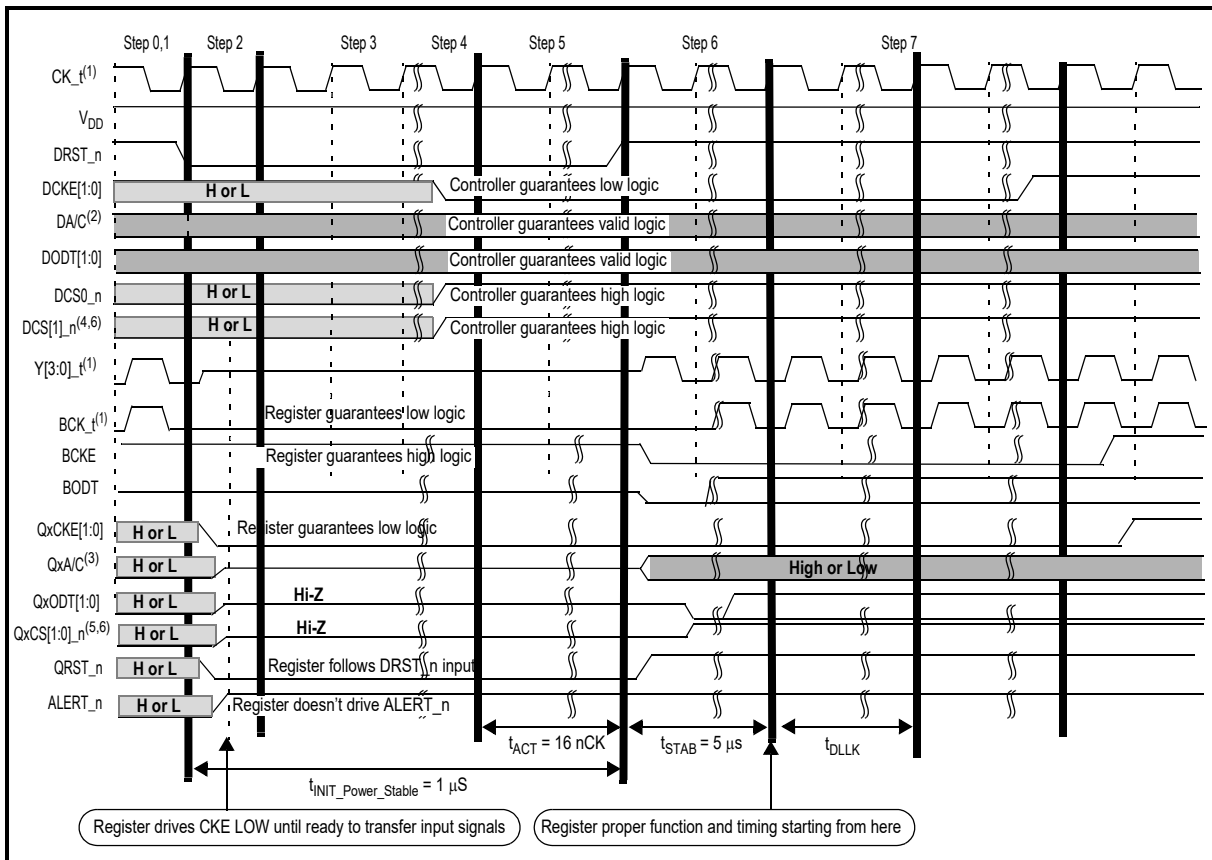


Figure 2 — Timing of Clock and Data during Initialization Sequence with Stable Power

1. CK_c, Y[3:0]_c and BCK_c left out for better visibility
2. DCKE0, DCKE1, DODT0, DODT1, DCS0_n and DCS1_n are not included in this range
3. QxCKEn, QxODTn, QxCSn_n are not included in this range.
4. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
5. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
- 6.) From step 6 onwards, the QxCS2_n and QxCS3_n outputs will initially be enabled and controlled directly by the DC0 and DC1 inputs, respectively, since Direct DualCS mode is enabled by default in F0RC0D. Therefore, it is required that the host always drives the DC0 and DC1 inputs with the correct levels needed for chip select signals during power on initialization for DIMMs utilizing QxCS2_n and QxCS3_n. This also applies in configurations using Encoded QuadCS mode.

Table 4 — DDR4RCD02 Device Initialization Sequence¹ when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	V _{DD} , AV _{DD} , PV _{DD}	DRST_n	V _{refCA}	DCS[1:0]_n ²	DODT0, DODT1	DCKE0, DCKE1	DA/C	DPAR	CK _t , CK _c	QCS[1:0]_n ³	QxODT0, QxODT1	QxCKE0, QxCKE1	QxA/C	ALERT_n	Y[3:0]_t, Y[3:0]_c
0	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L ⁴	Z	H ⁴	Z
3	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ⁵	L	X	H	running
7	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 22, Table 23 and Table 24).					

1. X = Logic LOW or logic HIGH. Z = floating.

2. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.

3. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.

4. ALERT_n is pulled high externally and QxCKEn will be driven to this logic state by the register after DRST_n is driven LOW and V_{DD} is nominal.

5. This indicates the state of QxODTx after DRST_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}), the state of QxODTx is a function of DODTx (HIGH or LOW).

2.4 Parity

The DDR4RCD02 includes a parity checking function. The DDR4RCD02 accepts a parity bit at its input pin DPAR one cycle after the corresponding data input.

If parity checking is enabled, the register only forwards sampled commands to the outputs when no parity error occurred. Since comparing the incoming parity against the parity calculated from the data received one cycle earlier requires a small logic delay, a programmable command latency¹ is available in the Command Latency Adder control word F0RC0F. The min CLA setting with parity enabled is 1 tCK. The latency from DCA input to QCA output is always one cycle greater than the latency from DPAR to QxPAR. Since the DDR4 DRAMs expect the parity input in the same cycle as data, the QxPAR outputs (if enabled) are always sent in the same cycle as the corresponding data outputs. It is the responsibility of the host to ensure Parity control word and the Command Latency Adder control word are programmed in a compatible way.

If parity checking is disabled, the register forwards sampled commands to the outputs unconditionally, i.e., the

1. The definition of 'Command' in this context also includes the QxCSy_n, QxCKEn and QxODTn signals.

command appears on the outputs regardless of whether a parity error occurred or not.

The output timing is determined by the Command Latency Adder control word regardless of whether the device has parity checking enabled or disabled. The behavior with parity checking disabled is the same with the exception that ALERT_n is never asserted as result of a CA parity error (but can still be asserted as a result of an assertion of the ERROR_IN_n input). Even with parity checking disabled the DPAR input is forwarded to both QxPAR outputs (if they are enabled), which are asserted in the same cycle as the command output.

After the DDR4RCD02 receives DPAR from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW.

The convention of parity is even parity, i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. The DIMM-dependent control signals (DCKE0, DCKE1, DCS0_n .. DCS3_n, DODT0 and DODT1) are not included in the parity check computations.

Even after a CA parity error has been registered, the device will still forward DCKEn and DODTn to the DRAMs, and the device will enter CKE power down mode depending on the DCKEn transitions.

If a parity error occurs and parity checking is enabled in F0RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in F0RCFx to '1' and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If Control Gear-down mode is enabled, ALERT_n will be asserted on an even and fixed number of clock cycles after the erroneous command is registered. The assertion of the ALERT_n will either be after four cycles or after six cycles depending on the implementation of Control Gear-down in the RCD. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (F0RC0E) is '0'. In this case the erroneous command and all subsequent commands are not forwarded¹ (i.e. QxCsY_n are not asserted) to the DRAM until the memory controller issues a 'Clear CA Parity Error' command, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Assertion' bit is '1', the ALERT_n pulse width is as defined in Table 47 with start of the ALERT_n pulse width counted from the third input clock edge after the 1st parity error. If the 'ALERT_n Re-enable' bit is '0', the erroneous command and all subsequent commands are not forwarded (i.e. QxCsY_n are not asserted) to the DRAM until the end of the ALERT_n pulse width and parity checking remains disabled until a 'Clear CA Parity Error' command is sent, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Re-enable' bit is '1', the device will re-enable parity after the ALERT_n pulse and the device will forward commands to the DRAM. The 'CA Parity Error Status' bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit. The other bits in the Error Log Register are not updated on this subsequent error. Both the 'CA Parity Error Status' bit as well as the '> 1 Error' bit will be cleared by sending a 'Clear CA Parity Error' command.

Using the CW Source Selection & CW Destination Selection control words (See "CW Selection Control Words" on page 85.) and CW Data control word (See "F0RC6x: CW Data Control Word" on page 86.), the host can read the Error Log Register by writing it first into page 0 of the DRAM MPR, from where the host can read it using the defined DDR4 DRAM MPR read functionality.

2.4.1 Parity Timing Scheme Waveforms

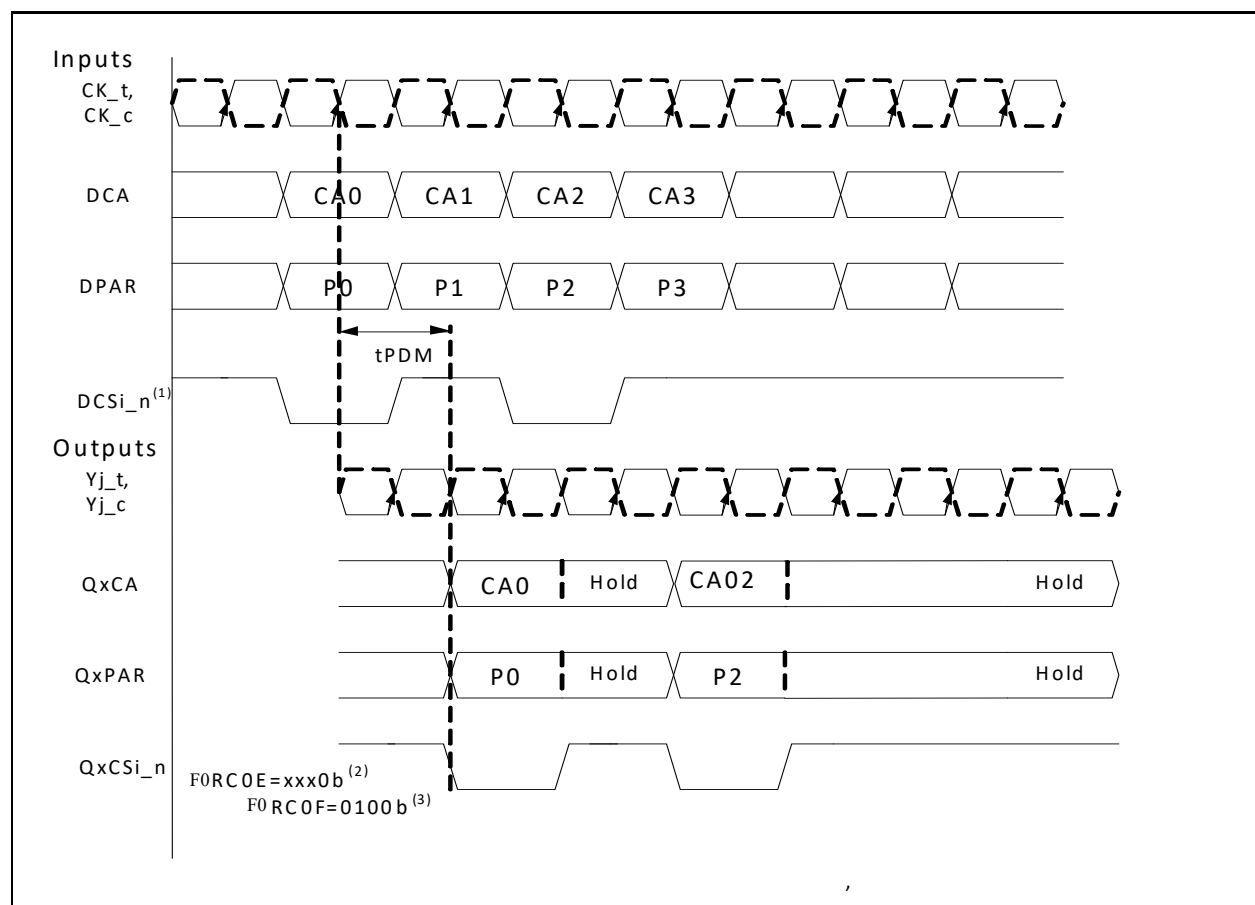
In Figure 5 and Figure 6 both the clock, data and parity input signals as well as the associated output signals are shown to illustrate the effect of the programmable command latency control bits. All other timing diagrams depict

1. However, CMD4 MPR writes to the DRAM that are the result of 'CW Write' commands to F0RC06 are still allowed.

only the input signals and the ALERT_n output.

The DPAR signal arrives one input clock cycle after the corresponding data input signals. ALERT_n is asserted three input clock cycles after the corresponding data is registered. If Parity is enabled and the ALERT_n assertion bit in the **Parity , NV Mode Enable, and ALERT Configuration** Control Word is set, ALERT_n will stay LOW for a minimum of ‘minimum ALERT_n pulse width’ (see Table 47) clock cycles or until DRST_n is driven LOW. If Parity is enabled and the ALERT_n assertion bit in the **Parity , NV Mode Enable, and ALERT Configuration** Control Word is cleared, ALERT_n will be deasserted when a ‘Clear CA Parity Error’ command is received or when DRST_n is driven LOW.

Figure 3 shows the timing diagram with an additional command latency of 0 which requires parity checking to be disabled.



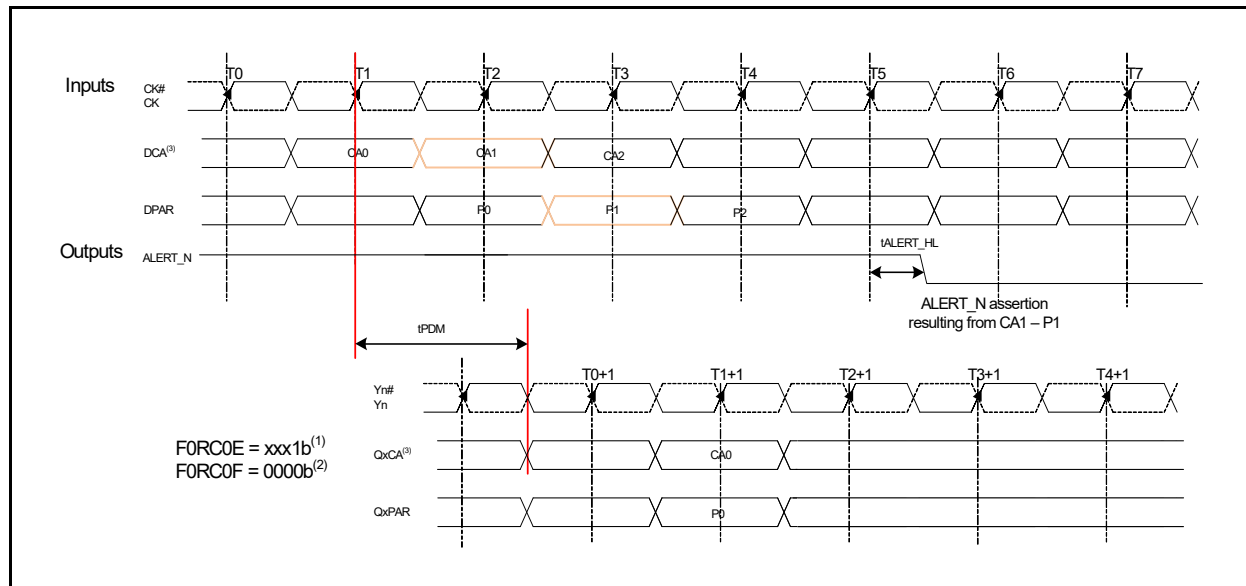
(1) Assuming only one rank selected, all other DCS_x_n are high

(2) Parity checking is disabled

(3) Additional Command latency = 0

Figure 3 — Timing of Clock, Data, and Parity Signals with Parity Checking Disabled

Figure 4 shows the parity diagram with single parity-error occurrence with an additional command latency of 1 and assumes the occurrence of only one parity error when data is clocked in at the T2 input clock cycle (DPAR clocked in on the T3 input clock cycle).



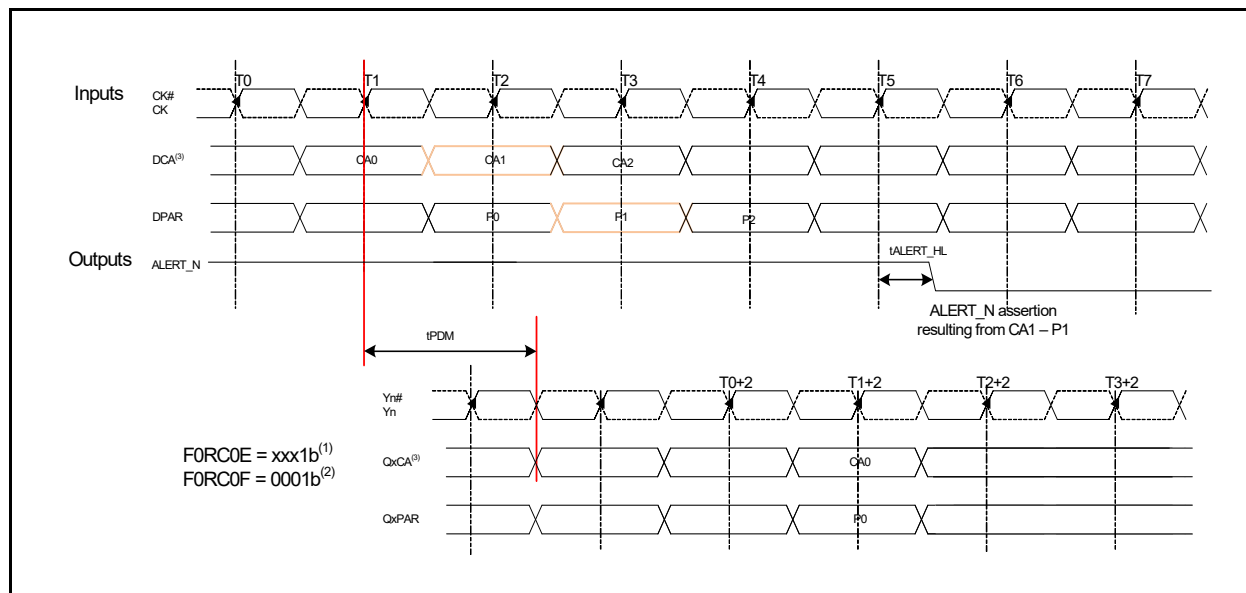
(1) Parity checking is enabled

(2) Additional Command latency = 1

(3) Each command CAx is accompanied by a DCSx_n or QxCSy_n assertion which is not shown for better visibility

Figure 4 — Timing of Clock, Data, and Parity Signals with Checking Enabled and Latency=1

Figure 5 shows the parity diagram with single parity-error occurrence with an additional command latency of 2 and assumes the occurrence of only one parity error when data is clocked in at the T2 input clock cycle (DPAR clocked in on the T3 input clock cycle).



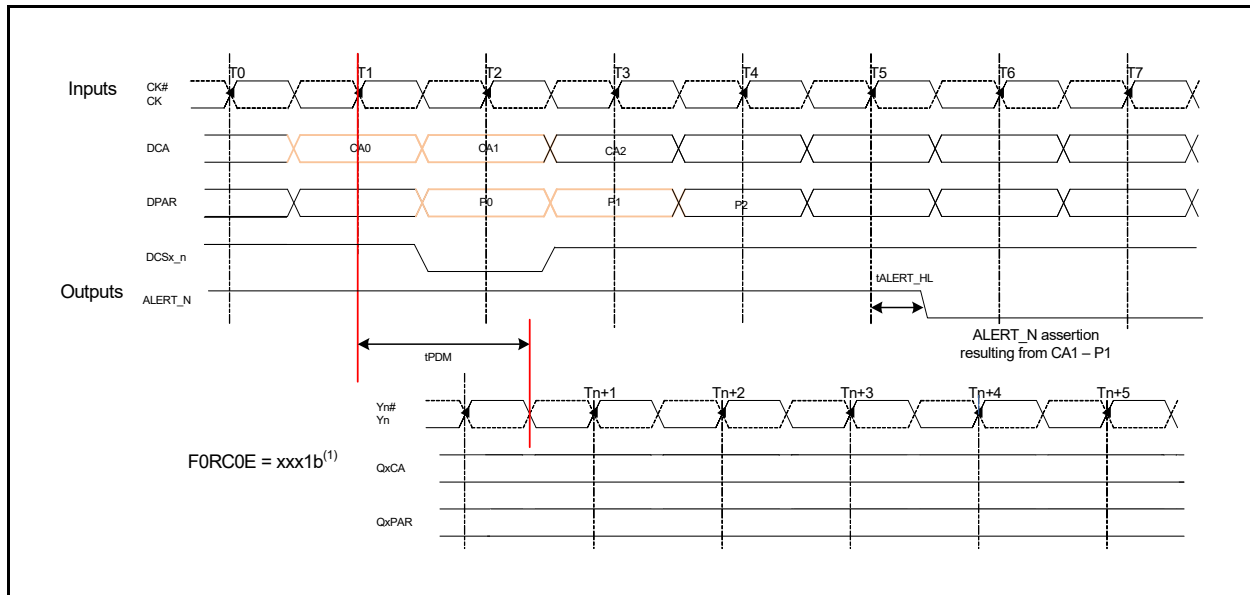
(1) Parity checking is enabled

(2) Additional Command latency = 2

(3) Each command CAx is accompanied by a DCSx_n or QxCSy_n assertion which is not shown for better visibility

Figure 5 — Timing of Clock, Data, and Parity Signals with Checking Enabled and Latency=2

Figure 6 shows the parity diagram with two parity-error occurrences; during chip-deselect and chip-select modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the T1 and T2 input clock cycles (DPAAR clocked in on the T2 and T3 input clock cycles). Parity error in the chip-deselect mode is ignored, but parity error in the chip-select mode is detected.



(1) Parity checking is enabled

Figure 6 — Parity-error Occurrence on Chip-deselect Mode

2.5 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DB). This interface is enabled on power-on and only disabled when the ‘LRDIMM Disable’ bit in the DIMM Configuration Control Word (F0RC0D) is set.

2.5.1 Control Bus Signals

Table 5 — List of Signals for Data Buffer Control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
BVrefCA	Reference voltage output for command and control signals connected to the data buffers	1
Total		9

2.5.2 Control Bus Timing

The output signals BCOM, BODT and BCKE are driven at the same time as the QxCA outputs, i.e. they are affected by the Command Latency Adder Control Word F0RC0F but a latency adder of 0 is not a valid configuration.

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU ¹	Reserved for future use	1110
RFU ¹	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

2.5.3.2 Command Sequences

With the exception of the NOP command, all commands require more than one clock cycle in order to send additional information needed by the buffer in the execution of the command. We call this succession of command and its corresponding data transfers a command sequence. The command sequence for Read or Write commands requires two additional cycles to transfer the rank number corresponding to the write or read command, the sequence for MRS Writes requires seven clock cycles in addition to the basic command, the sequence for the BCW Write command uses six additional clock cycles and the BCW Read command uses five additional clock cycles.

2.5.3.3 Parity Error Checking

Command sequences are protected by a parity checking scheme. Parity checking on the command bus signals is disabled by default, and it is necessary to enable parity checking by writing a buffer configuration bit by using a BCW instruction. The DDR4RCD02 always generates the parity cycles in the BCOM command sequences. Parity checking only applies to the BCOM[3:0] signals. The convention of parity is even parity, i.e. valid parity is defined as

an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. Parity will be checked in accumulated sequential fashion during all the cycles of a command sequence. The parity bit is transmitted for each BCOM[3:0] signal in the corresponding BCOM[3:0] line during the last transfer (clock cycle) in the command sequence.

2.5.3.4 Command Sequence Error Detection

In order to keep the command bus from getting stuck in an out-of-sync situation in terms of the handling of command versus data transfers, a protection scheme is necessary.

Details of the command sequence error detection algorithm are documented in the DDR4 DB specification.

Upon detection of a command sequence error, the DB will assert its ALERT_n output which is assumed to be routed to the ERROR_IN_n input of the RCD, where it causes the assertion of the RCD ALERT_n output.

The RCD will not change its operation in response to the input signal level at the ERROR_IN_n input.

2.5.3.5 Error Handling

The error handler in the host will use the length of the RCD's ALERT_n output pulse to determine what kind of error occurred and if necessary read the error log register of the RCD as well as the error log register of the DDR4 DRAMs and data buffers to determine the source of the error and the specific command that caused the error.

The host may or may not try to recover from the error condition by retrying the affected commands.

2.5.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the DDR4RCD02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$$DB_WL(R)^1 = CWL + AL + PL + DWL(R)$$

$$DB_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$$

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

For the detailed equations for DWL and MRE refer to the DDR4DB02 specification.

The DDR4RCD02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4RCD02 for all ranks and nibbles.

-
1. This equation assumes that the DDR4 data buffer MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/F[3:0]BC9x are at their default power-on setting.
 2. This equation assumes that the DDR4 data buffer MDQS Read Delay Control Words in F[3:0]BC4x/F[3:0]BC5x are at their default power-on setting.

Timing parameters that are integer multiples of tCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tCK are shown in *red italic* letters.

For simplicity the timing diagrams only show one of the possible host interface termination modes and RTT_PARK is never shown even though it is always supported.

2.5.4.1 Write Commands

Table 7 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI.

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 7 shows the timing sequence for a Write command.

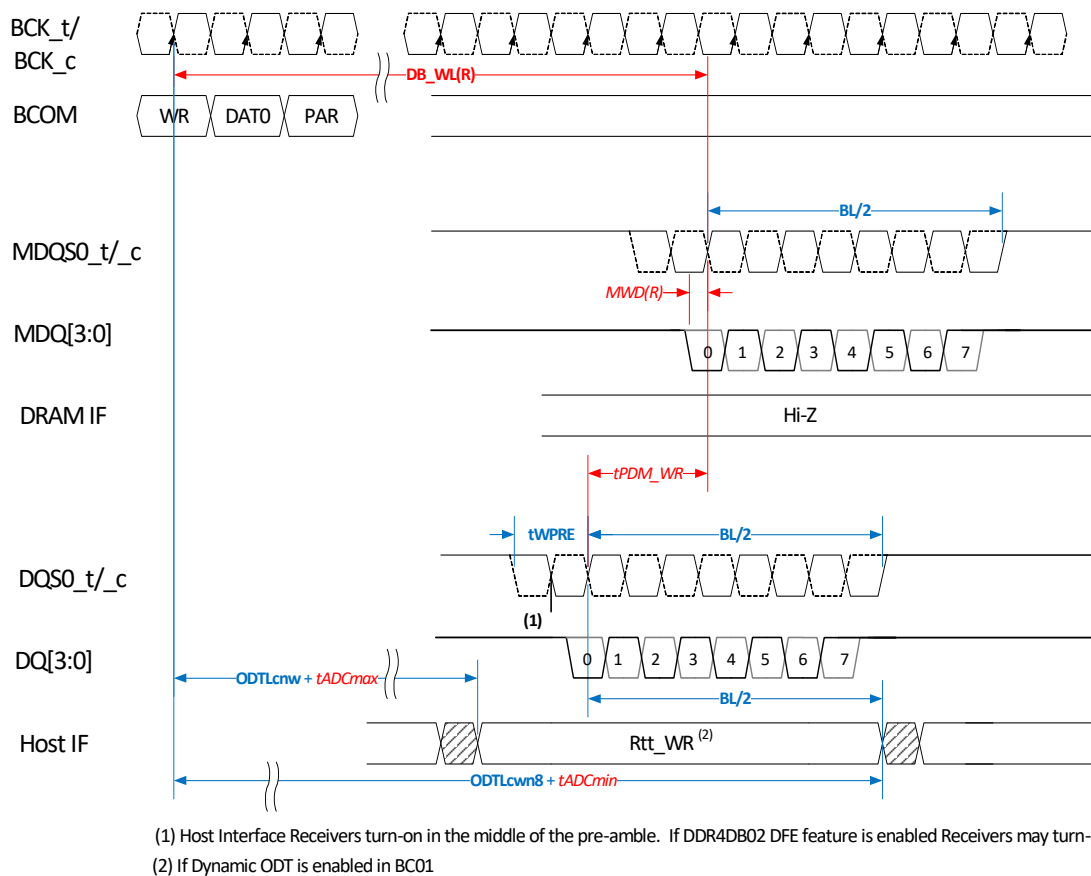


Figure 7 — WRITE Timing

2.5.4.2 Read Commands and MPR Override Reads

Table 8 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 ($A[1:0] = '00'$ or $'10'$).

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 8 shows the timing sequence for a Read command.

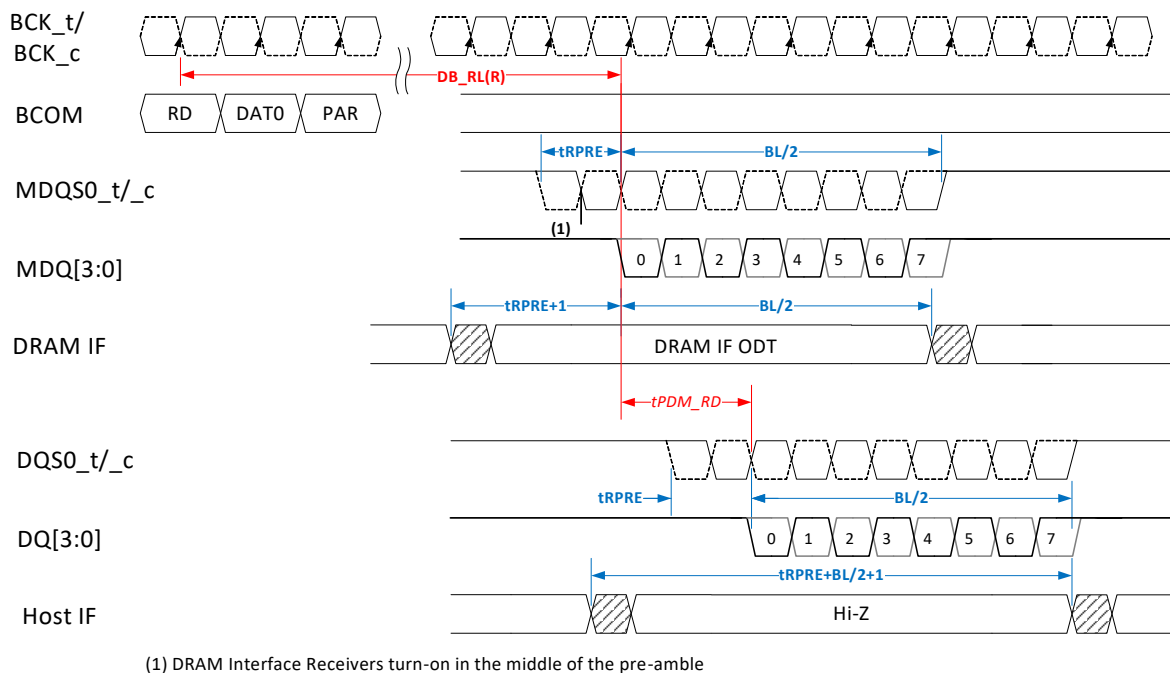


Figure 8 — READ Timing

Read commands can be used to access locations other than the memory array in the DDR4 DRAM devices. These special read commands are MPR override reads which access the MPR locations inside the DB. MPR override mode is configured in the DB. Since there is only one set of MPR registers in the DB, the RCD ignores the rank information

when it sends the Read command to the DB and sends the BA[1:0] bits (indicating which of the three MPR locations are accessed) instead of the rank information in the first data cycle. MPR override reads are only allowed to rank 0, i.e. the RCD never mirrors BA0 and BA1 for MPR override reads.

2.5.4.3 MRS Write Commands

The DDR4RCD02 generates MRS Write commands to the data buffers for each MRS command to the A-side DRAMs (i.e. with BG1 = 0) for rank 0 only. The register does not generate MRS Write commands to the data buffer for MRS commands to the B-side DRAMs (i.e. with BG1='1') or for MSR commands ranks other than 0.

Table 9 shows the sequence for MRS Write commands.

Table 9 — Multicycle Sequence for MRS Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	MRS Write	MRS Write Command BCOM[3:0] = 1011
2	DAT0	MRS ID code BCOM[3:0] = {0, BG0, BA1, BA0}
3	DAT1	First data transfer for MRS Write command BCOM[3:0] = {0, DA2, DA1, DA0}
4	DAT2	Second data transfer for MRS Write command BCOM[3:0] = {0, DA5, DA4, DA3}
5	DAT3	Third data transfer for MRS Write command BCOM[3:0] = {0, DA8, DA7, DA6}
6	DAT4	Fourth data transfer for MRS Write command BCOM[3:0] = {0, DA11, DA10, DA9}
7	DAT5	Fifth data transfer for MRS Write command BCOM[3:0] = {0, 0, DA13, DA12}
8	PAR[3:0]	Even parity bits for MRS Write command and data PAR[x]: parity bit for 7 previous BCOM[x] transfers
9	Next Cmd	Next Command

The sequence for an MRS Write command is shown in Figure 9 below. The timing diagrams show how the MRS Write command is followed by six data transfer cycles and a parity data transfer cycle. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tBCW parameter that indicates the spacing from the MRS Write command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRS Write command also imposes a limitation on how close consecutive MRS Write commands can be issued to the data buffer.

For MRS Write commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in F0RC0D is set to '0' (LRDIMM), the DDR4RCD02 generates a -BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer's host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection. The DB will not capture any MRS bits written in PDA mode.

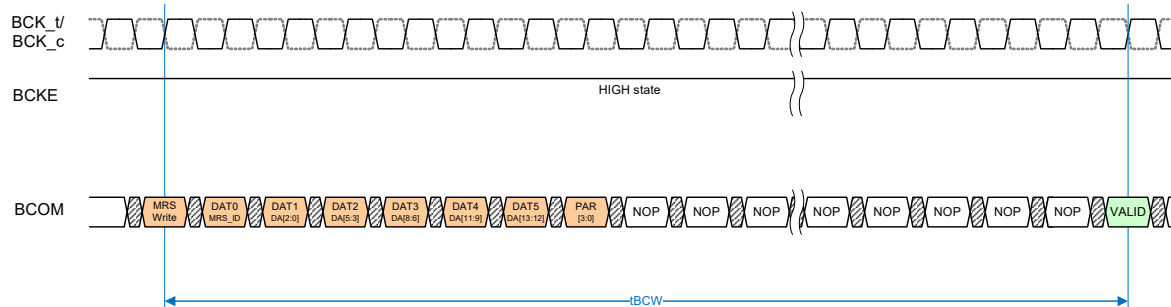


Figure 9 — MRS Write Command Sequence

2.5.4.4 BCW Write Command

Table 10 shows the sequence for buffer control word write commands.

Table 10 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0}
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

The sequence for a BCW Write command is shown in Figure 10 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

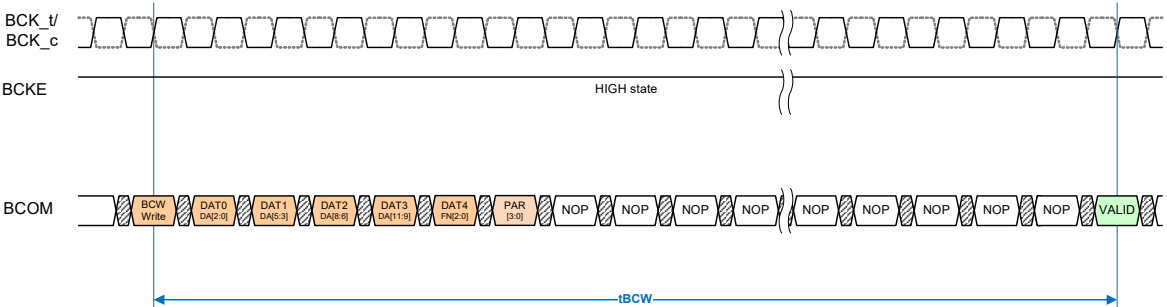


Figure 10 — Buffer Control Word Write Command Sequence

2.5.4.5 BCW Read Commands

The DDR4RCD02 generates a BCW Read command on the buffer control bus when it receives a CW Read command in F0RC06 with A12 = 1.

Table 11 shows the sequence for BCW Read commands.

Table 11 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

The sequence for BCW Read command is shown in Figure 11 below. The timing diagrams show how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR0 override read (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD02 will forward Read command to DRAM but DDR4DB02 will ignore read data from DRAM.

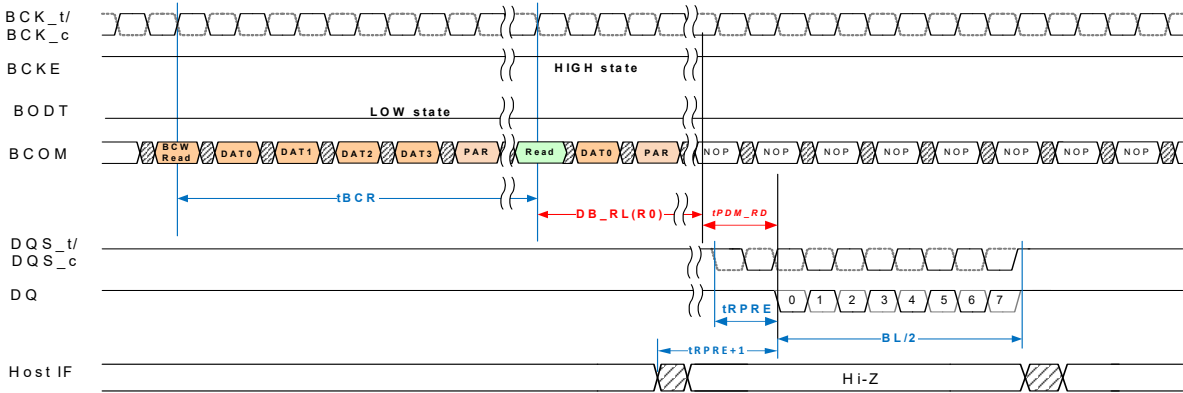


Figure 11 — BCW Read Command Sequence

2.6 DQ Bus Termination in LRDIMM Application

The DDR4RCD02 supports DQ bus termination in LRDIMM applications (i.e. with data buffers connected to it) by providing the BODT output connected to the data buffers.

Unless BODT is turned off in F0RC8x bits DA[5] or DA[7], BODT is the logical OR of the DODT0 and DODT1 inputs, i.e. if one or both of these inputs is asserted HIGH, the BODT output is asserted HIGH.

When BODT is enabled, the host controls enabling RTT_NOM on the host interface of the data buffer through assertion of the DODT signals, which are OR'ed by the RCD, which in turn asserts BODT HIGH or LOW to the data buffer. The enabling/disabling of the on-die termination at the DRAM interface of the data buffer is independent from the BODT input control signal.

The timing for enabling RTT_NOM on the host interface in response to BODT being captured HIGH is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the BODT signal assertion than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

It is the responsibility of the host to assert the DODT signal to the RCD early enough to ensure that the host interface termination is active prior to start of the read preamble at the host interface. The duration of the data buffer's RTT_NOM termination is controlled by the host through the length of the DODT pulse.

Since the data buffer can either drive data or terminate (but not both at the same time), the data buffer disables RTT_NOM at the host interface for reads targeted to this DIMM during the duration of the read burst (including the Read Preamble).

The timing for enabling RTT_WR on the host interface in response to a WRITE command being captured on the BCOM inputs is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the WRITE command capture than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

Figure 12 shows the host interface ODT timing based on the assertion of the input signal BODT. The DDR4DB02 parameters ODTLon, ODTLoff, ODTLcnw, ODTLcwn and tADC are defined in the Electrical and Timing chapter of the Data Buffer Specification. For simplicity this diagram shows ODT timings always aligned with rising clock edges but due to the existence of the fractional cycle delays DB_WL(R) and tPDM_WR or tPDM_WR_RA, this is typically not the case.

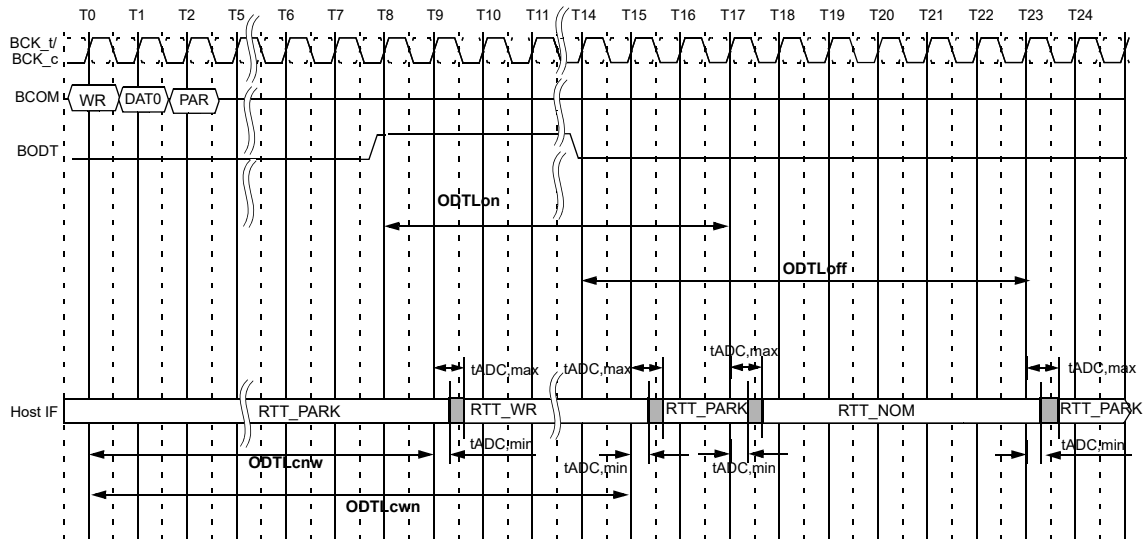


Figure 12 — BODT Timing (Dynamic ODT, 1tCK Preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

$$DB_WL(R) = CWL + AL + PL + DWL(R)$$

$$ODTLon = DB_WL(R^1) - tPDM_WR - tWPRE - 1; \text{ where } tWPRE = 1 \text{ or } 2 \text{ (when F0BC1x DA7 = 0)}$$

$$= DB_WL(R^1) - tPDM_WR_RA - tWPRE - 1; \text{ where } tWPRE = 1 \text{ or } 2 \text{ (when F0BC1x DA7 = 1)}$$

$$ODTLoff = ODTLon$$

$$ODTLcnw = DB_WL(R) - tPDM_WR - tWPRE - 1; \text{ where } tWPRE = 1 \text{ or } 2 \text{ (when F0BC1x DA7 = 0)}$$

$$= DB_WL(R) - tPDM_WR_RA - tWPRE - 1; \text{ where } tWPRE = 1 \text{ or } 2 \text{ (when F0BC1x DA7 = 1)}$$

$$ODTLcwn = ODTLcnw + tWPRE + BL/2 + 1; \text{ where } tWPRE = 1 \text{ or } 2 \text{ and } BL = 4, 8 \text{ or } 10 \text{ with CRC enabled}$$

Unless F0RC8x bit DA[7] = 1, the host also controls the QxODT signals at the DRAM interface directly through the assertion of the two DODT signals at the host interface. The host may utilize non-target termination to a rank on the same DIMM other than the target rank for read transactions. The host may also utilize non-target termination to a rank on the same DIMM other than the target rank for write transactions.

If F0RC8x DA[7:6] = 11, the assertion of the QxODT outputs is caused by the capture of a Write or Read command, controlled by the rules in F0RC9x and F0RCAx respectively. The assertion timing of the QxODT pulse is controlled by F0RC8x bits DA[4:0] and F0RC5x bits DA[3:0]. Table 12 shows the default QxODT[1:0] high times for Write

1. RTT_NOM termination without a coinciding DDR4DB02 data movement (e.g. WR) uses rank 0 timing while RTT_NOM termination with a coinciding data movement will use the timing of the target rank, which implies that the data buffer can dynamically switch between different rank timings from one access to the next.

and Read commands.

Table 12 — Default Write, Read QxODT[1:0]¹ Signal High Time

Operation	Pre-amble	Burst Length	QxODT[1:0] High Time		Unit
			Write CRC Disabled	Write CRC Enabled	
Write	1 nCK	BL8	6	7	nCK
		BC4	4	7	
	2 nCK	BL8	7	8	
		BC4	5	8	
Read	1 nCK	BL8	6		
		BC4	4		
	2 nCK	BL8	7		
		BC4	5		

1. Only applicable if F0RC8x DA[7:6] = 11. Applies to QxODT[1:0] Write and Read patterns that are selected in F0RC9x and RCAx respectively. The DDR4RCD02 is responsible for monitoring DRAM MRS command for Pre-ample, Burst Length and Write CRC setting. The DDR4RCD02 adjusts QxODT[1:0] dynamically if dynamic burst length on the fly function is selected in DRAM. The DDR4RCD02 assumes that all ranks are configured identically for Write/Read Pre-ample, Burst Length and Write CRC and may monitor DRAM MRS commands for only rank 0.

2.7 Power Saving Modes

The device supports different power saving mechanisms.

When both inputs CK_t and CK_c are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACE0, QACE1, QBCE0 and QBCE1 which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]_n must be pulled HIGH to prevent accidental access to the control registers and DCE0 as well as DCE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK_t=CK_c=LOW) will only put the DDR4RCD02 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when DRST_n is driven LOW.

A weak drive feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]_n inputs and weakly drive all outputs corresponding with the chip select gated inputs when all the DCS[n:0]_n inputs are HIGH. If any one of the DCS[n:0]_n input is LOW, the Q_n outputs will function normally.

Once all the DCS[n:0]_n inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCE0, DCE1, DODT0 and DODT1 need to be driven by the system all the time.

The DRST_n input has priority over all other power saving mechanisms. When DRST_n is driven LOW, it will force the Q_n outputs to float, deasserts the open-drain ALERT_n output, forces the QACE0, QACE1, QBCE0 and QBCE1 outputs LOW, disables Input Bus Termination (IBT) and forces BCK_t/BCK_c LOW and BCKE HIGH.

2.7.1 Register CKE Power Down

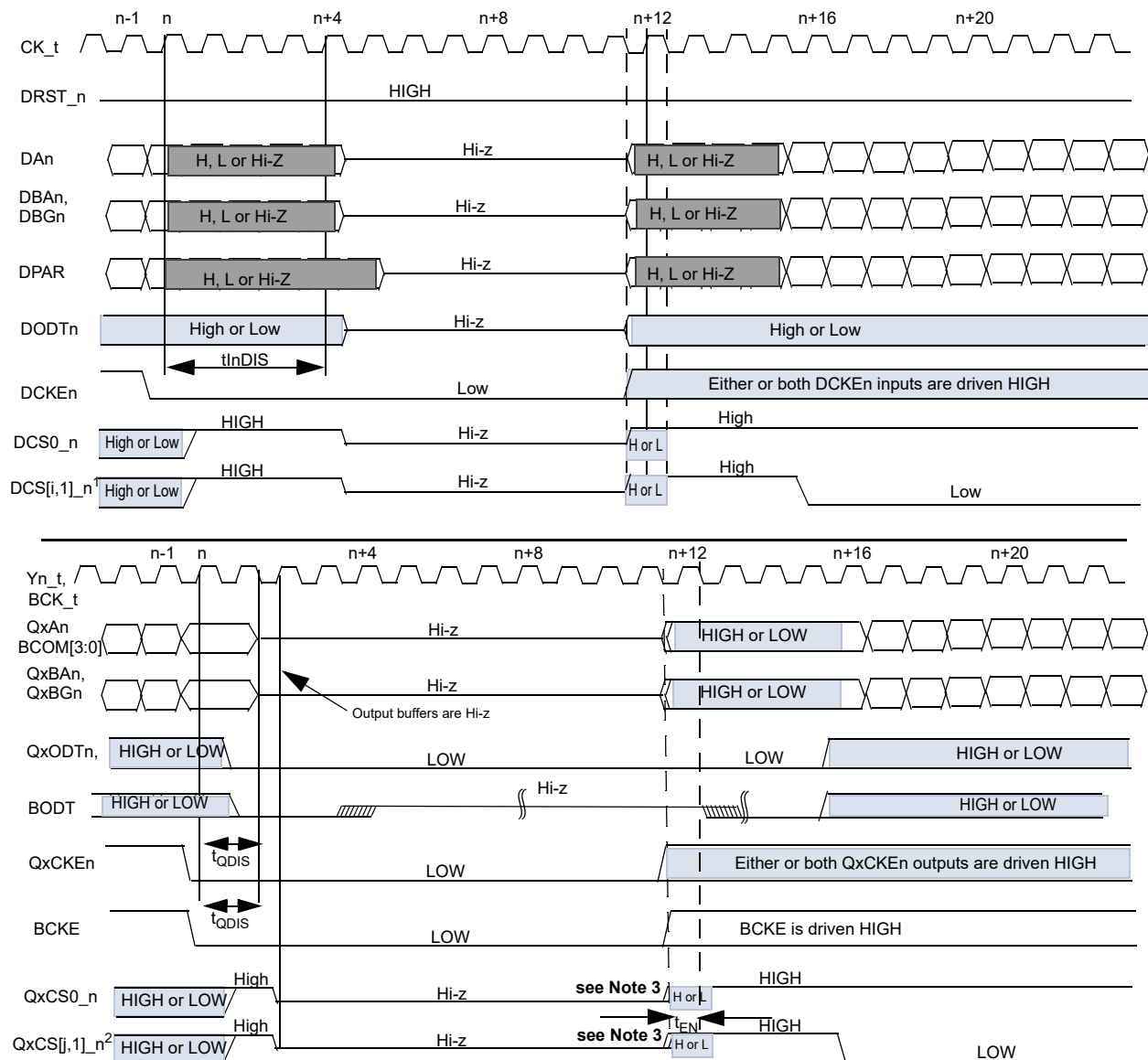
The DDR4RCD02 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to LOW. If either input Chip Select signal, DCS[n:0]_n, is asserted together with DCKEn, the DDR4RCD02 transfers the corresponding command to its outputs together with QxCKEn LOW, after the command latency adder programmed into F0RC0F.

There are two modes of CKE Power Down selected by control word F0RC09. Bit DA2 in F0RC09 indicates whether register turns off IBT or keeps IBT on.

The statements about DODT_n and QxODT_n in the remainder of this section assume that the DODT_n inputs and QxODT_n outputs are enabled in F0RC8x. If a DODT_n input is disabled in F0RC8x, it is always disabled, even in CKE power down mode. If a QxODT_n output is disabled in F0RC8x, it is always disabled, even in CKE power down mode.

2.7.1.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers are disabled except for CK_t/CK_c, DCKEn and DRST_n. Upon entry into CKE Power Down mode with IBT off, IBT will be off on all inputs except DCKEn. The DDR4RCD02 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the DPAR input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS} , the register can tolerate floating input except for CK_t/CK_c, DCKEn and DRST_n. The DDR4RCD02 also disables all its output buffers except for Y_{n_t}/Y_{n_c}, QxODT_n, QxCKEn and BCKE. The Y_{n_t}/Y_{n_c} outputs continue to drive a valid phase accurate clock signal. The QxODT_n, QxCKEn and BCKE outputs are driven LOW. The register output buffers are HI-Z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 13. Note that t_{QDIS} only starts when both QxCKEn outputs are driven low, i.e. it is delayed by the Command Latency Adder (CLA) in F0RC0F.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, $i = 3$.

(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, $j = 3$.

(3) Upon CKE Power Down exit, QxCSy_n may follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and be held HIGH for the remainder of $t_{FixedOutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

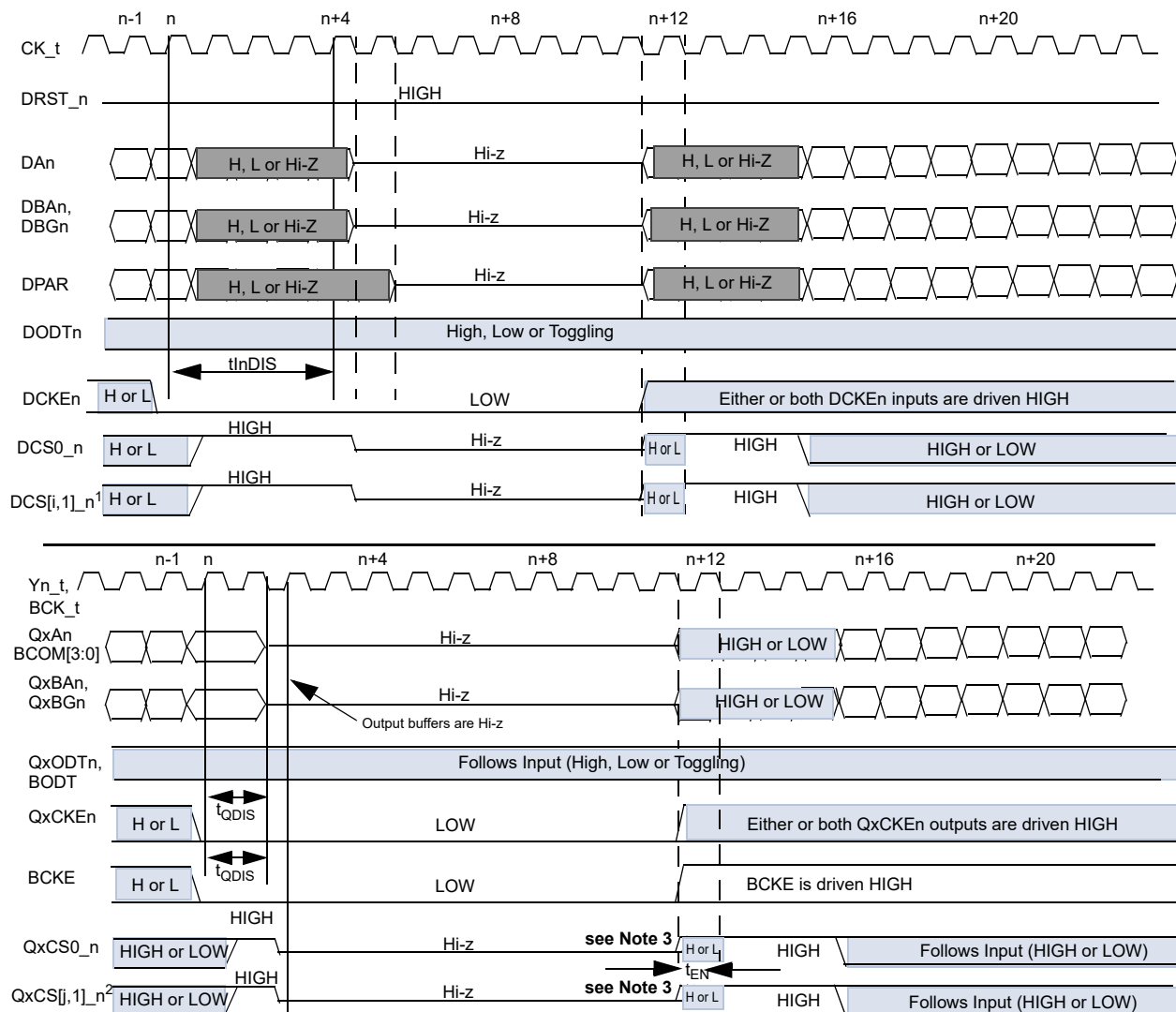
Figure 13 — Power Down Mode Entry and Exit with IBT Off

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately (i.e. without the command latency adder in F0RC0F) starts driving HIGH on the appropriate QxCKEn signals and the BCKE output. The QxCSy_n signals are driven HIGH and QxODTn signals are driven LOW. Other output signals QxA[17:0], QxBA[1:0], QxBG[1:0], QxACT_n, QxC2 and QxPAR are driven either HIGH or LOW to ensure stable

valid logic on all register outputs when QxCKEn goes HIGH. The data buffer communications and control signals BCOM[3:0] are also driven either HIGH or LOW, i.e. at a valid logic level unless F0RC0D DA2 = 1. The register drives output signals to these levels for $t_{\text{Fixedoutput}}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels. BODT is driven LOW during $t_{\text{Fixedoutput}}$ and driven afterwards at the logical OR level of the DODT0 and DODT1 inputs unless F0RC8x DA7 = 1 or DA5 = 1. When exiting CKE power down mode, either one of the Chip select register inputs DCSn_n can be asserted for $\text{CLA} \cdot t_{\text{CK}}$. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn_n can be asserted for $\text{CLA} \cdot t_{\text{CK}}$. The register guarantees that input receivers are stabilized within $t_{\text{Fixedoutput}}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 13.

2.7.1.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down mode with IBT on, all register input buffers are disabled except for CK_t/CK_c , DCKEn, DODTn, ERROR_IN_n and DRST_n. Upon entry into CKE Power Down mode with IBT on, IBT will remain on for all inputs. The DDR4RCD02 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the DPAR input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS} , the register can tolerate floating input except for CK_t/CK_c , DCKEn, DODTn and DRST_n. The DDR4RCD02 also disables all its output buffers except for Yn_t/Yn_c , QxODTn, QxCKEn, BODT and BCKE. The Yn_t/Yn_c outputs continue to drive a valid phase accurate clock signal. The QxCKEn and BCKE outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 14. Note that t_{QDIS} only starts when both QxCKEn outputs are driven low, i.e. it is delayed by the Command Latency Adder (CLA) in F0RC0F.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, $i = 3$.

(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, $j = 3$.

(3) Upon CKE Power Down exit, QxCsY_n may follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and be held HIGH for the remainder of $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCsY_n outputs will follow DCSx_n inputs.

Figure 14 — Power Down Mode Entry and Exit with IBT On

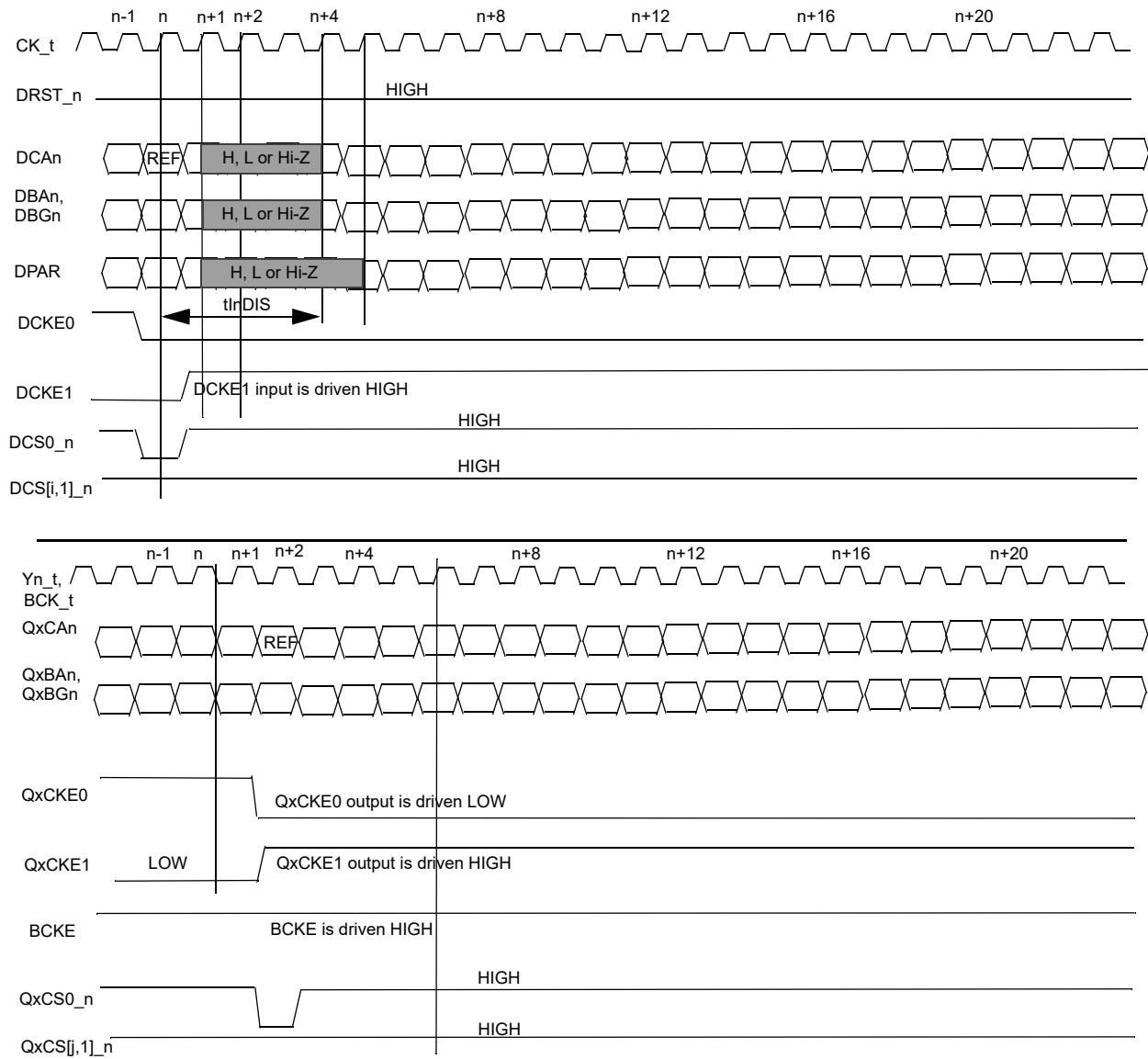
To re-enable the DDR4RCD02 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the DDR4RCD02 immediately (i.e. without the command latency adder in F0RC0F) starts driving HIGH on the appropriate QxCKEn signals and the BCKE output. The QxCsN_n signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxA[17:0], QxBA[1:0], QxBG[1:0], QxACT_n, QxC2 and QxPAR are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The data buffer communications and control signals BCOM[3:0] are also driven either HIGH or LOW, i.e. at a valid logic level unless F0RC0D DA2 = 1. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels.

BODT is driven at the logical OR level of the DODT0 and DODT1 inputs unless F0RC8x DA7 = 1 or DA5 = 1. When exiting CKE power down mode, either one of the Chip select register inputs DCSn_n can be asserted for $CLA \cdot t_{CK}$. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn_n can be asserted for $CLA \cdot t_{CK}$. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 14.

The previous diagrams showed CKE power down entry and exit with a Command Latency Adder (CLA) of 0. With a non-zero CLA the CKE power down mode entry is delayed by $CLA \cdot t_{CK}$ w.r.t. the RCD outputs, i.e. the outputs are tristated later. The delay caused by CLA also applies to the DRAM Power Down Entry (PDE) and Self Refresh Entry (SRE) since both commands as well as the falling CKE edge are delayed on the RCD outputs. Input disable is just based on the DCKEn timing, i.e. the inputs are disabled at the same time as without a command latency adder. Power down mode exit is also based on the DCKEn inputs, i.e. the RCD CKE power down mode exit (as well as the DRAM Power Down Exit and Self Refresh Exit) is not delayed by CLA. Therefore special consideration needs to be given to the case when the duration of the RCD CKE power down mode is less than the Command Latency Adder CLA, i.e. when the LOW overlap between DCKE0 and DCKE1 is less or equal than CLA. This case is shown in Figure 15 which depicts single cycle LOW overlap between DCKE0 and DCKE1 with a Command Latency Adder of 1.

Since forwarding the rising edge of CKE is not delayed by CLA, there is no LOW overlap between QxCKE0 and QxCKE1 and hence the output side of the RCD never enters power down mode. However, the inputs of the RCD start to disable when registering both DCKE inputs LOW in the same cycle. During $t_{Fixedoutput}$ (which is triggered by the rising edge of one of the DCKE inputs), the RCD is required to follow all inputs for the duration of CLA. This ensures that any commands the RCD captures while both DCKE inputs are sampled LOW are forwarded to the outputs.

The duration of $t_{Fixedoutput}$ depends on CLA which ensures that the RCD holds the QxCsSy_n outputs HIGH during the last few cycles of $t_{Fixedoutput}$ which correspond to the time when the RCD inputs may have been disabled.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, $i = 3$.

(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, $j = 3$.

(3) Upon CKE Power Down exit, QxCSy_n must follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and then be held HIGH for the remainder of $t_{\text{FixedOutput}}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

Figure 15 — Single Cycle Power Down Mode Entry and Exit with CLA=1

2.7.2 Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Y_n clocks to float, the DDR4RCD02 supports a Clock Stopped power down mode. When both inputs CK_t and CK_c are being held LOW (i.e. below V_{IL} (static)) or float (when they will eventually settle at LOW because of the 10 k Ω to 100 k Ω pull-down resistor in the CK_t/CK_c input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirements are shown in Figure 16, “Clock Stopped Power Down Entry and Exit with IBT On” and Figure 17, “Clock Stopped Power Down Entry and Exit with IBT Off”. The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0, QBCKE1, BCK_t/BCK_c and BCKE (which must be kept driven LOW) unless the buffer control bus is disabled in F0RC0D. The device deasserts the open-drain ALERT_n output in clock stopped power down mode. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0, QxCKE1, BCK_t/BCK_c and BCKE can be disabled.

2.7.2.1 Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, DCKEn will be deasserted for a minimum of one tCKoff before pulling CK_t and CK_c LOW. After holding CK_t and CK_c LOW (i.e. below V_{IL} (static)) for at least one tCKEV, both CK_t and CK_c can be floated. Because of the 10 k Ω to 100 k Ω pull-down resistor in the CK_t/CK_c input buffer, CK_t/CK_c will stay at LOW even though they are not being driven. The register is now in Clock Stopped Power Down mode. If the buffer control bus is enabled in F0RC0D, the RCD drives BCK_t/BCK_c and BCKE LOW while in Clock Stopped Power Down mode. After CK_t and CK_c are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can be floated. At this point, all input receivers and input termination of the DDR4RCD02 are disabled. The only active input circuits are CK_t and CK_c , which are required to detect the wake up request from the host.

2.7.2.2 Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS0_n must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. The state of the DCS[n:0]_n inputs must not be changed before the end of tSTAB. The input clock CK_t/CK_c must be stable for a time equal or greater than tSTAB before any access to the DDR4RCD02 can take place.

If the buffer control bus is enabled in F0RC0D, the RCD drives BCKE, BCK_t and BCK_c LOW during tSTAB.

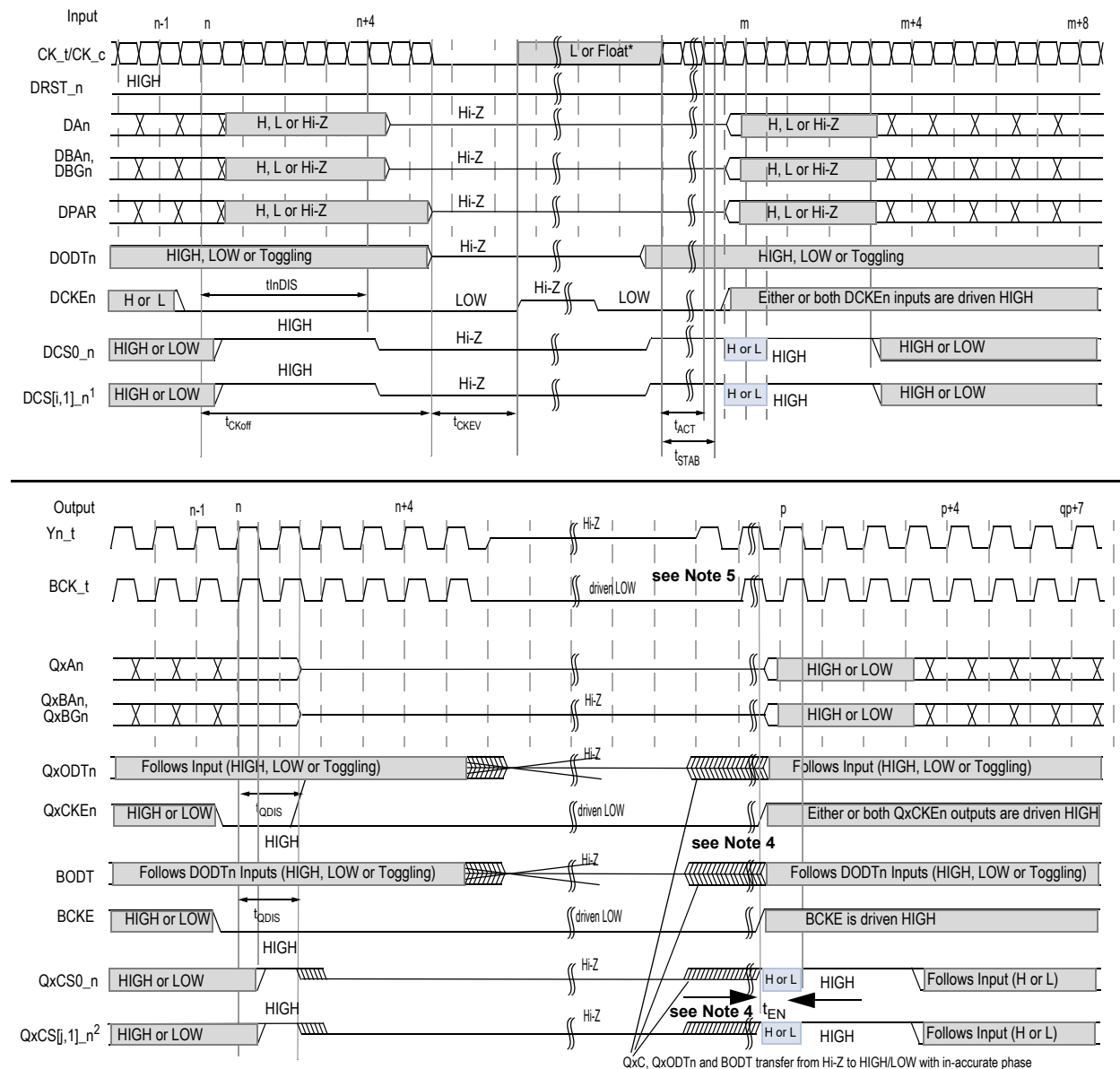


Figure 16 — Clock Stopped Power Down Entry and Exit with IBT On