

# **JEDEC STANDARD**

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## **DDR4 Data Buffer Definition (DDR4DB01)**

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### **JESD82-32**

**NOVEMBER 2016**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## DDR4 DATA BUFFER DEFINITION (DDR4DB01)

(From JEDEC Board Ballot JCB-14-12, formulated under the cognizance of the JC-40.4 Subcommittee on Registered & Fully Buffered Memory Support Logic.)

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### 1 Scope

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This standard defines standard specifications for features and functionality, DC and AC interface parameters and test loading for definition of the DDR4 data buffer for driving DQ and DQS nets on DDR4 LRDIMM applications. Any TBDs as of this document, are under discussion by formulating committee.

The purpose is to provide a standard for the DDR4DB01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR4DB01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

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### 2 Device standard

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#### 2.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V  $V_{DD}$  operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are  $V_{DD}$  terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR4DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK\_t and BCK\_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers. The buffer control word (BCW) mechanism is described in more detail in 2.5.

The DDR4DB01 also supports dedicated pins for ZQ calibration and for parity error alerts.

##### 2.1.1 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of 200  $\mu$ s in the RESET state (i.e., the BCK\_t/BCK\_c inputs are held LOW and the BCKE input is held HIGH). In the RESET state all other input receivers are disabled, and can be left floating. In the RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All outputs must float. In the RESET state the data buffer is in low power state and host interface or DRAM interface termination is disabled.

With a falling edge of the BCKE input, the data buffer transitions to the clock stopped power down mode. A certain period of time ( $t_{ACT}=16 t_{CK}$ ) before the BCKE input is pulled LOW the reference voltage BVrefCA needs to be stable within specification.

With stable clock input signals BCK\_t/BCK\_c and BCKE still held LOW, the buffer transitions into the equivalent of CKE power down mode.

### 2.1.1.1 Clock Stabilization Time $t_{DLLK}$

During DLL stabilization time  $t_{DLLK}$  the data buffer is not fully operational. In ensure correct operation, some rules apply to the inputs of the buffer:

- BCKE must remain LOW.
- BODT is kept at a stable valid logic level.

These rules apply to any instance where stabilization time  $t_{DLLK}$  is required:

- Exit from Reset state
- Exit from clock stop power down
- Changing clocking related registers
- Changing input clock frequency during boot or run time

Since the data buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the DLL stabilization time ( $t_{DLLK}$ ) the DB must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs.

### 2.1.1.2 Reset Initialization with Stable Power

The timing diagram depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. The data buffer remains in the RESET state for a minimum of  $16 * t_{CK}$  (i.e., BCK\_t/BCK\_c are held LOW (i.e., below  $V_{IL(static)}$ ) and BCKE input is held HIGH for that long).

After initialization, the host needs to write to those control registers in the RCD and DB whose contents need to be changed before it can proceed to the DRAM initialization.

## 2.1.2 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB01).

### 2.1.2.1 Control Bus Signals

**Table 1 — List of Signals for Data Buffer control**

| Name         | Description                                                | Signal Count |
|--------------|------------------------------------------------------------|--------------|
| BCOM[3:0]    | Data buffer command signals                                | 4            |
| BCKE         | Function of registered DCKE (dedicated non-encoded signal) | 1            |
| BODT         | Function of registered DODT (dedicated non-encoded signal) | 1            |
| BCK_t, BCK_c | Input clock                                                | 2            |
| BVrefCA      | Reference voltage for command and control signals          | 1            |
| <b>Total</b> |                                                            | <b>9</b>     |

### 2.1.2.2 Command List

**Table 2 — DDR4 Data Buffer Command Table**

| Command          | Description                                                                                                                                                                                     | BCOM[3:0]<br>Encoding |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| WR               | Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot. | 1000                  |
| RD               | Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.                             | 1001                  |
| MRS Write        | Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.                                          | 1011                  |
| BCW Write        | Write buffer control word data in the next five command slots, followed by parity in the last command time slot.                                                                                | 1100                  |
| BCW Read         | Read buffer control word address in the four command slots, followed by parity in the last command time slot.                                                                                   | 1101                  |
| RFU <sup>1</sup> | Reserved for future use                                                                                                                                                                         | 1110                  |
| RFU <sup>1</sup> | Reserved for future use                                                                                                                                                                         | 1111                  |
| NOP              | Idle, do nothing                                                                                                                                                                                | 1010                  |
|                  |                                                                                                                                                                                                 |                       |

1. RFU commands are treated as NOP commands for command sequence error detection

### 2.1.3 Dedicated Signals

BCKE, BODT, and BCK\_t/BCK\_c are considered dedicated signals because they have direct control of certain commands and/or modes of operation. The following sections describe how the dedicated signals are used.

#### 2.1.3.1 CKE Power Down with ODT enabled Entry

The data buffer enters into a power saving state when its BCKE input transitions from high to low if BC09 DA3 = 1. The DB enters CKE Power Down mode with ODT enabled if BC09 DA2 = 0. The event is captured by the data buffer device synchronously with the BCK\_t/BCK\_c input clock. In this power saving state, most input receivers and all output drivers in the data buffer are disabled. Similarly, any internal non-essential circuits can be powered down in this mode. The input receivers that need to remain enabled are BCK\_t/BCK\_c, BCKE and BODT. The data buffer device disables input receivers within tInDIS clocks after latching the BCKE inputs LOW. After tInDIS, the data buffer can tolerate floating inputs except for BCK\_t/BCK\_c, BODT and BCKE. Since the data buffer control signals will be terminated to  $V_{TT}$  in the DDR4 LR-DIMM board, the register device will need to disable all unused data buffer control output drivers to avoid wasting power when the data buffers are in the CKE Power Down state. It is required that data buffer clock signal (BCK\_t/BCK\_c) will continue toggling at a stable phase and frequency during CKE Power Down mode in order to allow the data buffer devices to remain locked to this clock.

#### 2.1.3.2 CKE Power Down with ODT disabled Entry

The data buffer enters into a power saving state when its BCKE input transitions from high to low if BC09 DA3 = 1. The DB enters CKE Power Down mode with ODT disabled if BC09 DA2 = 1. The event is captured by the data buffer device synchronously with the BCK\_t/BCK\_c input clock. In this power saving state, most input receivers and all output drivers in the data buffer are disabled. Similarly, any internal non-essential circuits can be powered down in this mode. The input receivers that need to remain enabled are BCK\_t/BCK\_c and BCKE. The BODT input receiver is disabled in this mode. The data buffer device disables input receivers within tInDIS clocks after latching the BCKE inputs LOW. After tInDIS, the data buffer can tolerate floating inputs except for BCK\_t/BCK\_c, and BCKE. Since the data buffer control signals will be terminated to  $V_{TT}$  in the DDR4 LR-DIMM board, the register device will need to disable all unused data buffer control output drivers to avoid wasting power when the data buffers are in the CKE Power Down state. It is required that data buffer clock signal (BCK\_t/BCK\_c) will continue toggling at a stable phase and frequency during CKE Power Down mode in order to allow the data buffer devices to remain locked to this clock.

#### 2.1.3.3 CKE Power Down with ODT enabled Exit

When BCKE is driven from low to high by the register and the data buffer captures this event synchronously with the BCK\_t/BCK\_c input clock, the buffer exits its CKE Power Down mode. When BCKE is driven from LOW to HIGH by the register, it is required that valid logic levels are driven at all the data buffer inputs and that these levels be held constant for  $t_{Fixedoutput}$  to allow input receivers to stabilize. During the  $t_{Fixedoutput}$  window, it is required that the command driven to the data buffer is a NOP (BCOM[3:0] = 1010). After the input receivers are stabilized, the data buffer will start processing commands in its normal operation mode with the correct latency and timing.

#### 2.1.3.4 CKE Power Down with ODT disabled Exit

When BCKE is driven from low to high by the register and the data buffer captures this event synchronously with the BCK\_t/BCK\_c input clock, the buffer exits its CKE Power Down mode. When BCKE is driven from LOW to HIGH by the register, it is required that valid logic levels are driven at all the data buffer inputs and that these levels be held constant for  $t_{Fixedoutput}$  to allow input receivers to stabilize. During the  $t_{Fixedoutput}$  window, it is required that the command driven to the data buffer is a NOP (BCOM[3:0] = 1010) and that the BODT signal is constantly driven LOW. After the input receivers are stabilized, the data buffer will start processing commands in its normal operation mode with the correct latency and timing. This also applies to BODT-controlled termination enable/disable events.

### 2.1.3.5 Clock Stopped Power Down Entry

To support ACPI S3 Power Management mode, the data buffer supports a Clock Stopped Power Down mode. When both inputs BCK\_t and BCK\_c are held at LOW ( $V_{IL}$  (static)) the data buffer device stops operation and enters low-power static and standby operation. The device will stop its internal clock circuits and it will float all outputs drivers and disable all input receivers.

To enter Clock Stopped Power Down mode, the device will first enter CKE Power Down mode. Once in CKE Power Down mode, BCKE will continue be driven to LOW, followed by BCK\_t and BCK\_c also driven LOW. The device is now in Clock Stopped Power Down mode. In this mode all input receivers and input termination of the data buffer will be disabled. The only input circuits that need to remain active are BCK\_t/BCK\_c and BCKE, which are required to detect the wake up request from the register or a RESET condition.

### 2.1.3.6 Clock Stopped Power Down Exit

To wake up the data buffer from its Clock Stopped Power Down mode, the data buffer BCKE input must continued to be driven LOW to ensure that the data buffer device goes into CKE Power Down mode immediately after exiting Clock Stopped Power Down mode. If Clock Stopped Power Down mode had been entered from CKE Power Down with the host ODT termination feature enabled, it is also necessary for BODT to be driven to LOW before the data buffer is taken out of Clock Stopped Power Down mode. After that, a frequency and phase accurate input clock signal must be applied. The state of the BCKE and BDODT input signals must not be changed before the end of the DLL stabilization time (tDLLK). If Clock Stopped Power Down mode had been entered from CKE Power Down with host ODT termination disabled, the host interface DQ termination is disabled until the end of tDLLK and from then on works with synchronous timing and deterministic latency. The input clock BCK\_t and BCK\_c must be stable for a time equal or greater than tDLLK before any access to the data buffer can take place. During DLL stabilization time the BCKE signal need to be kept at LOW level.

### 2.1.3.7 Host Interface ODT Termination

The DDR4DB01 supports DQ bus termination in LRDIMM applications by providing the BODT input connected to the DDR4RCD01.

Unless BODT is turned off in RCD RC8x bits DA[5] or DA[7], BODT is the logical OR of the RCD DODT0 and DODT1 inputs, i.e., if one or both of these inputs is asserted HIGH, the RCD BODT output is asserted HIGH.

When BODT is enabled, the host controls enabling RTT\_NOM on the host interface of the data buffer through assertion of the DODT signals, which are OR'ed by the RCD, which in turn asserts BODT HIGH or LOW to the data buffer. The enabling/disabling of the on-die termination at the DRAM interface of the data buffer is independent from the BODT input control signal.

The timing for enabling RTT\_NOM on the host interface in response to BODT being captured HIGH is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the BODT signal assertion than the latency for enabling the host interface DQS\_t/DQS\_c receivers after a WRITE command is received, depending on the length of the write preamble.

It is the responsibility of the host to assert the DODT signal to the RCD early enough to ensure that the host interface termination is active prior to start of the read preamble at the host interface. The duration of the data buffer's RTT\_NOM termination is controlled by the host through the length of the DODT pulse.

Since the data buffer can either drive data or terminate (but not both at the same time), the data buffer disables RTT\_NOM at the host interface for reads targeted to this DIMM during the duration of the read burst (including the Read Preamble).

### 2.1.3.7 Host Interface ODT Termination (cont'd)

The timing for enabling RTT\_WR on the host interface in response to a WRITE command being captured on the BCOM inputs is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the WRITE command capture than the latency for enabling the host interface DQS\_t/DQS\_c receivers after a WRITE command is received, depending on the length of the write preamble.

Figure 1 shows the host interface ODT timing based on the assertion of the input signal BODT. The DDR4DB01 parameters ODTLon, ODTLoff, ODTLcnw, ODTLcwn and tADC are defined in the Electrical and Timing chapter. For simplicity this diagram shows ODT timings always aligned with rising clock edges but due to the existence of the fractional cycle delays DB\_WL(R) and tPDM\_WR or tPDM\_WR\_RA, this is typically not the case.

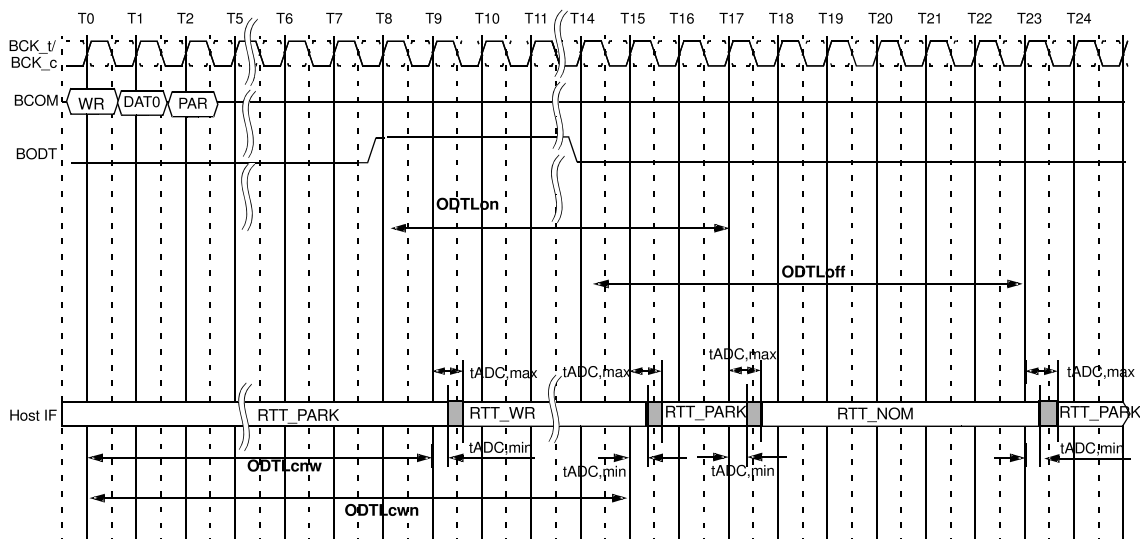


**Figure 1 — Host Interface ODT Timing**

$$DB\_WL(R) = CWL + AL + PL + DWL(R)$$

$$ODTLon = DB\_WL(R^1) - tPDM\_WR - tWPRES - 1; \text{ where } tWPRES = 1 \text{ or } 2 \text{ (when } F0BC1x \text{ DA7} = 0)$$

$$= DB\_WL(R^1) - tPDM\_WR\_RA - tWPRES - 1; \text{ where } tWPRES = 1 \text{ or } 2 \text{ (when } F0BC1x \text{ DA7} = 1)$$

$$ODTLoff = ODTLon$$

$$ODTLcnw = DB\_WL(R) - tPDM\_WR - tWPRES - 1; \text{ where } tWPRES = 1 \text{ or } 2 \text{ (when } F0BC1x \text{ DA7} = 0)$$

$$= DB\_WL(R) - tPDM\_WR\_RA - tWPRES - 1; \text{ where } tWPRES = 1 \text{ or } 2 \text{ (when } F0BC1x \text{ DA7} = 1)$$

$$ODTLcwn = ODTLcnw + tWPRES + BL/2 + 1; \text{ where } tWPRES = 1 \text{ or } 2 \text{ and } BL = 4, 8 \text{ or } 10 \text{ with CRC enabled}$$

Unless DDR4RCD01 RC8x bit DA[7] = '1', the host also controls the QxODT signals at the DRAM interface directly through the assertion of the two DODT signals at the host interface. The host may utilize non-target termination to a rank on the same DIMM other than the target rank for read transactions. The host may also utilize non-target termination to a rank on the same DIMM other than the target rank for write transactions.

1. RTT\_NOM termination without a coinciding DDR4DB01 data movement (e.g., WR) uses Rank 0 timing while RTT\_NOM termination with a coinciding data movement will use the timing of the target rank, which implies that the data buffer can dynamically switch between different rank timings from one access to the next.

### 2.1.3.8 DRAM Interface ODT Termination

The timing for enabling/disabling the on-die termination circuits at the DRAM interface of the DDR4 data buffer is independent from the BODT input control signal. Instead, the hardware in the data buffer will enable the DRAM interface termination within the clock cycle preceding the MDQS preamble during data transactions resulting from DRAM Read commands. This timing is controlled by the DB hardware using the trained DRAM interface receive enable control word settings stored in F[3:0]BC2x and F[3:0]BC3x.

### 2.1.4 Dual Frequency Support

The DDR4DB01 supports operation at a second, i.e., lower than nominal, frequency as a means to save RCD/DB and DRAM power when the memory bandwidth demand allows.

To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR4DB01 can be trained twice at two different frequencies at boot up time and retain register settings associated with each of the two frequencies. See 2.5.12 for a complete list of control words that are duplicated to support dual frequency context switching. The DDR4DB01 hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed.

Switching between the two frequency contexts is achieved by writing to control word BC0A bit DA3. DA3='0' selects the default frequency context 1 while DA3='1' selects frequency context 2.

Dual frequency training at boot up time requires selecting the appropriate frequency context, performing the training at that frequency and then selecting the other frequency context and performing the training at the other frequency. Subsequently, every time the operation frequency changes, the corresponding frequency context bit must be set in the DDR4DB01 via control word writes to BC0A and F0BC6x. The control word write to BC0A/F0BC6x must be the last access to the DB before the input frequency on the BCK\_t/BCK\_c pins changes. See 2.1.5 for the exact sequence of steps for an input frequency change to an LRDIMM.

### 2.1.5 Input Clock Frequency Change

Once the DDR4DB01 is initialized, the DDR4DB01 requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Clock stop power down mode. The complete sequence of input clock frequency change for the DDR4RCD01 and DDR4DB01 is as follows:

1. Disable CKE power down mode in RCD (i.e., write to RC09, bit 3 = '0').
2. Ensure CKE power down mode in DB is enabled (i.e., BC09, bit 3 = '1').
3. Send new BC0A and F0BC6x frequency setting to DB. The DB will defer the application until the next rising edge of BCKE.
4. Put the DRAMs into Self Refresh by sending SRE commands to all ranks. After this step all DCKE inputs will be LOW but the RCD will stay active. The DB will enter CKE power down mode.
5. Send new RC0A and RC3x frequency setting to RCD without asserting CKE. The control word writes will proceed because RCD is still active. DRAMs are still in Self Refresh. No additional commands to the RCD are allowed after this step (until step 8).
6. Host changes frequency by going through Clock Stopped mode. Both CK inputs need to be driven LOW (i.e., below  $V_{IL(static)}$ ) for a minimum of  $t_{CKEV}$  before the clock frequency may change. The DDR4DB01 input clock frequency is allowed to change only within range between the minimum and maximum application or test frequencies specified in Table 116.
7. The DCKE inputs must be held at stable LOW levels during  $t_{CKEV}$  and during the  $t_{STAB}$  time after the clock signals are restarted.
8. Assert DCKE and exit DRAM Self Refresh.
9. Wait  $t_{DLLK}$  for DB clocks to stabilize.
10. Depending on the new clock frequency, additional MRS commands to the DRAM may need to be issued to appropriately set CL, AL, and CWL with BCKE continuously registered high. RCD CKE power down mode may be re-enabled.

### 2.1.6 Command Sequences

With the exception of the NOP command, all commands require more than one clock cycle in order to send additional information needed by the buffer in the execution of the command. We call this succession of command and its corresponding data transfers a command sequence. The command sequence for Read or Write commands requires two additional cycles to transfer the rank number corresponding to the write or read command, the sequence for MRS Writes requires seven clock cycles in addition to the basic command, the sequence for the BCW Write command uses six additional clock cycles and the BCW Read command uses five additional clock cycles.

#### 2.1.6.1 Parity Checking

Command sequences are protected by a parity checking scheme. Parity checking on the command bus signals is disabled by default, and it is necessary to enable parity checking by writing a buffer configuration bit by using a BCW instruction. The RCD always generates the parity cycles in the BCOM command sequences. Parity checking only applies to the BCOM[3:0] signals. The convention of parity is even parity, i.e., valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. . The parity bit is transmitted for each BCOM[3:0] signal in the corresponding BCOM[3:0] line during the last transfer (clock cycle) in the command sequence.

#### 2.1.6.2 Command Sequence Error Detection

In order to keep the command bus from getting stuck in an out-of-sync situation in terms of the handling of command versus data transfers, a protection scheme is necessary.

To implement the command sequence protection scheme, one of the command pins of the bus will be dedicated as a flag to identify the type of transfer. BCOM[3] will be used to indicate if the transfer is a command transfer (BCOM[3] = 1) or a data transfer (BCOM[3] = 0). There is only one exception where BCOM[3] loses this special meaning. That is during the cycles when the four-bit command parity word is transferred from the register to the buffers.

The data buffer will check the value of BCOM[3] every clock cycle, with the exception of parity transfers (PAR[3:0]), and it will detect any errors in the command sequences. An error in the command sequence occurs if any of the following cases is detected.

1. The buffer receives a command transfer (BCOM[3] = 1) when expecting to receive a data transfer (BCOM[3] = 0).
2. The buffer receives a data transfer (BCOM[3] = 0) when expecting to receive a command transfer (BCOM[3] = 1).

### 2.1.6.3 Error Handling

When a BCOM parity error is detected, the data buffer will take the following actions.

1. The data buffer logs all the bits of the erroneous command in the Error Log Register (F7BC0x .. F7BC3x) if there is no previous (parity or command sequence) error already logged in these registers and sets the parity error bit to '1'.
2. BCOM parity checking will be disabled.
3. If the parity error is detected during a configuration command (BCW Write or MRS Write), the state of the buffer configuration bits will not be modified. In other words, the configuration command will not be executed.
4. All scheduled RD/WR commands that have not yet executed are dropped
5. The data buffer will assert the ALERT\_n output pin LOW for tPAR\_ALERT\_PW clock cycles in a similar way as the DDR4 DRAM responds to CA parity errors. If an error occurs ALERT\_n is driven LOW with the third input clock edge after the corresponding incorrect data were captured on the data buffer command inputs. If BC0E DA2='1', ALERT\_n goes to high impedance with the tPAR\_ALERT\_PW+3 input clock cycle after the parity error was detected. If BC0E DA2='0', ALERT\_n continues to be driven LOW until a 'Clear Error Status' command is received. During the ALERT\_n pulse duration, RD and WR commands are ignored.
6. The 'Clear Error Status' command will re-enable BCOM parity checking. If the ALERT\_n re-enable bit in BC0E is set, BCOM parity checking will be re-enabled after the expiration of the ALERT\_n pulse.

When a command sequence error is detected, the data buffer will take the following actions.

1. The data buffer logs all the bits of the erroneous command in the Error Log Register (F7BC0x .. F7BC3x) if there is no previous (parity or command sequence) error already logged in these registers and sets the sequence error bit to '1'.
2. Command Sequence error checking and parity error checking will be disabled.
3. If the sequence error is detected during a configuration command (BCW Write or MRS Write), the state of the buffer configuration bits will not be modified. In other words, the configuration command will not be executed.
4. All scheduled RD/WR commands that have not yet executed are dropped
5. The data buffer will assert the ALERT\_n output pin LOW for tSEQ\_ALERT\_PW clock cycles in a similar way as the DDR4 DRAM responds to CA parity errors. If an error occurs ALERT\_n is driven LOW with the third input clock edge after the corresponding incorrect data were captured on the data buffer command inputs. If BC0E DA2='1', ALERT\_n goes to high impedance with the tSEQ\_ALERT\_PW+3 input clock cycle after the protocol violation was detected. If BC0E DA2='0', ALERT\_n continues to be driven LOW until a 'Clear Error Status' command is received. During the ALERT\_n pulse, RD and WR commands are ignored.
6. The 'Clear Error Status' command will re-enable command sequence error checking. If the ALERT\_n re-enable bit in BC0E is set, sequence error checking will be re-enabled after the expiration of the ALERT\_n pulse.

### 2.1.7 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB01. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB\_RL and DB\_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB01 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB01 outputs respectively. Both DB\_RL and DB\_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$$

$$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + t_{RPRE}/2$$

The equations for DWL and MRE for Ranks 0 to 3 are:

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

$$DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * t_{CK}/64$$

$$DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * t_{CK}/64$$

$$DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * t_{CK}/64$$

$$DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * t_{CK}/64$$

$$DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * t_{CK}/64$$

$$DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * t_{CK}/64$$

$$DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * t_{CK}/64$$

$$DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * t_{CK}/64$$

$$MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * t_{CK}/64$$

$$MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * t_{CK}/64$$

$$MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * t_{CK}/64$$

$$MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * t_{CK}/64$$

$$MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * t_{CK}/64$$

$$MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * t_{CK}/64$$

$$MRE[3].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * t_{CK}/64$$

$$MRE[3].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * t_{CK}/64$$

$t_{RPRE}/2$  exists in DB\_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB01 delays  $t_{PDM\_RD}$  and  $t_{PDM\_WR}$  are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge

1.This equation assumes that the DDR4DB01 MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/F[3:0]BC9x are at their default power-on setting.

2.This equation assumes that the DDR4DB01 MDQS Read Delay Control Words in F[3:0]BC4x/F[3:0]BC5x are at their default power-on setting.

of MDQS for a WR command respectively. By default these delays are constant per DDR4DB01 for all ranks and nibbles.

## 2.1.7 Command Sequence Descriptions (cont'd)

Timing parameters that are integer multiples of  $t_{CK}$  are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of  $t_{CK}$  are shown in *red italic* letters. Timing parameters for transparent mode are shown in **plain green**.

For simplicity the timing diagrams only show one of the possible host interface termination modes and RTT\_PARK is never shown even though it is always supported.

### 2.1.7.1 Write Commands

Table 3 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 ( $A[1:0] = '00'$  or  $'10'$ ).

**Table 3 — Multicycle Sequence for Write Commands**

| Time<br>(clock cycle) | BCOM[3:0] | Description                                                                                                                                                                                 |
|-----------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                     | Prev Cmd  | Previous command or data transfer                                                                                                                                                           |
| 1                     | WR        | Write command<br>BCOM[3:0] = 1000                                                                                                                                                           |
| 2                     | DAT0      | Transfer the rank ID for write command<br>BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes<br>Burst length information for Write data<br>BCOM[3:2] = {0, 0} for BC4<br>BCOM[3:2] = {0, 1} for BC8 |
| 3                     | PAR[3:0]  | Even parity bits for WR command and data<br>PAR[x]: Parity bit for previous two BCOM[x] transfers                                                                                           |
| 4                     | Next Cmd  | Next Command                                                                                                                                                                                |

### 2.1.7.1 Write Commands (cont'd)

Figure 2 shows the timing sequence for a Write command.

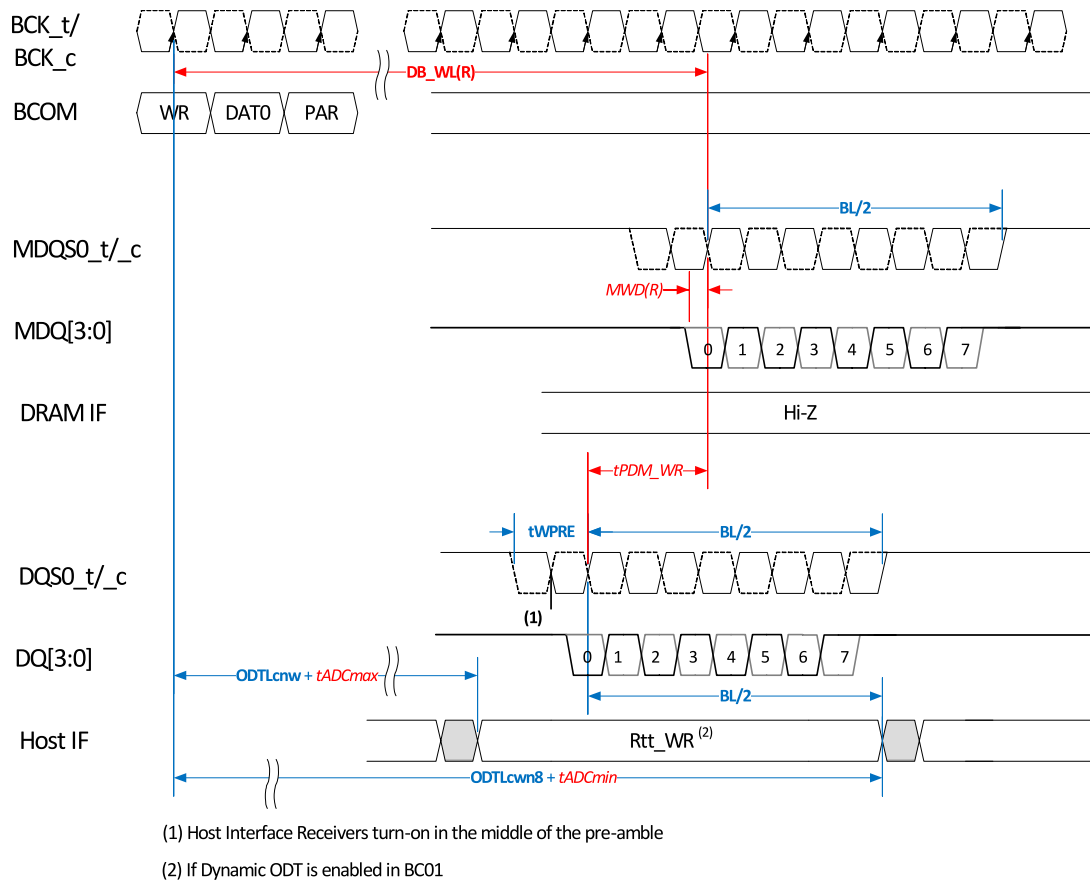


**Figure 2 — WRITE Timing**

### 2.1.7.2 Read Commands and MPR Override Reads

Table 4 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 ( $A[1:0] = '00'$  or  $'10'$ ).

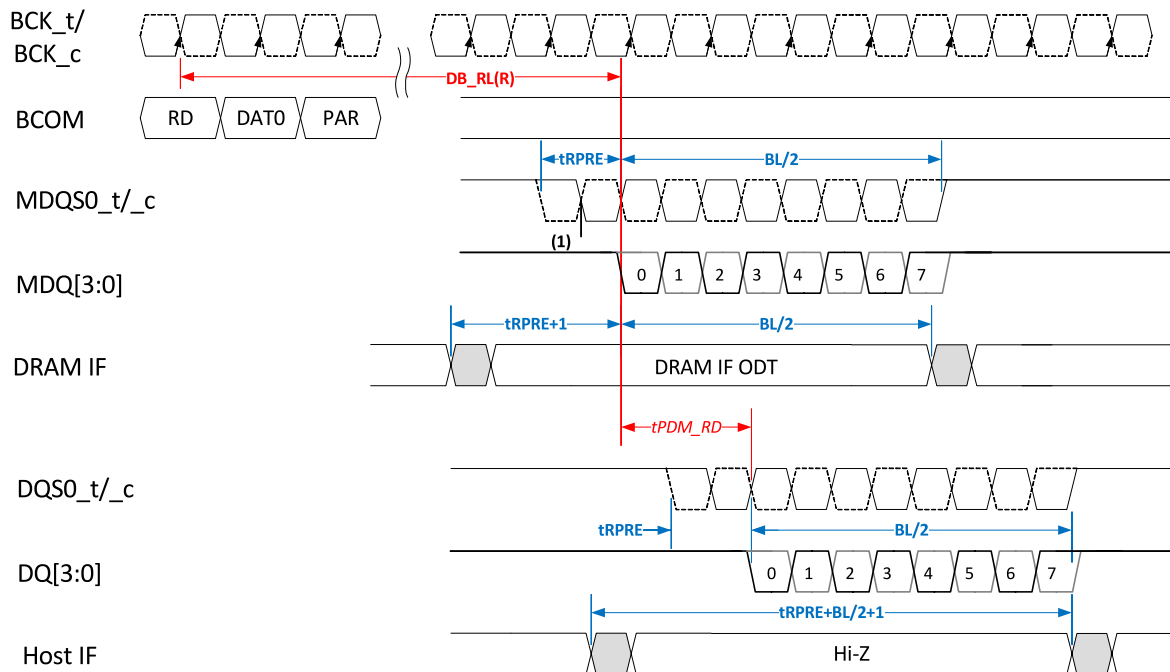
**Table 4 — Multicycle Sequence for Read Commands**

| Time (clock cycle) | BCOM[3:0] | Description                                                                                                                                                                                                                                                                                              |
|--------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                  | Prev Cmd  | Previous command or data transfer                                                                                                                                                                                                                                                                        |
| 1                  | RD        | Read command<br>BCOM[3:0] = 1001                                                                                                                                                                                                                                                                         |
| 2                  | DAT0      | Transfer the rank ID for read command or the MPR selection ID in MPR override read mode<br>BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads<br>BCOM[1:0] = {BA1, BA0} for MPR override reads<br>Burst length information for Read data<br>BCOM[3:0] = {0, 0} for BC4 <sup>1</sup><br>BCOM[3:2] = {0, 1} for BC8 |
| 3                  | PAR[3:0]  | Even parity bits for RD command and data<br>PAR[x]: Parity bit for previous two BCOM[x] transfers                                                                                                                                                                                                        |
| 4                  | Next Cmd  | Next Command                                                                                                                                                                                                                                                                                             |

1.BC4 is not supported for MPR override reads

### 2.1.7.2 Read Commands and MPR Override Reads (cont'd)

Figure 3 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

**Figure 3 — READ Timing**

Read commands can be used to access locations other than the memory array in the DDR4 DRAM devices. These special read commands are MPR override reads. The DDR4DB01 uses the Rank 0 output enable timing for these reads. By default, the only function of the data buffer during MPR reads and MRS reads is to simply forward the data received at the DRAM interface to the edge connector interface. In order to allow training of the data buffer to host segment separately from the data buffer to DRAM segment, the buffer can be configured in an override mode for MPR read commands. The override mode for MPR reads is enabled by a buffer control word, BCW, bit (F0BC1x, DA1). The power-on default values for MPR0 to MPR3 are the same as the power-on default values for the DRAM MPRs, see Table 58. When the MPR read override mode is enabled the buffer sends its own MPR data bits on the host interface instead of the data received from the DRAMs. The DB implements the equivalent of the writeable DRAM page 0 Multi Purpose Registers. The DDR4DB01 supports two modes in which MPR can be accessed for read. The two modes are serial return and parallel return. There is also an optional staggered return format described in 2.1.7.3. 5 and 6 illustrate the serial return and parallel return methods for MPR0 reads. Both nibbles of the DB drive identical information. In these examples the pattern programmed in the MPR0 (F5BC0x, DA[7:0]) is 0111 1111. Back to back accesses to MPR0 in serial or parallel modes return the same information.

## 2.1.7.2 Read Commands and MPR Override Reads (cont'd)

Table 5 — MPR Override Read Format for Serial Return

| Serial | UI0 | UI1 | UI2 | UI3 | UI4 | UI5 | UI6 | UI7 |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| DQ0    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ1    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ2    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ3    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ4    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ5    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ6    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ7    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

Table 6 — MPR Override Read Format for Parallel Return

| Parallel | UI0 | UI1 | UI2 | UI3 | UI4 | UI5 | UI6 | UI7 |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| DQ0      | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| DQ1      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ2      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ3      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ4      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ5      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ6      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ7      | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

The DDR4DB01 supports MPR override reads using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR override reads. The DDR4DB01 supports MPR override read commands that are 4  $t_{CK}$  apart so that in BL8 mode a stream can be created on the data bus with no bubbles or clocks between read data.

## 2.1.7.3 Optional MPR Override Read Format for Staggered Returns

Table 7 illustrates the staggered return method. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. A read command to MPR0 will result in data being driven from MPR0 on DQ0, data from MPR1 on DQ1 and so forth as shown in the UI0-7 column in Table 7. For the return pattern shown in Table 7, the controller issues a 8-command sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3 resulting in a un-interrupted stream of 64UI.

Table 7 — MPR0,1,2,3,0,1,2,3 Override Read Format for Staggered Return

| RD Command Staggered | MPR0 UI0-7 | MPR1 UI8-15 | MPR2 UI16-23 | MPR3 UI24-31 | MPR0 UI32-39 | MPR1 UI40-47 | MPR2 UI48-55 | MPR3 UI56-63 |
|----------------------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DQ0                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ1                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ2                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ3                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ4                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ5                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ6                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ7                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |

**2.1.7.3 Optional MPR Override Read Format for Staggered Returns (cont'd)**

The DDR4DB01 can respond to back to back read commands starting with MPR1 as shown in Table 8.

**Table 8 — MPR1,2,3,0,1,2,3,0 Override Read Format for Staggered Return**

| RD Command Staggered | MPR1 UI0-7 | MPR2 UI8-15 | MPR3 UI16-23 | MPR0 UI24-31 | MPR1 UI32-39 | MPR2 UI40-47 | MPR3 UI48-55 | MPR0 UI56-63 |
|----------------------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DQ0                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ1                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ2                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ3                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ4                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ5                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ6                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ7                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |

The DDR4DB01 can respond to back to back read commands starting with MPR2 as shown in Table 9.

**Table 9 — MPR2,3,0,1,2,3,0,1 Override Read Format for Staggered Return**

| RD Command Staggered | MPR2 UI0-7 | MPR3 UI8-15 | MPR0 UI16-23 | MPR1 UI24-31 | MPR2 UI32-39 | MPR3 UI40-47 | MPR0 UI48-55 | MPR1 UI56-63 |
|----------------------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DQ0                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ1                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ2                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ3                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ4                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ5                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ6                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ7                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |

The DDR4DB01 can respond to back to back read commands starting width MPR3 as shown in Table 10.

**Table 10 — MPR3,0,1,2,3,0,1,2 Override Read Format for Staggered Return**

| RD Command Staggered | MPR3 UI0-7 | MPR0 UI8-15 | MPR1 UI16-23 | MPR2 UI24-31 | MPR3 UI32-39 | MPR0 UI40-47 | MPR1 UI48-55 | MPR2 UI56-63 |
|----------------------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DQ0                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ1                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ2                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ3                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |
| DQ4                  | MPR3       | MPR0        | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         |
| DQ5                  | MPR0       | MPR1        | MPR2         | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         |
| DQ6                  | MPR1       | MPR2        | MPR3         | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         |
| DQ7                  | MPR2       | MPR3        | MPR0         | MPR1         | MPR2         | MPR3         | MPR0         | MPR1         |

#### 2.1.7.4 MRS Write Commands

The RCD only generates MRS Write commands to the data buffers for each A-side MRS command to Rank 0.

Table 11 shows the sequence for MRS Write commands.

**Table 11 — Multicycle Sequence for MRS Write Commands**

| Time (clock cycle) | BCOM[3:0] | Description                                                                                            |
|--------------------|-----------|--------------------------------------------------------------------------------------------------------|
| 0                  | Prev Cmd  | Previous command or data transfer                                                                      |
| 1                  | MRS Write | MRS Write Command<br>BCOM[3:0] = 1011                                                                  |
| 2                  | DAT0      | MRS ID code<br>BCOM[3:0] = {0, BG0, BA1, BA0}                                                          |
| 3                  | DAT1      | First data transfer for MRS Write command<br>BCOM[3:0] = {0, DA2, DA1, DA0}                            |
| 4                  | DAT2      | Second data transfer for MRS Write command<br>BCOM[3:0] = {0, DA5, DA4, DA3}                           |
| 5                  | DAT3      | Third data transfer for MRS Write command<br>BCOM[3:0] = {0, DA8, DA7, DA6}                            |
| 6                  | DAT4      | Fourth data transfer for MRS Write command<br>BCOM[3:0] = {0, DA11, DA10, DA9}                         |
| 7                  | DAT5      | Fifth data transfer for MRS Write command<br>BCOM[3:0] = {0, 0, DA13, DA12}                            |
| 8                  | PAR[3:0]  | Even parity bits for MRS Write command and data<br>PAR[x]: parity bit for 7 previous BCOM[x] transfers |
| 9                  | Next Cmd  | Next Command                                                                                           |

The sequence for an MRS Write command is shown in Figure 4. The timing diagram shows how the MRS Write command is followed by six data transfer cycles and a parity data transfer cycle. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the MRS Write command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRS Write command also imposes a limitation on how close consecutive MRS Write commands can be issued to the data buffer.

For MRS commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in RC0D is set to '0' (LRDIMM), the DDR4 register generates a BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer's host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection. The DDR4DB01 will not capture any MRS bits written in PDA mode.

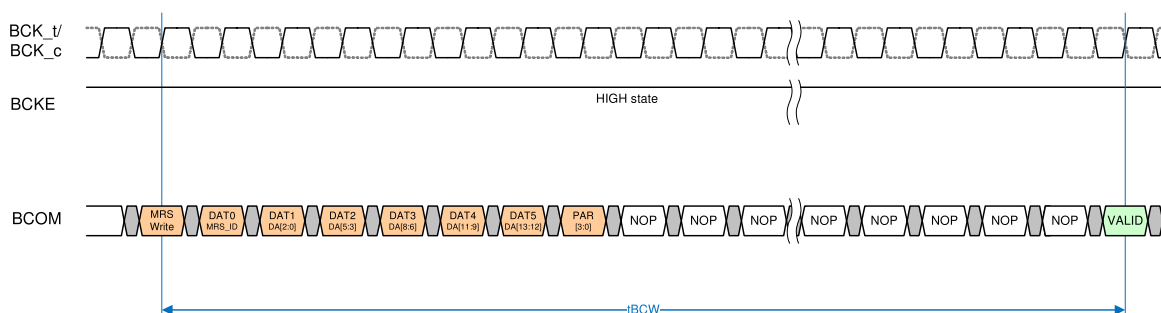


**Figure 4 — MRS Write command sequence**

### 2.1.7.5 Per DRAM Addressability Support

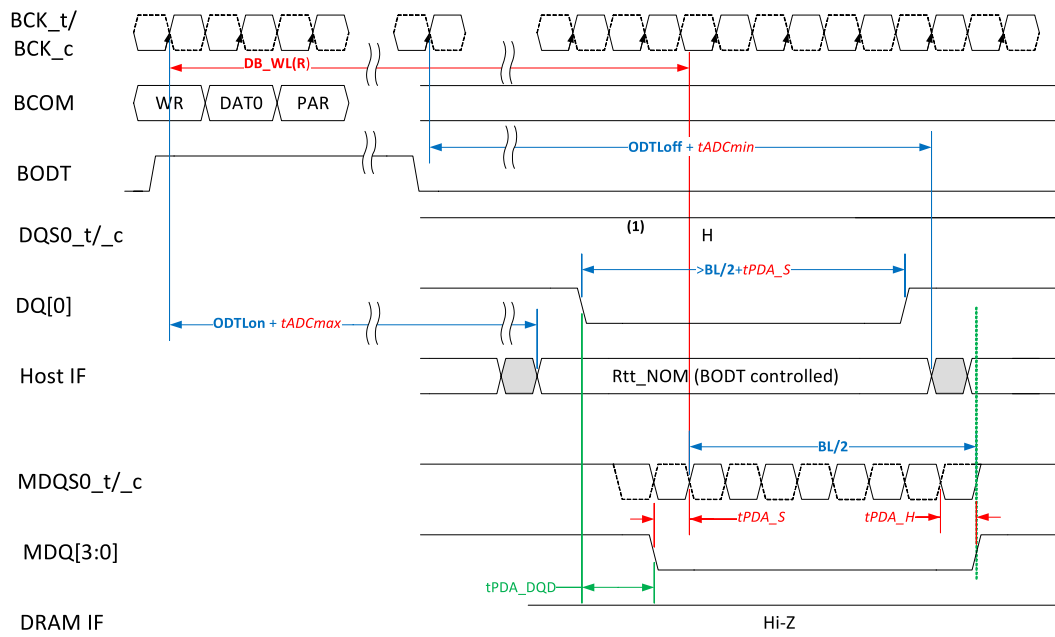
In order to enable the DDR4 ‘per DRAM addressability (PDA)’ feature the data buffer will perform a “write” data transaction in each MRS Write command to transfer data from the host interface to the DRAM interface whenever the PDA mode enable bit in F0BC1x is set to 1 to indicate that this feature is enabled. This will need to be a special write mode in the data buffer because it is necessary to meet the PDA setup and hold timing parameters ( $t_{PDA\_S}$  and  $t_{PDA\_H}$ ) in the DDR4 DRAMs. This special write mode will work by allowing the host to have direct control of the MDQ signals on the DRAM interface of the buffer in transparent mode. In other words, the DQ to MDQ path will work in asynchronous transparent mode. In this way, the host will be able to assert the MDQ0 lines early enough to meet  $t_{PDA\_S}$  and late enough to meet  $t_{PDA\_H}$ . The data buffer will control the data strobe (MDQS\_t/MDQS\_c) burst on the DRAM interface as in a normal write command.

The DB does not process regular DRAM Write commands while in PDA mode. However, the RCD needs to process DRAM MPR Write commands correctly during this time. Before entering ‘per DRAM addressability (PDA)’ mode, DRAM write leveling is required to be performed by the host to the DRAM.

The sequence to enter and exit PDA mode for LRDIMMs is as follows (steps 1 and 2 can be swapped if desired):

1. Send MRS command to MR3 with A4=1 to the rank to be put into PDA mode
2. Send BCW to F0BC1x with DA2=1 to enter DB PDA mode
3. Perform per DRAM MRS commands or MPR writes (only for the rank that was put in PDA mode in step 1)
4. Send MRS command to MR3 with A4=0 to the rank that is in PDA mode with all DRAMs selected (DQ0=0)
5. Send BCW to F0BC1x with DA2=0 to exit DB PDA mode

The timing diagram in Figure 5 shows how the data buffer will handle MRS commands in ‘per DRAM addressability (PDA)’ mode. The path from host DQ to DRAM interface MDQ works in (asynchronous) transparent mode in this case.



(1) Host may send the DQS0\_t/\_c signal in PDA mode

Figure 5 — Processing of DRAM MRS command by data buffer in PDA mode

### 2.1.7.6 BCW Write Command

Table 12 shows the sequence for buffer control word write commands.

**Table 12 — Multicycle Sequence for BCW Write Commands**

| Time (clock cycle) | BCOM[3:0] | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                  | Prev Cmd  | Previous command or data transfer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1                  | BCW Write | Buffer control word write access command<br>BCOM[3:0] = 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2                  | DAT0      | First data transfer for BCW Write command<br>BCOM[3:0] = {0, DA2, DA1, DA0}                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 3                  | DAT1      | Second data transfer for BCW Write command<br>BCOM[3:0] = {0, DA5, DA4, DA3}                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4                  | DAT2      | Third data transfer for BCW Write command<br>BCOM[3:0] = {0, DA8, DA7, DA6}                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 5                  | DAT3      | Fourth data transfer for BCW Write command<br>BCOM[3:0] = {0, DA11, DA10, DA9}                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6                  | DAT4      | Fifth data transfer for BCW Write command<br>BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes<br>BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes<br>BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes<br>BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes<br>BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes<br>BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes<br>BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes<br>BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes |
| 7                  | PAR[3:0]  | Even parity bits for BCW Write command and data<br>PAR[x]: parity bit for 6 previous BCOM[x] transfers                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 8                  | Next Cmd  | Next Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

The sequence for a BCW Write command is shown in Figure 6. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tBCW parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

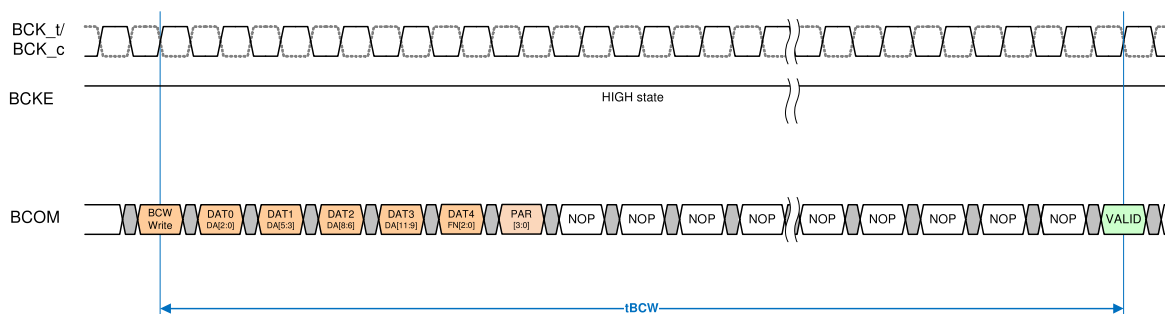


**Figure 6 — Buffer Control Word Write command sequence**

### 2.1.7.7 Per Buffer Addressability Feature

It is necessary for the data buffer to support a feature similar to per-DRAM addressability in the buffer control word access transactions. This feature will be used to allow the host controller to configure each data buffer independently from each other. This is a requirement, for example, to allow independent VrefDQ training per buffer or independent ODT impedance settings for certain buffers.

The PBA feature will be enabled by a BCW bit stored in a word that does not contain any registers that need to be programmed in per-buffer addressability mode. This is necessary so that it is possible to get the buffers in and out of PBA mode without having to modify BCW bits that have been programmed specifically per buffer. The mechanism to enable and disable BCW Write access per buffer will be very similar to the PDA mechanism, it will be based on the DQ0 host interface input signal, and it will only work once host interface write leveling training has been completed from the host controller to the data buffers. When PBA mode is enabled each buffer will use the captured DQ0 input signal level to determine if the BCW Write transaction actually applies to that particular buffer.

The sequence for two consecutive BCW Write commands with ‘per-buffer addressability (PBA)’ mode enabled is shown in Figure 7. This sequence shows consecutive BCW Write commands. Figure 8 shows the sequence for a BCW write command with ‘per-buffer addressability (PBA)’ mode enabled followed by a non-BCW write command. Since in the ‘per-buffer addressability (PBA)’ mode only BCW Write commands are allowed, the BCW Write command shown in Figure 7 has to be used to disable (exit) the ‘per-buffer addressability (PBA)’ mode. Before entering ‘per-buffer addressability (PBA)’ mode, the following buffer control words must be programmed: Host Interface RTT\_NOM Control Word (BC00) and Host Interface RTT\_PARK Control Word (BC02). After the Host Interface RTT\_NOM and Host Interface RTT\_PARK have been programmed ‘per-buffer addressability (PBA)’ mode can be enabled using BCW bit (F0BC1x, DA0). In the ‘per-buffer addressability (PBA)’ mode, all BCW Write commands are qualified with DQ0. If the value on DQ0 is 0 then the buffer executes the BCW write command. If the value on DQ0 is 1, then the buffer ignores the BCW Write command. The controller can choose to drive all the DQ bits. The per buffer control word command cycle time in PBA mode tMRD\_PBA is required to complete the write operation to the mode register and is the minimum time required between two BCW Write commands, as shown in Figure 7. Remove the buffer from ‘per-buffer addressability (PBA)’ mode by setting the corresponding BCW bit (F0BC1x, DA0). This command will require DQ0=0.

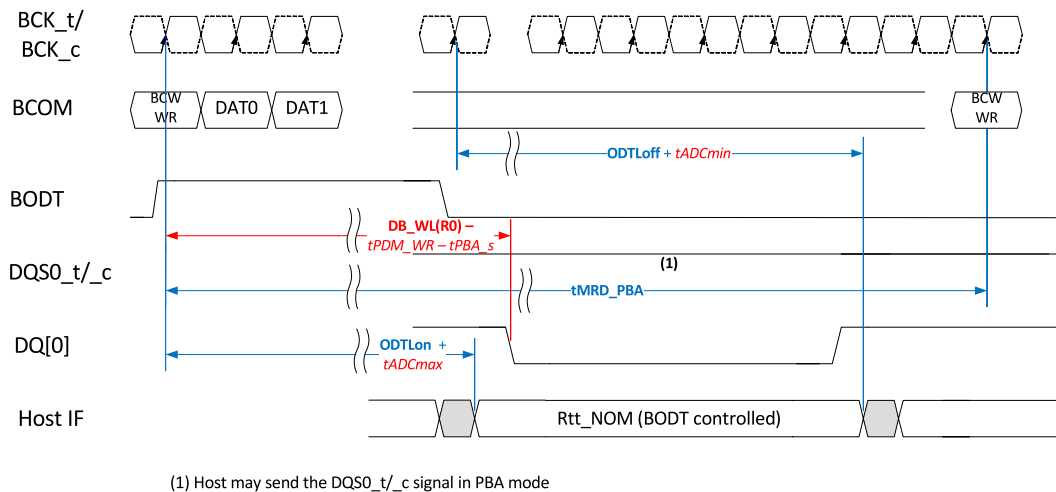
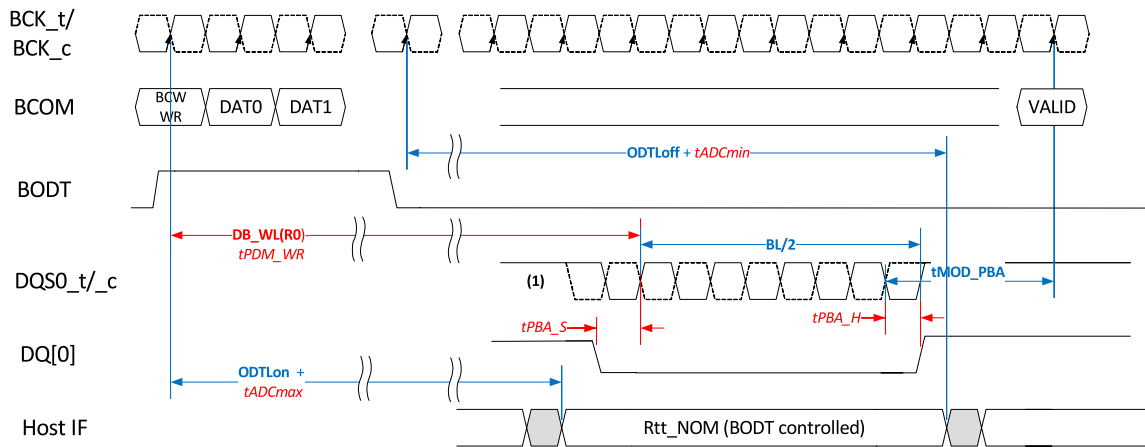


Figure 7 — BCW Write to BCW Write command sequence in PBA mode

Removing a buffer from ‘per-buffer addressability (PBA)’ mode will require programming the entire buffer control word when the BCW Write command is issued. The per buffer control word command update delay time tMOD\_PBA is required to complete the write operation to the mode register and is the minimum time required between a BCW command and any other valid command when ‘per buffer addressability (PBA)’ mode is enabled, as shown in Figure 8. The data buffer uses Rank 0 write timing in PBA mode.

### 2.1.7.7 Per Buffer Addressability Feature (cont'd)



(1) Host may not send the DQS0\_t/\_c signal in PBA mode

**Figure 8 — BCW Write to other command sequence in PBA mode**

Dynamic ODT is not supported. So extra care is required for the ODT setting. If RTT\_NOM is enabled in the Host Interface RTT\_NOM Control Word (BC00), the buffer data termination needs to be controlled by the BODT pin and applied with the same timing parameters as in normal operation.

### 2.1.7.8 BCW Read Commands

Buffer Control Words can be read from the DDR4DB01 via BCW read commands. Table 13 shows the sequence for BCW Read commands.

**Table 13 — Multicycle Sequence for BCW Read Commands**

| Time (clock cycle) | BCOM[3:0] | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                  | Prev Cmd  | Previous command or data transfer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1                  | BCW Read  | Buffer control word read access command<br>BCOM[3:0] = 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2                  | DAT0      | First data transfer for BCW Read command<br>BCOM[3:0] = {0, DA5, DA4, 0}                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3                  | DAT1      | Second data transfer for BCW Read command<br>BCOM[3:0] = {0, DA8, DA7, DA6}                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4                  | DAT2      | Third data transfer for BCW Read command<br>BCOM[3:0] = {0, DA11, DA10, DA9}                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5                  | DAT3      | Fourth data transfer for BCW Read command<br>BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads<br>BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads<br>BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads<br>BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads<br>BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads<br>BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads<br>BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads<br>BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads |
| 6                  | PAR[3:0]  | Even parity bits for BCW Read command and data<br>PAR[x]: parity bit for 5 previous BCOM[x] transfers                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 7                  | Next Cmd  | Next Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

### 2.1.7.8 BCW Read Commands (cont'd)

The sequence for BCW Read command is shown in Figure 9. The timing diagram shows how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR override read from MPR0 (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB\_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD01 will forward Read command to DRAM but DDR4DB01 will ignore read data from DRAM. After the read command that follows the BCW Read command, the DB will be back in normal operation, i.e., all subsequent reads come from the DRAM interface (unless F0BC1x DA1=1). The host is required to wait at least tBCR between issuing a BCW Read command and the following Read command.

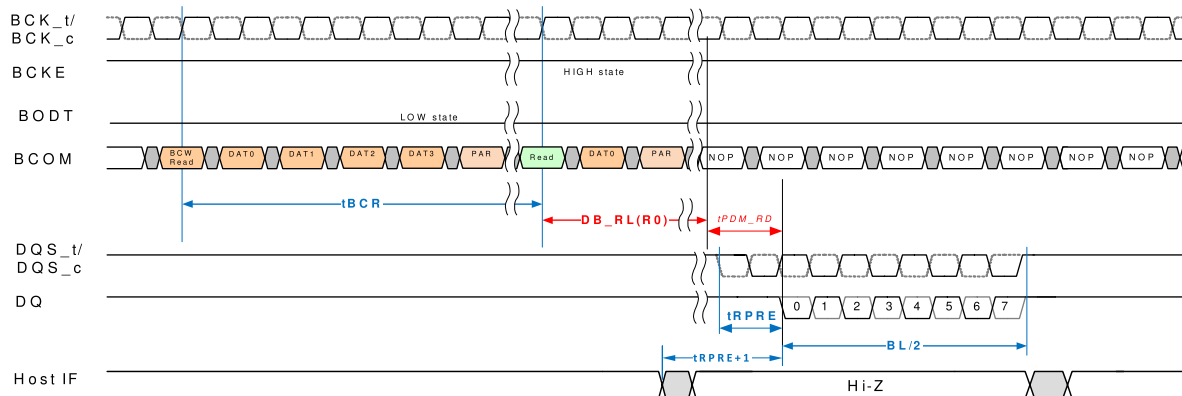


Figure 9 — BCW Read command sequence

#### 2.1.7.8.1 BCW Read Data Format

Only the serial data format is available for Reads following a BCW Read commands - see Table 14. The data buffer is required to drive associated strobes with the read data return. Serial return implies that the same pattern is returned on all DQ lanes as shown in Table 14. All undefined or reserved bits in the BCW must be driven as '0'. In this example the value programmed in BCWXx (DA[7:0]) is 0111 1111. The command issued from the register is BCW Read (BCOM[3:0] = 1101). This tells the buffer that the 8 bits from BCWXx need to be accessed serially. All BCW read transactions are done in burst length of 8 by the buffer. All BCW accesses are aligned to byte boundaries. The DB will always send two 4-bit CWs on every 4-bit CW Read command. In case of a 4-bit CW Read command with an even address in RCD RC6x DA[7:4], the DB will send the addressed 4-bit CW in UI0 .. UI3 and the next address 4-bit CW in UI4 .. UI7. In case of a 4-bit CW Read command with an odd address in RCD RC6x DA[7:4], the DB will send the addressed 4-bit CW in UI4 .. UI7 and the previous address 4-bit CW in UI0 .. UI3.

Table 14 — BCW Read Data Format

| Serial | UI0 | UI1 | UI2 | UI3 | UI4 | UI5 | UI6 | UI7 |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| DQ0    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ1    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ2    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ3    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ4    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ5    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ6    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| DQ7    | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |



### 2.1.8 Training Support Features

The DDR4DB01 does not contain self-sufficient training state machines for calibrating its timing control settings. It will instead depend on the host controller to get the timing control registers programmed with the appropriate settings that will allow the DB to work in the DDR4 LRDIMM environment. To enable the host controller in performing the training procedure in an efficient and reliable manner, the data buffer provides various training support features. The following sections describe such training support features in the DDR4DB01

The DB provides separate timing control registers for the lower and upper nibble. However, there is only one Buffer Training Mode Control Word so both nibbles are always in the same training mode.

Table 15 provides an overview of the buffer control words (BCW) that are involved in the timing control and timing training features of the DDR4DB01.

**2.1.8 Training Support Features (cont'd)****Table 15 — Timing and Training Control Words**

| Address                            | Description                                                                                   | Scope                                                                                                                                   |
|------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| BC0C                               | Training control word                                                                         | Training mode enable                                                                                                                    |
| F0BCCx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0 | Additional cycles of DRAM Interface Receive Enable Delay and Write Leveling Delay per rank and per nibble                               |
| F0BCDx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0 |                                                                                                                                         |
| F0BCEx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2 |                                                                                                                                         |
| F0BCFx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2 |                                                                                                                                         |
| F1BCCx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1 |                                                                                                                                         |
| F1BCDx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1 |                                                                                                                                         |
| F1BCEx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3 |                                                                                                                                         |
| F1BCFx                             | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3 |                                                                                                                                         |
| F[3:0]BC2x                         | Lower nibble DRAM interface receive enable training control                                   | DRAM Interface Receive Enable phase and cycle control per rank                                                                          |
| F[3:0]BC3x                         | Upper nibble DRAM interface receive enable training control                                   |                                                                                                                                         |
| F[3:0]BC4x                         | Lower nibble MDQS read delay control                                                          | Input MDQS delay control per rank                                                                                                       |
| F[3:0]BC5x                         | Upper nibble MDQS read delay control                                                          |                                                                                                                                         |
| F[3:0]BC8x                         | Lower nibble MDQ-MDQS write delay control                                                     | Output MDQ signal phase control per rank                                                                                                |
| F[3:0]BC9x                         | Upper nibble MDQ-MDQS write delay control                                                     |                                                                                                                                         |
| F[3:0]BCAx                         | Lower nibble DRAM interface write leveling control                                            | DRAM Interface write leveling phase and cycle control per rank                                                                          |
| F[3:0]BCBx                         | Upper nibble DRAM interface write leveling training control                                   |                                                                                                                                         |
| F5BC0x - F5BC3x<br>F6BC0x - F6BC3x | Lower and upper nibble Multi Purpose Registers[7:0]                                           | Store read/write data patterns for receive enable, read and write delay and host interface write training as well as MPR override mode. |
| F6BC4x                             | Buffer training configuration control word                                                    | Configuration control for certain training modes                                                                                        |
| F6BC5x                             | Buffer training status word                                                                   | Status for certain training modes                                                                                                       |
| F[7:4]BC8x                         | MDQ0/4-Read delay control                                                                     | Input MDQ delay control per rank and per lane                                                                                           |
| F[7:4]BC9x                         | MDQ1/5-Read delay control                                                                     |                                                                                                                                         |
| F[7:4]BCAx                         | MDQ2/6-Read delay control                                                                     |                                                                                                                                         |
| F[7:4]BCBx                         | MDQ3/7-Read delay control                                                                     |                                                                                                                                         |
| F[7:4]BCCx                         | MDQ0/4-MDQS write delay control                                                               | Output MDQ signal phase control per rank and per lane                                                                                   |
| F[7:4]BCDx                         | MDQ1/5-MDQS write delay control                                                               |                                                                                                                                         |
| F[7:4]BCEx                         | MDQ2/6-MDQS write delay control                                                               |                                                                                                                                         |
| F[7:4]BCFx                         | MDQ3/7-MDQS write delay control                                                               |                                                                                                                                         |

**2.1.8 Training Support Features (cont'd)**

Table 16 provides a summary description of the various training support functions and features in the DDR4DB01.

**Table 16 — Summary of Training Support Features and Functions**

| Training Step                                       | Features                                                                                                                                      |
|-----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| DRAM Interface Receive Enable Phase Training (MREP) | Receiver enable phase detector on MDQS pins<br>Phase detector output driven on host interface DQ pins                                         |
| DRAM Write Leveling (DWL)                           | Generates MDQS but forwards MDQ to DQ.                                                                                                        |
| Host Interface Write Leveling (HWL)                 | Write Leveling phase detector on DQS pins<br>Phase detector output driven on host interface DQ pins                                           |
| MDQS Read Delay Training (MRD)                      | Phase adjustment for MDQS input delay<br>Multi Purpose Register control words<br>Data comparator output driven to host interface DQ pins      |
| MDQ-MDQS Write Delay Training (MWD)                 | Phase adjustment for MDQ-MDQS output delay<br>Multi Purpose Register control words<br>Data comparator output driven to host interface DQ pins |
| Host Interface Write Training (HIW)                 | Write data comparator logic<br>Multi Purpose Register control words<br>Data comparator output in training status word                         |

For the training modes that utilize a data comparison between received data and expected data (stored in the data buffer MPR), the host needs to wait tCCD\_CMP between commands with data movement (i.e., READ or WRITE). The DDR4DB01 does not support contiguous DQ data streams (i.e., without dead cycles between data bursts) in these training modes.

An example sequence for DDR4DB01 training is described in the flow diagram of Figure 10.

The host is responsible to program the Rank Presence control word BC07 to match the ranks of the particular module in training before any of the training modes are entered and this control word should not be changed from this point in time onwards (until the module is reset or retrained).

### 2.1.8 Training Support Features (cont'd)

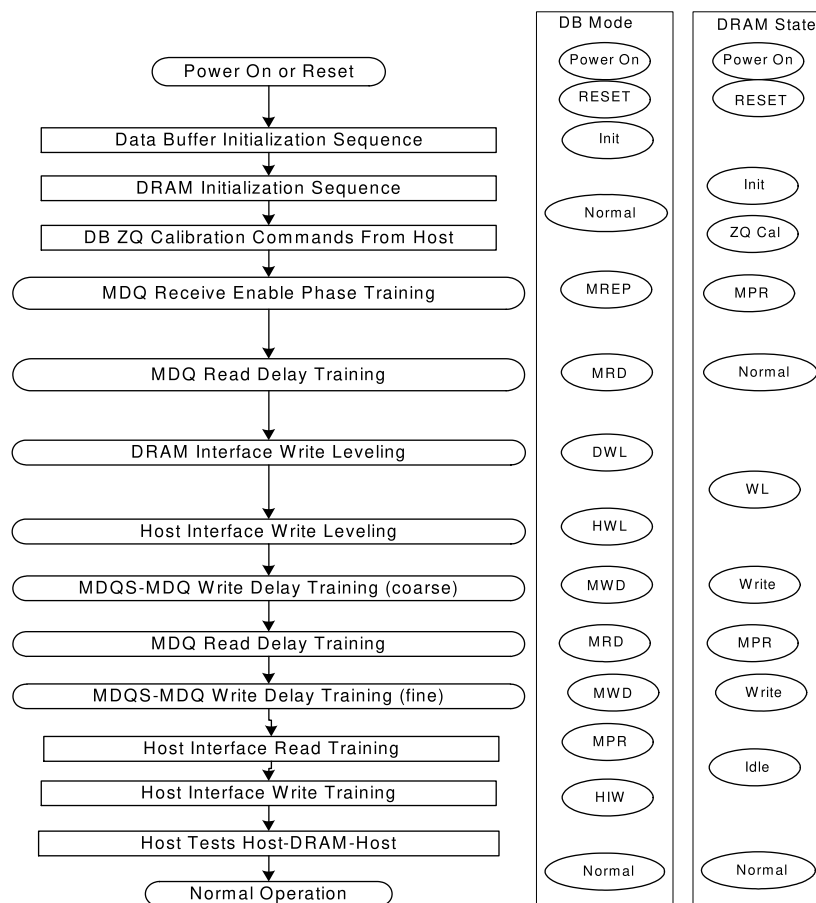


**Figure 10 — Example of Training Sequence Flow Diagram**

### 2.1.8.1 DRAM Interface MDQ Receive Enable Phase (MREP) Training Mode

This training mode has been defined so that it can be performed before any training has taken place between the host controller and the DDR4DB01

The DRAM interface receive enable phase timing selection is controlled in steps of  $1/64 * t_{CK}$  by Bits DA[5:0] in F[3:0]BC2x and F[3:0]BC3x. The host controller has the ability of setting the values for this parameter by means of BCW Write commands. The problem is how to find the optimal settings that will allow the data buffer to work reliably in the LRDIMM environment. To help the host controller solve this problem, the data buffer provides a DRAM interface receive enable phase training mode. In this training mode, the data buffer uses a group of programmable delay elements and sampling circuits to capture the MDQSx\_t/MDQSx\_c signals received from the DRAMs. There is one delay element per nibble and per rank. When the Receive Enable training control bits (F[3:0]BC2x/F[3:0]BC3x) are all zero, the phase of the internal DRAM interface receive enable clock is aligned to the data buffer input clock signal (BCK\_t/BCK\_c). In this training mode, the output of each MDQ/MDQS sampling circuit is driven onto the four host interface DQ pins corresponding to each nibble. In this training mode, the DQS\_t/DQS\_c inputs and outputs at the host interface are disabled.

To perform receive enable phase training, the host will first enable the MDQS Receive Enable Training mode in the Training Control Word (BC0C). After that, and assuming that the DRAMs have already been initialized, the host will send a sequence of Read commands to the DRAMs (using the DRAMs MPR) in order to generate a continuous train of pulses in the MDQSx\_t/MDQSx\_c inputs of the data buffer. The data buffer will use the RANK\_ID field in the Read Command sequences received through the BCOM[3:0] interface to select which receiver enable timing control register will be used during training. The DB will use F0BC2x and F0BC3x for Rank 0, F1BC2x and F1BC3x for Rank 1, and so on. Using the output of the sampling circuits available on the DQ pins, the host controller will be able to decide if it needs to increase or decrease the receive enable phase control settings in the data buffer by means of BCW Write commands. The objective is to find the end of the DRAM read preamble, i.e., first rising edge of MDQS\_t. At this time, the output of the sampling circuits will change from 0 to 1. With this method, the host controller will be able to align the internal receive enable clock to the first rising edge of the incoming MDQSx\_t/MDQSx\_c signals. Once this point has been found, the host controller will program the final value by applying an offset to the training result. The host must apply an offset of half clock cycle ( $32/64 * t_{CK}$ ) for 1  $t_{CK}$  read preamble mode or an offset of a full clock cycle ( $1 * t_{CK}$ ) for 2  $t_{CK}$  read preamble mode.

The MREP training step trained the partial cycle fields in the DRAM interface receive enable control words to their correct position, aligned with the strobes coming from the DRAMs. However, in the presence of large command delay differences between DRAM and data buffer, the full cycle fields in the DRAM interface receive enable control words may also need adjustment so that the data buffer receivers are enabled in the correct cycle. To accomplish this task, the host can put the data buffer into MRD mode by a BCW write to BC0C. In MRD mode, the host writes a known pattern to the DRAM MPR registers and also into the MPR registers of the data buffer and reads it back, allowing the data buffer to compare the read data with the known pattern. See 2.1.8.4 for details on MRD mode.

If the comparison shows that the data read is equal to the data written, the full cycle field in F0BCCx, F1BCCx, F0BCEx and F1BCEx is correct. If there is a mismatch, the host adjusts the full cycle field bits and repeats the READ/WRITE sequence until the comparison results show that the data written was correctly read back.

The data buffer provides only a single Read FIFO fall-through time for all ranks and for correct operation this delay cannot change. Any potential adjustments to this data buffer Read FIFO fall-through time have to be performed prior to this training step. The host is responsible for establishing and maintaining its own unique read enable timing for each rank.

The DRAM interface receive enable timing established in this training step is also used by the DB for the driver enable for the DQ/DQS outputs for Read commands (by adding an offset that corresponds to the Read FIFO flow-through time) as well as for the turn-on and turn-off timing of the DRAM interface MDQ/MDQS ODT termination.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

To allow the host to perform its own receive enable training, the host needs to exit MREP mode and put the data buffer into normal mode. In normal mode, the DB will forward the read data from the DRAM interface to the host interface and generate the associated DQS\_t/DQS\_c strobes. Optionally, Read Preamble Training mode (F0BC1x DA4=1) may be enabled normal mode to help the host with its own receive enable training.

### 2.1.8.2 DRAM Interface Write Leveling (DWL) Training Mode

This training mode has been defined so that it can be performed before any training has taken place between the host and the DDR4 DB.

The DRAM interface write leveling phase timing selection is controlled in steps of  $1/64 * t_{CK}$  by Bits DA[5:0] in F[3:0]BCAx and F[3:0]BCBx. The host controller has the ability of setting the values for this parameter by means of BCW Write commands. There is one delay element per nibble and per rank. In this training mode, the data buffer drives the DRAM feedback onto the four host connector interface DQ pins corresponding to each nibble.

To perform DRAM interface write leveling training, the host will first enable the DRAM Interface Write Leveling Training mode in the Training Control Word (BC0C). After that the host will increment the strobe timing by writes to F[3:0]BCAx/F[3:0]BCBx. The data buffer will generate a sequence of pulses on its MDQSx\_t/MDQSx\_c outputs (meeting the DDR4DB01 tMQSH(min) and tMQL(min) parameters). In this training mode the DQ inputs are disabled and the DQ outputs drive the sampled MDQ inputs. The DQS\_t/DQS\_c inputs and outputs at the host interface are disabled. The data buffer will use the content of BC08 DA[1:0] to select which Write Leveling timing control word will be used during DRAM Write Leveling training. The DB will use F0BCAx/F0BCBx and F0BCDx for Rank 0, F1BCAx/F1BCBx and F1BCDx for Rank 1, F2BCAx/F2BCBx and F0BCFx for Rank 2 and F3BCAx/F3BCBx and F1BCFx for Rank 3. Using the DRAM feedback available on the data buffer's DQ output pins, the host controller will be able to decide if it needs to increase or decrease the DRAM Write Leveling control settings in the data buffer by means of BCW Write commands.

The host controller can perform this procedure independently for the upper and the lower nibbles, because the data buffer provides independent controls for the upper and the lower nibbles. The host controller can also perform this procedure independently per rank because the data buffer provides independent receive enable phase timing controls per rank.

The DRAM Write Leveling training step should be followed by the host interface write leveling step by writing with a BCW to BC0C.

### 2.1.8.3 Host Interface Write Leveling (HWL) Mode

Since the DRAM write leveling timing adjustments are done by the data buffer, the host does not yet know the required strobe alignments to the clock. To help the host controller solve this problem, the data buffer provides a host interface write leveling training mode. The host controller is responsible for performing this procedure independently for each rank (and maintain its adjusted DQS delays per rank) since the buffer has the same Write FIFO fall-through times independent of the rank.

To perform write leveling phase training, the host will first enable the Host Interface Write Leveling mode in the Training Mode Control Word (BC0C). After that, and assuming that the DRAM interface write leveling training has already been performed, the host will issue DESELECT commands to the DB (targeted at the DRAMs). The host will generate one half-cycle DQSx\_t/DQSx\_c pulse per DESELECT command. This Host interface write leveling scheme assumes that the data buffer has only a single Write FIFO fall-through time through the data buffer and that this delay doesn't change (until the next initialization sequence) so any potential adjustments to the data buffer Write FIFO fall-through time have to be performed prior to this training step.

In this training mode, the DDR4 DB keeps the MDQ/MDQS drivers disabled. The DB will signal the strobe to clock alignment on the host connector interface DQ pins (in the same way a DRAM signals its strobe to clock alignment), i.e., the DQS\_t/DQS\_c inputs and the DQ outputs are enabled. Since the strobe to clock alignment has already been performed on the DRAM interface side, and the Write FIFO fall-through time is fixed, the data buffer knows the required strobe timing on the host interface for each nibble for each rank and can provide the alignment information to the host. The host controller will be able to decide if it needs to increase or decrease the DQSx\_t/DQSx\_c timing. The objective is to find the setting where the output of the DB DQ pins changes from '0' to '1'.

The host controller needs to perform this procedure independently for the upper and the lower nibbles, because each x4 DRAM will require a different write leveling adjustment. The host controller can also perform this procedure independently per rank because the data buffer provides independent receive enable phase timing controls per rank. The host is required to program BC08 DA[1:0] with the Rank ID of the rank being write leveled before entering HWL mode.

### 2.1.8.3 Host Interface Write Leveling (HWL) Mode (cont'd)

When the BODT input is asserted the DB provides RTT\_NOM termination on DQS<sub>t</sub>/DQS<sub>c</sub> in this mode with the previously established host ODT timing but DQ termination is OFF. When the BODT input is de-asserted the DB provides RTT\_PARK termination on DQS<sub>t</sub>/DQS<sub>c</sub> in this mode with the previously established host ODT timing but DQ termination is OFF. The data buffers on all LRDIMMs in a channel must be put into this mode for write leveling. The write leveling is performed one rank at a time and the data buffers on other DIMMs should have their DQ outputs and terminations disabled with writes to BC03, DA3='1'.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

The procedures described in the DWL and HWL training modes are used to achieve phase alignment between the DRAM strobe and the clock inputs. However, the host still does not know whether its strobe timing established in the HWL step corresponds to the correct CAS Write Latency (CWL) required by the DRAM. After the training steps are completed, the host performs a sequence of Writes followed by Reads to establish the correct cycle timing for write leveling by writing the Additional Cycles of DRAM Interface Write Leveling Delay control words (F0BCDx, F1BCDx, F0BCFx, F1BCFx).

### 2.1.8.4 DRAM-to-DB Read Delay (MRD) Training Mode

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM (either from its internal array or from the MPRs for data-preserving read training). The data buffer provides data pattern control words that are programmed with the expected read data from the DRAM and the results of the comparison is provided on the data buffers host interface.

To perform DRAM-to-DB read training, the host will first enable the MDQS read delay training mode in the Training Mode Control Word (BC0C).

The delay of the DRAM interface data strobe signals (MDQS<sub>t</sub>/MDQS<sub>c</sub>) during read transactions is selected by buffer control word F[3:0]BC4x and F[3:0]BC5x for lower and upper nibble respectively. The nominal setting for F[3:0]BC4x/F[3:0]BC5x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into F[3:0]BC4x/F[3:0]BC5x. Since the DDR4DB01 uses the RANK ID fields in the BCOM Read Command sequences to select the correct DRAM interface receive enable timings for the reads from the DRAMs, the content of BC08 DA[1:0] is don't care while in this training mode.

In this training mode, the data buffer uses a data pattern comparator to determine if the read data arriving from the DRAMs after a Read command match an expected result. There is one data comparator per data buffer. The output of the data comparator is driven onto the eight host connector interface DQ pins corresponding. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. Bit 0 of the Buffer Training Configuration control word F6BC4x selects whether all four DQ bits within a nibble are driven to '0' if there is any mismatch in any of the 32 bits associated with that nibble or whether only the DQ bit(s) of the particular lane(s) (i.e., the series of 8 bits arriving on the same DQ bit) that had one or more mismatches are driven to '0'. The expected data pattern values are stored in the MPR control words F5BC0x through F5BC3x and F6BC0x through F6BC3x.

MPR0[7:0] will contain the expected first UI (UI0) for MDQ[7:0] and MPR7[7:0] will contain the expected last UI (UI7) for MDQ[7:0], or in a general sense: MPRx[7:0] should match UIx for MDQ[7:0].

The 64 bits contained in these data registers can support arbitrary data patterns in a single BL8 data transaction. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

#### 2.1.8.4 DRAM-to-DB Read Delay (MRD) Training Mode (cont'd)

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to the baseline MDQS delay may be required. For this purpose the host controller can utilize the per lane MDQS-MDQ read delay control words F[7:4]BC8x through F[7:4]BCBx. F4BC8x controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BC9x controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of  $\pm 3 \times 1/64 \times t_{CK}$  is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQS delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

#### 2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e., the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx\_t/MDQSx\_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of  $\pm 3 \times 1/64 \times t_{CK}$  is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

### 2.1.8.6 Host Interface Read Training

For the DB-to-host read training, the DQS delay adjustments are performed in the host so that it can correctly sample the data driven by the DB (originating from the data buffer's MPRs instead of originating from the DRAM MPRs).

To perform DB-to-host read training, the host will first enable the MPR Override mode in the Buffer Configuration Control Word (F0BC1x) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host will cause the data buffer to send the contents of the data buffer's MPR back to the host by issuing DRAM Read commands through the DDR4 register.

This mode utilizes MPR0 to MPR3 and supports the same formats as a DDR4 DRAM page 0 MPR reads (Serial, Parallel, and the Optional Staggered if supported ).

The DDR4DB01 uses the Rank 0 output enable timing for MPR Override reads.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

### 2.1.8.7 Host Interface Write Training (HIW) Mode

For the host-to-DB write delay training, the DQ-DQS delay adjustments are performed in the host so that the data buffer receives the DQ and DQS signals with the optimal phase relationship. The data buffer provides data pattern control words that are programmed with the expected write data from the host and the results of the comparison is provided in the training status word (F6BC5x) and in BC0F, DA3. The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x). Read command in that mode is designed to provide the content of F6BC5x[7:0] on the DQ[7:0] for a burst length of 8 in a way similar to the MPR mode with data coming from the mentioned register. The DDR4DB01 uses the Rank 0 output enable timing for these reads.

To perform host-to-DB write training, the host will first enable the host interface write training mode in the Training Mode Control Word (BC0C), followed by write commands to the RCD and DB. The DDR4DB01 uses the RANK ID field in the BCOM Write Command sequences to select the correct host interface write leveling timing. The content of BC08 DA[1:0] are don't care while in this training mode. Using the result from the data comparator available in the Training Status Word and Error Status Word, the host controller will be able to determine if it has found the correct value of DQS-DQ delay for that particular nibble or bit lane or if needs to increment or decrement its own phase delay. The host may also send one or more consecutive read commands to obtain the result from the data comparator available in the Training Status Word F6BC5x.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

After the host interface read and write training steps are completed the host may perform additional writes and read to and from DRAM to further train the host bus by adjusting its own I/O timings

### 2.1.9 Transparent Mode

Transparent mode is enabled in the DDR4DB01 by setting F0BC1x DA5 to 1. While in transparent mode, the DB does not interpret BCOM commands. For BCOM[3:0] input values of '1010' it directs the data flow from host interface to DRAM interface and it enables the on-die termination at the host interface. For BCOM[3:0] input values other than '1010', the Data Buffer directs the data flow from DRAM interface to host interface and it enables the on-die termination at the DRAM interface. The Data Buffer does not support high-speed changes in direction of data flow. The tMRD\_TM parameter in the Timing Requirements section describes how often the direction in data flow can be reversed in transparent mode.

In transparent mode the Data Buffer statically enables the input receivers of the interface that is receiving signals and it permanently enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. In this mode, the data and data strobe signals flow asynchronously through the DB. The DB needs to provide balanced (matched) propagation delay for all the signals within each DQ/DQS-MDQ/MDQS nibble.

All the clock frequencies available in normal mode in the Data Buffer will also be supported in transparent mode.

### 2.1.9 Transparent Mode (cont'd)

The test equipment will have direct control of the BODT signal through the DODTn inputs of the DDR4 Register. The DB supports two modes for using the BODT signal while transparent mode is enabled. The two modes are selected by F0BC1x DA6 and they are described in Table 17. In the first mode, the BODT input signal is ignored and the enabling of the on-die termination is determined only by the BCOM[3:0] inputs. The host interface termination is enabled for BCOM[3:0] input values of '1010', and the DRAM interface termination is enabled for BCOM[3:0] input values other than '1010'. In the second mode, the BODT signal is used as a condition, in addition to the BCOM[3:0] values, to enable or disable the on-die terminations of the DRAM interface and the host interface. In the second mode, the on-die terminations are enabled when BODT is driven HIGH, and the terminations are disabled when the BODT signal is driven LOW.

In transparent mode, the strength of the DRAM Interface termination is controlled by the MDQ RTT Buffer Control Word (BC04) and the strength of the Host Interface termination is controlled only by the RTT\_NOM Buffer Control Word (BC00).

**Table 17 — DB Termination Control in Transparent Mode**

| BCOM[3:0] | BODT | BODT Mode (F0BC1x DA6) | Host Termination | DRAM Termination |
|-----------|------|------------------------|------------------|------------------|
| = '1010'  | LOW  | 0                      | ON               | OFF              |
|           |      | 1                      | <b>OFF</b>       | OFF              |
|           | HIGH | 0                      | ON               | OFF              |
|           |      | 1                      | ON               | OFF              |
| ≠ '1010'  | LOW  | 0                      | OFF              | ON               |
|           |      | 1                      | OFF              | <b>OFF</b>       |
|           | HIGH | 0                      | OFF              | ON               |
|           |      | 1                      | OFF              | ON               |

### 2.1.10 ZQ Calibration

The DDR4DB01 performs I/O circuit calibration when it receives BC06 commands CMD1 (ZQCL) or CMD2 (ZQCS). In order to use ZQ calibration command, a 240  $\Omega$  +/- 1% resistor must be connected between the ZQCAL pin and Vss.

Proper host interface RTT\_NOM, RTT\_WR, RTT\_PARK DQ/DQS drive strength, DRAM interface RTT and MDQ/MDQS drive strength not guaranteed until a ZQCL calibration command is issued.

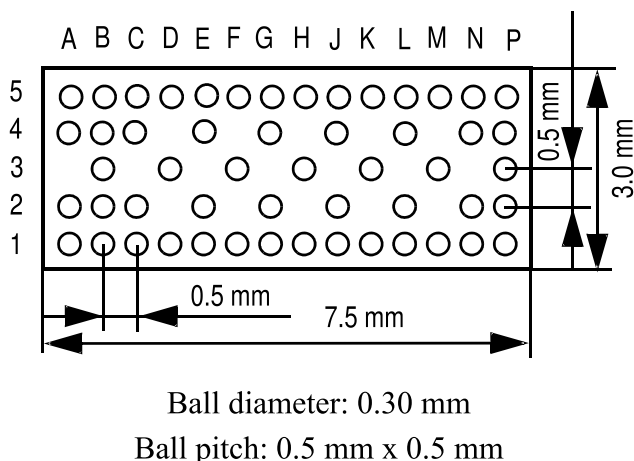
The host sends ZQCL and ZQCS calibration commands through the DDR4 register. The host needs to issue ZQ calibration commands sequentially to each package rank (i.e., wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one). No other commands that cause data transfers on the host interface DQ/DQS outputs or the DRAM interface MDQ/MDQS outputs are allowed during the tZQinit, tZQoper or tZQCS periods.

The DDR4DB01 may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands. That will depend on the behavior of the DDR4 register. If the DDR4RCD01 is configured to generate a CMD1 or CMD2 BCW sequence upon receiving ZQCL and ZQCS commands from the host, then it will cause the DB to perform the corresponding calibration command. The host also has the ability to directly issue BC06 BCW transactions to send CMD1 and CMD2 commands to the DDR4 data buffers.

## 2.2 Mechanical Outline

Package options include a 53-ball Fine-Pitch BGA (FBGA) with 0.5mm ball pitch, 14 x 5 grid with 17 balls depopulated, 7.5mm x 3.0mm as defined in MO-276 (Issue F, Variation DA). The device pinout supports register link inputs on the left side columns to support easy signal routing to the DDR4 register. Corresponding host side data/strobe balls are placed in a way to match the corresponding pin location on the connector if the device is mounted on the backside of an LRDIMM module. Each  $V_{DD}$  and  $V_{SS}$  is located close to an associated no ball position to allow low cost via technology combined with the small 0.5mm ball pitch.

**Figure 11 — Ball Configuration (TOP VIEW)**



## 2.3 Pinout

Table 18 specifies the pinout for the DDR4DB01. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

**Table 18 — Ball Assignment - 53-ball FBGA, 14 x 5 Grid, TOP VIEW**

|   | A     | B        | C        | D        | E        | F        | G        | H        | J        | K        | L        | M        | N        | P       |
|---|-------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|---------|
| 5 | BCOM3 | BCOM2    | MDQ3     | MDQ2     | MDQ7     | MDQ6     | MDQS0_t  | MDQS0_c  | MDQS1_c  | MDQS1_t  | MDQ1     | MDQ0     | MDQ5     | MDQ4    |
| 4 | BCOM0 | BCOM1    | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ | ALERT_n |
| 3 |       | $V_{DD}$ |          | $V_{DD}$ |          | $V_{DD}$ |          | $V_{DD}$ |          | $V_{DD}$ |          | $V_{DD}$ |          | BVrefCA |
| 2 | BCK_t | BCKE     | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ |          | $V_{SS}$ | ZQCAL   |
| 1 | BCK_c | BODT     | DQ3      | DQ2      | DQ7      | DQ6      | DQS0_t   | DQS0_c   | DQS1_c   | DQS1_t   | DQ1      | DQ0      | DQ5      | DQ4     |

## 2.4 Terminal Functions

**Table 19 — Terminal functions**

| Signal Group               | Signal Name     | Type                              | Description                                                                                                            |
|----------------------------|-----------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------|
| Data buffer control inputs | BODT            | CMOS <sup>1</sup> $V_{REF}$ based | Data buffer on-die termination signal                                                                                  |
|                            | BCKE            | CMOS <sup>1</sup> $V_{REF}$ based | Data buffer clock enable signal for data buffer power management                                                       |
|                            | BCOM[3:0]       | CMOS <sup>1</sup> $V_{REF}$ based | Register communication bus for data buffer programming and control access                                              |
| Clock inputs               | BCK_t, BCK_c    | CMOS differential                 | Differential clock input pair                                                                                          |
| Host Interface             | DQ[3:0]         | CMOS bidirectional                | Host side data lower nibble                                                                                            |
|                            | DQS0_t          |                                   | Host side data strobe for lower nibble                                                                                 |
|                            | DQS0_c          |                                   | Host side data strobe complement for lower nibble                                                                      |
|                            | DQ[7:4]         |                                   | Host side data upper nibble                                                                                            |
|                            | DQS1_t          |                                   | Host side data strobe for upper nibble                                                                                 |
|                            | DQS1_c          |                                   | Host side data strobe complement for upper nibble                                                                      |
| DRAM Interface             | MDQ[3:0]        | CMOS bidirectional                | DRAM side data lower nibble                                                                                            |
|                            | MDQS0_t         |                                   | DRAM side data strobe for lower nibble                                                                                 |
|                            | MDQS0_c         |                                   | DRAM side data strobe complement for lower nibble                                                                      |
|                            | MDQ[7:4]        |                                   | DRAM side data upper nibble                                                                                            |
|                            | MDQS1_t         |                                   | DRAM side data strobe for upper nibble                                                                                 |
|                            | MDQS1_c         |                                   | DRAM side data strobe complement for upper nibble                                                                      |
| Error out                  | ALERT_n         | Open drain                        | When LOW, this output indicates that a parity error was identified associated with the data buffer control bus inputs. |
| Miscellaneous pins         | BVrefCA         | VDD/2                             | Input reference voltage for data buffer control bus receivers                                                          |
|                            | V <sub>DD</sub> | Power Input                       | Power supply voltage                                                                                                   |
|                            | V <sub>SS</sub> | Ground Input                      | Ground                                                                                                                 |
|                            | ZQCAL           | Reference                         | Reference pin for driver calibration                                                                                   |

1. These receivers use BVrefCA as the switching point reference

## 2.5 Buffer Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. Buffer control word (BCW) writes are sent to the DDR4 Data Buffer (DB) from the DDR4 Registering Clock Driver (RCD) as a command sequence through the buffer control bus (BCOM). Section 2.1.7.6 describes BCW write command sequences in detail. The different control words and settings are described in the following sections. Any change to the control words requires some time for the device to settle. For changes to the control word setting, the controller needs to wait  $t_{MRC}$  ( $16t_{CK}$ ) after the last control word access before further access to the DRAM can take place. For any changes to the clock timing (including writes to BC0A/F0BC6x) this settling may take up to  $t_{DLLK}$  time. The command bus must be kept HIGH during that time (BCOM[3:0] = 1010 indicates idle, NOP, command).

The BCW space of the DB is divided into eight function spaces (F0 to F7). In F0 the DDR4 data buffer allocates decoding for 16 4-bit control words (BC00 through BC0F - see Table 20, “4-bit BCW Decoding”) and 15 8-bit control words (BC1x through BCFx). All buffer control words in F1 to F7 are 8-bit. Access to a given 4-bit control word is selected by bits DA4 through DA11 of the BCW write command sequence. The data bits to be written into the 4-bit control words are contained in bits DA0 through DA3 of the BCW write command sequence. Access to a given 8-bit control word (see Table 21, “8-bit BCW Decoding”) is selected by bits DA8 through DA11 of the BCW Write command sequence. The data bits to be written into the 8-bit control words are contained in bits DA0 through DA7 of the BCW command sequence.

For rank specific control words F0 is used for Rank 0, F1 is used for Rank 1, F2 is used for Rank 2 and F3 is used for Rank 3 (with the exception of the per bit lane control words which are in F4 to F7 for ranks 0 to 3 respectively).

During BCW Write commands, the BCKE data buffer input pin must be asserted high. If the CKE power down feature is disabled, the BCKE input is a don't care (either HIGH or LOW). The BODT input can be either HIGH or LOW and is ignored by the data buffer for the purpose of BCW access. Control bus parity is checked during BCW write operations unless parity is disabled in the Parity Control Word. ALERT\_n is asserted and the command is ignored if a parity error is detected.

Control word access must be possible in any valid frequency range in either of the two possible frequency bands.

All timing control words which are affected by a change in clock frequency need to be duplicated for the 2nd frequency context selected with BC0A, DA3.

### 2.5.1 BCW Decoding

The BCW write command sequence is initiated in the data buffer when the BCOM control bus code received at the DDR4 DB is equal to 1100b (BCOM[3:0]=1100). The BCW address and the settings are transmitted over bits DA[11:0] included in the BCW write command sequence in the six clock cycles immediately following the cycle when the 1100b BCOM command is captured. The BCW write command sequence uses one of the six data transfers just mentioned to transmit three function selection bits that select the function space targeted for that particular BCW write command. The reset default state of all control word bits (except vendor specific ones) is '0'. Every time the device is reset, its default state is restored. Stopping the clocks (BCK\_t=BCK\_c=LOW) to put the device in low-power mode will not alter the control word settings as long as BCKE is not HIGH while BCK\_t and BCK\_c are LOW.

Table 20 — 4-bit BCW Decoding

| BCW  | FNC bits |   |   | Address Bit |    |   |   |   |   |   |   |              |   |   |   | Description                            |
|------|----------|---|---|-------------|----|---|---|---|---|---|---|--------------|---|---|---|----------------------------------------|
|      | 2        | 1 | 0 | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3            | 2 | 1 | 0 |                                        |
| BC00 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | setting[3:0] |   |   |   | Host Interface DQ RTT_NOM Control      |
| BC01 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | setting[3:0] |   |   |   | Host Interface DQ RTT_WR Control       |
| BC02 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 1 | setting[3:0] |   |   |   | Host Interface DQ RTT_PARK Control     |
| BC03 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 1 | setting[3:0] |   |   |   | Host Interface DQ Driver Control Word  |
| BC04 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 1 | 0 | setting[3:0] |   |   |   | DRAM Interface MDQ RTT Control Word    |
| BC05 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 1 | 0 | setting[3:0] |   |   |   | DRAM Interface MDQ Driver Control Word |
| BC06 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 1 | 1 | command[3:0] |   |   |   | Command Space Control Word             |
| BC07 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 0 | 1 | 1 | setting[3:0] |   |   |   | Rank Presence Control Word             |
| BC08 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 0 | 0 | setting[3:0] |   |   |   | Rank Selection Control Word            |
| BC09 | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 0 | 0 | setting[3:0] |   |   |   | Power Saving Settings Control Word     |
| BC0A | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 0 | 1 | setting[3:0] |   |   |   | LRDIMM Operating Speed                 |
| BC0B | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 0 | 1 | setting[3:0] |   |   |   | Operating Voltage Control Word         |
| BC0C | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 1 | 0 | setting[3:0] |   |   |   | Buffer Training Mode Control Word      |
| BC0D | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 1 | 0 | setting[3:0] |   |   |   | Reserved for future use                |
| BC0E | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 1 | 1 | setting[3:0] |   |   |   | Parity Control Word                    |
| BC0F | 0        | 0 | 0 | 0           | 0  | 0 | 0 | 0 | 1 | 1 | 1 | setting[3:0] |   |   |   | Error Status Word                      |

Table 21 — 8-bit BCW Decoding

| BCW        | FNC bits |   |   | Address Bit |    |   |   |              |   |   |   |   |   |   |   | Description                                                                                   |
|------------|----------|---|---|-------------|----|---|---|--------------|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------|
|            | 2        | 1 | 0 | 11          | 10 | 9 | 8 | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                               |
| F[7:0]BC7x | x        | x | x | 0           | 1  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Function Space Selector Control Word                                                          |
| F0BC1x     | 0        | 0 | 0 | 0           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Buffer Configuration Control Word                                                             |
| F0BC6x     | 0        | 0 | 0 | 0           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Fine Granularity Frequency Operating Speed Control Word                                       |
| F0BCCx     | 0        | 0 | 0 | 1           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0 |
| F0BCDx     | 0        | 0 | 0 | 1           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0 |
| F0BCEx     | 0        | 0 | 0 | 1           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2 |
| F0BCFx     | 0        | 0 | 0 | 1           | 1  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2 |
| F1BCCx     | 0        | 0 | 1 | 1           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1 |
| F1BCDx     | 0        | 0 | 1 | 1           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1 |
| F1BCEx     | 0        | 0 | 1 | 1           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3 |
| F1BCFx     | 0        | 0 | 1 | 1           | 1  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3 |

Table 21 — 8-bit BCW Decoding

| BCW           | FNC bits |   |   | Address Bit |    |   |   |              |   |   |   |   |   |   |   | Description                                                                       |
|---------------|----------|---|---|-------------|----|---|---|--------------|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------|
|               | 2        | 1 | 0 | 11          | 10 | 9 | 8 | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                   |
| F[3:0]BC2x    | 0        | x | x | 0           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower Nibble DRAM Interface Receive Enable Training Control Word for Ranks 0 to 3 |
| F[3:0]BC3x    | 0        | x | x | 0           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper Nibble DRAM Interface Receive Enable Training Control Word for Ranks 0 to 3 |
| F[3:0]BC4x    | 0        | x | x | 0           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower Nibble MDQS Read Delay Control Word for Ranks 0 to 3                        |
| F[3:0]BC5x    | 0        | x | x | 0           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper Nibble MDQS Read Delay Control Word for Ranks 0 to 3                        |
| F[3:0]BC8x    | 0        | x | x | 1           | 0  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower Nibble MDQ-MDQS Write Delay Control Word for Ranks 0 to 3                   |
| F[3:0]BC9x    | 0        | x | x | 1           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper Nibble MDQ-MDQS Write Delay Control Word for Ranks 0 to 3                   |
| F[3:0]BCAx    | 0        | x | x | 1           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Lower Nibble DRAM Interface Write Leveling Control Word for Ranks 0 to 3          |
| F[3:0]BCBx    | 0        | x | x | 1           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper Nibble DRAM Interface Write Leveling Control Word for Ranks 0 to 3          |
| F4BC0x        | 1        | 0 | 0 | 0           | 0  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | MRS0 Snooped Settings                                                             |
| F4BC1x        | 1        | 0 | 0 | 0           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | MRS1 Snooped Settings                                                             |
| F4BC2x        | 1        | 0 | 0 | 0           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | MRS2 Snooped Settings                                                             |
| F4BC3x        | 1        | 0 | 0 | 0           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | MRS3 Snooped Settings                                                             |
| F4BC4x        | 1        | 0 | 0 | 0           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | MRS4 Snooped Settings                                                             |
| F4BC5x        | 1        | 0 | 0 | 0           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | MRS5 Snooped Settings                                                             |
| F4BC6x        | 1        | 0 | 0 | 0           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | MRS6 Snooped Settings                                                             |
| F5BC0x = MPR0 | 1        | 0 | 1 | 0           | 0  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [7:0] for UI0                                              |
| F5BC1x = MPR1 | 1        | 0 | 1 | 0           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [15:8] for UI1                                             |
| F5BC2x = MPR2 | 1        | 0 | 1 | 0           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [23:16] for UI2                                            |
| F5BC3x = MPR3 | 1        | 0 | 1 | 0           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [31:24] for UI3                                            |
| F5BC4x        | 1        | 0 | 1 | 0           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Reserved                                                                          |
| F5BC5x        | 1        | 0 | 1 | 0           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Host Interface Vref Control Word                                                  |
| F5BC6x        | 1        | 0 | 1 | 0           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | DRAM Interface Vref Control Word                                                  |
| F6BC0x = MPR4 | 1        | 1 | 0 | 0           | 0  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [39:32] for UI4                                            |
| F6BC1x = MPR5 | 1        | 1 | 0 | 0           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [47:40] for UI5                                            |
| F6BC2x = MPR6 | 1        | 1 | 0 | 0           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [55:48] for UI6                                            |
| F6BC3x = MPR7 | 1        | 1 | 0 | 0           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | Upper & Lower MPR bits [63:56] for UI7                                            |
| F6BC4x        | 1        | 1 | 0 | 0           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | Buffer Training Configuration Control Word                                        |
| F6BC5x        | 1        | 1 | 0 | 0           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | Buffer Training Status Word                                                       |
| F7BC0x ..C3x  | 1        | 1 | 1 | 0           | 0  | x | x | setting[7:0] |   |   |   |   |   |   |   | Error Log Registers                                                               |
| F[7:4]BC8x    | 1        | x | x | 1           | 0  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | MDQ0/4-Read Delay Control Word for Ranks 0 to 3                                   |
| F[7:4]BC9x    | 1        | x | x | 1           | 0  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | MDQ1/5-Read Delay Control Word for Ranks 0 to 3                                   |
| F[7:4]BCAx    | 1        | x | x | 1           | 0  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | MDQ2/6-Read Delay Control Word for Ranks 0 to 3                                   |
| F[7:4]BCBx    | 1        | x | x | 1           | 0  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | MDQ3/7-Read Delay Control Word for Ranks 0 to 3                                   |
| F[7:4]BCCx    | 1        | x | x | 1           | 1  | 0 | 0 | setting[7:0] |   |   |   |   |   |   |   | MDQ0/4-MDQS Write Delay Control Word for Ranks 0 to 3                             |
| F[7:4]BCDx    | 1        | x | x | 1           | 1  | 0 | 1 | setting[7:0] |   |   |   |   |   |   |   | MDQ1/5-MDQS Write Delay Control Word for Ranks 0 to 3                             |
| F[7:4]BCEx    | 1        | x | x | 1           | 1  | 1 | 0 | setting[7:0] |   |   |   |   |   |   |   | MDQ2/6-MDQS Write Delay Control Word for Ranks 0 to 3                             |
| F[7:4]BCFx    | 1        | x | x | 1           | 1  | 1 | 1 | setting[7:0] |   |   |   |   |   |   |   | MDQ3/7-MDQS Write Delay Control Word for Ranks 0 to 3                             |