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DDR5 Registering Clock Driver Definition (DDR5RCD02)

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DDR5 REGISTERING CLOCK DRIVER DEFINITION (DDR5RCD02)

(From JEDEC Board Ballot JCB-22-43, item 339.98D and JCB-23-02, item 339.98E, formulated under the cognizance of JC-40, Digital Logic).

1 Scope

This standard defines specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR5 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR5 RDIMM and LRDIMM applications. The DDR5RCD02 Device ID is DID = 0x0052.

The terms 'Registering Clock Driver', 'RCD', 'register', or 'device' are used interchangeably to refer to this device in the remainder of this standard.

The purpose is to provide a standard for the DDR5RCD02 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR5RCD02 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Mechanical Outline

Package options include a 240-ball Flip-Chip Fine-Pitch BGA (FCBGA) with 0.60 mm/0.70 mm ball pitch, 14 x 19 grid. The package has a number of depopulated balls. Package size is 8.70 mm x 13.50 mm as defined in MO-330 Issue A, Variation 10013.50x8.70-70x6030-240A¹. The device pinout supports outputs on the top and outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector.

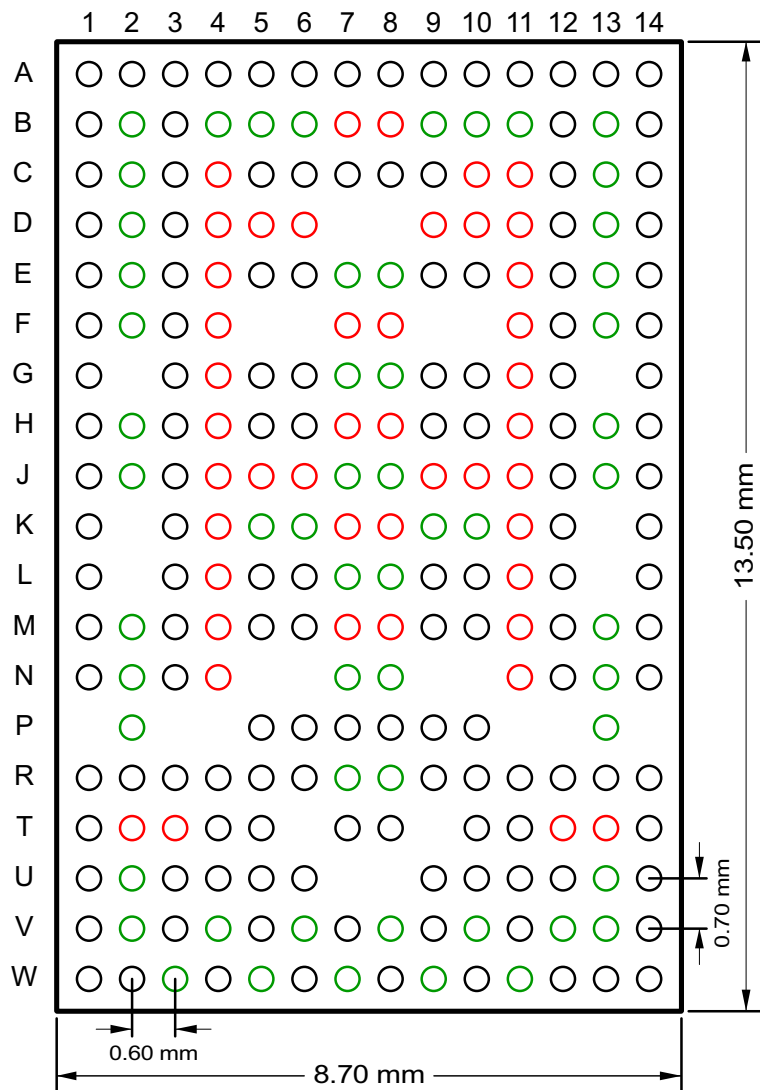


Figure 1 — Ball Configuration, TOP VIEW

Ball pitch: 0.60 mm x 0.70 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm)
X-ray view from topside

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5RCD02 must comply with a minimum thickness of 0.80 mm.

2.1 Pinout

Table 1 specifies the pinout for the DDR5RCD02.

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	A
B	QB CA1_A	V _{SS}	QB CA9_A	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	QB CA9_B	V _{SS}	QB CA1_B	B
C	QB CA6_A	V _{SS}	QB CA8_A	V _{DD}	ZQ CAL	SCL	DERROR _IN_A_n	DERROR _IN_B_n	SDA	V _{DDIO}	V _{DD}	QB CA8_B	V _{SS}	QB CA6_B	C
D	QB CA5_A	V _{SS}	QB CA2_A	V _{DD}	V _{DD}	V _{DD}			V _{DD}	V _{DD}	V _{DD}	QB CA2_B	V _{SS}	QB CA5_B	D
E	QB CA0_A	V _{SS}	QB CA4_A	V _{DD}	QBCK _A_c	QBCK _A_t	V _{SS}	V _{SS}	QBCK _B_t	QBCK _B_c	V _{DD}	QB CA4_B	V _{SS}	QB CA0_B	E
F	QBCS0 _A_n	V _{SS}	QBCS1 _A_n	V _{DD}			V _{DD}	V _{DD}			V _{DD}	QBCS1 _B_n	V _{SS}	QBCS0 _B_n	F
G	QA CA11_A		QA CA13_A	V _{DD}	QDCK _A_c	QDCK _A_t	V _{SS}	V _{SS}	QDCK _B_t	QDCK _B_c	V _{DD}	QA CA13_B		QA CA11_B	G
H	QA CA9_A	V _{SS}	QA CA12_A	V _{DD}	RFU	RFU	V _{DD}	V _{DD}	RFU	RFU	V _{DD}	QA CA12_B	V _{SS}	QA CA9_B	H
J	QA CA10_A	V _{SS}	QA CA3_A	V _{DD}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{DD}	QA CA3_B	V _{SS}	QA CA10_B	J
K	QA CA6_A		QA CA7_A	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	QA CA7_B		QA CA6_B	K
L	QA CA1_A		QA CA4_A	V _{DD}	QA CA2_A	QA CA8_A	V _{SS}	V _{SS}	QA CA8_B	QA CA2_B	V _{DD}	QA CA4_B		QA CA1_B	L
M	QA CA5_A	V _{SS}	QA CA0_A	V _{DD}	QACK _A_c	QACK _A_t	V _{DD}	V _{DD}	QACK _B_t	QACK _B_c	V _{DD}	QA CA0_B	V _{SS}	QA CA5_B	M
N	QACS0 _A_n	V _{SS}	QACS1 _A_n	V _{DD}			V _{SS}	V _{SS}			V _{DD}	QACS1 _B_n	V _{SS}	QACS0 _B_n	N
P		V _{SS}			QCCK _A_c	QCCK _A_t	QLBD	QLBS	QCCK _B_t	QCCK _B_c			V _{SS}		P
R	BCS _A_n	BCOM1 _A	BCOM2 _A	BRST _A_n	BCK _A_c	BCK _A_t	V _{SS}	V _{SS}	BCK _B_t	BCK _B_c	BRST _B_n	BCOM2 _B	BCOM1 _B	BCS _B_n	R
T	BCOM0 _A	V _{DD}	V _{DD}	DCS1 _A_n	QRST _A_n		DCK_t	DCK_c		QRST _B_n	DCS0 _B_n	V _{DD}	V _{DD}	BCOM0 _B	T
U	DCA0 _A	V _{SS}	DCS0 _A_n	DLBD_A	DLBS_A	ALERT _n			DRST_n	DLBS_B	DLBD_B	DCS1 _B_n	V _{SS}	DPAR _B	U
V	DCA1 _A	V _{SS}	DCA3 _A	V _{SS}	DPAR _A	V _{SS}	DCA6 _A	V _{SS}	DCA1 _B	V _{SS}	DCA3 _B	V _{SS}	V _{SS}	DCA6 _B	V
W	NU	DCA2 _A	V _{SS}	DCA4 _A	V _{SS}	DCA5 _A	V _{SS}	DCA0 _B	V _{SS}	DCA2 _B	V _{SS}	DCA4 _B	DCA5 _B	NU	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5] , Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).
Clock outputs	Q[D:A]CK_[B:A]_t Q[D:A]CK_[B:A]_c	POD differential	Clock outputs to the DRAMs. Four copies per channel.
Loopback	QLBD QLBS	POD	Loopback outputs to Host QLBD - loopback Data QLBS - loopback Strobe
Reset output	QRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD QRST_n to reset the DDR5 SDRAM on all DIMM topologies. The QRST outputs are asserted at power up. RCD requires MRW to independently de-assert to allow staggering of sub-channels.
Error out	ALERT_n	POD	When LOW, this output indicates that a parity error was identified associated with the CA inputs when parity checking is enabled or that the DERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not. One signal for the two channels.
SidebandBus pins ¹	SDA	Open drain or push-pull I/O ²	SidebandBus Data
	SCL	CMOS input ³	SidebandBus Clock
	VDDIO	Power input	SidebandBus power input

Table 2 — Terminal Functions (cont'd)

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V _{DD}	Power Input	Power supply voltage
	V _{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in RCD
NOTE 1 SA pins are not required for DDR5RCD02 as the address will be hard-coded. Refer to Section 7.5.1, “Target Address,” on page 88 for details.			
NOTE 2 SDA driver operation is dynamic. Depending on the SidebandBus mode of operation (I ² C RW25[5] = ‘0’ or I3C Basic RW25[5] = ‘1’), and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.			
NOTE 3 These inputs are 1.0 V inputs.			

Naming Convention:

Input Example:

DCAy_N - where ‘y’ is the signal number and ‘N’ is the sub-channel.

Output Example:

QxCAY_N - where ‘y’ is the signal number, ‘x’ is the output copy (A or B) and ‘N’ is the sub-channel.

3 Device Standard

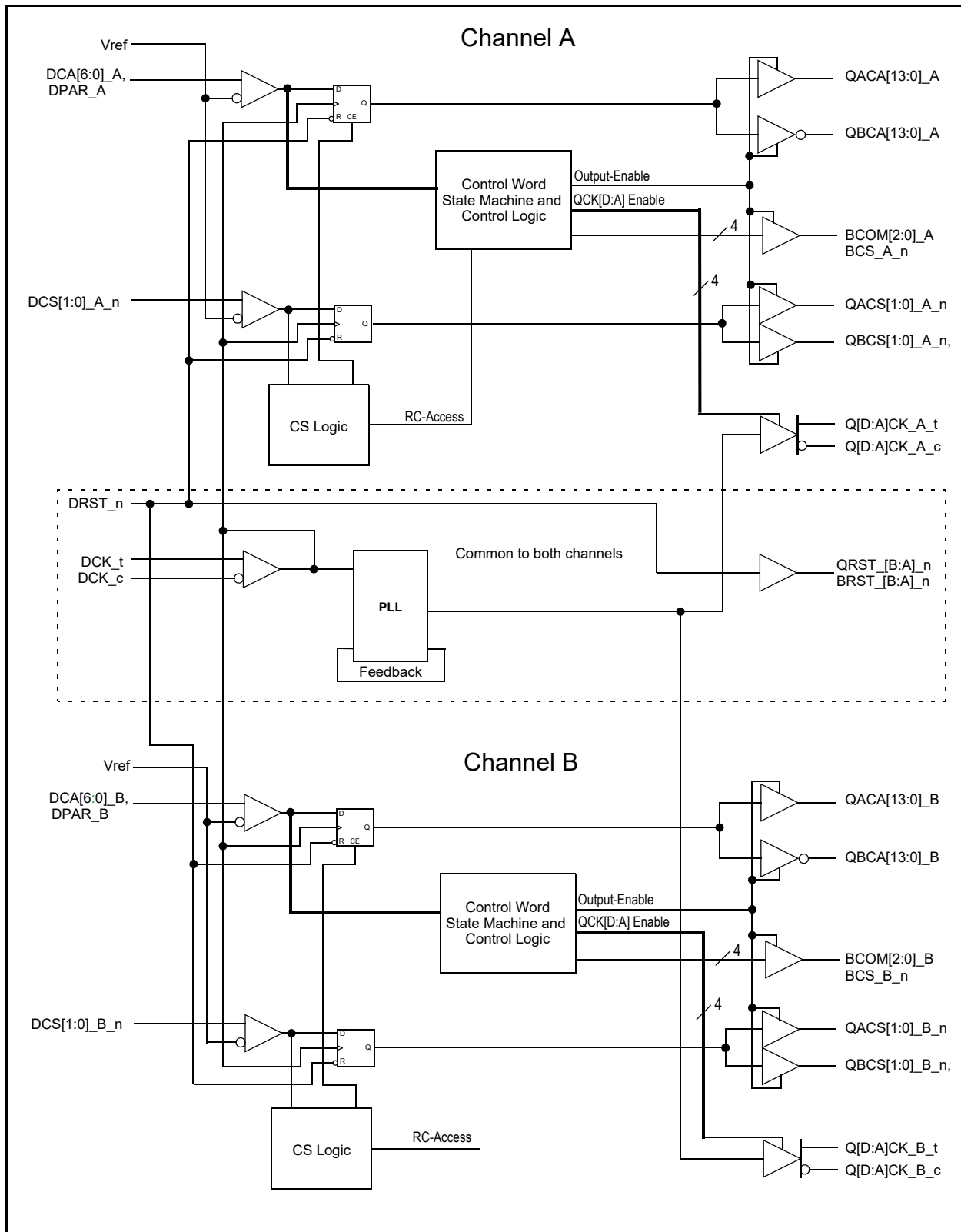
3.1 Description

The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.



3.2 Logic Diagram Positive Logic



3.3 Register Operation

3.3.1 Chip Select Operation

The component has two chip select inputs per channel, DCS0_n and DCS1_n, and two copies of each chip select output, QCS0_A_n, QCS1_A_n, QCS0_B_n and QCS1_B_n. Commands are sent to a single rank or multiple ranks, as determined by the DCS[1:0]_n inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

Table 3 — DCS - QxCS Mapping

Input CS	Output CS
DCS0_N_n	QxCS0_N_n
DCS1_N_n	QxCS1_N_n

3.3.2 ODT Operation

DDR5 does not have a separate ODT (On Die Termination) signal going to the DIMM or the DRAMs. The ODT control is encoded into the chip selects. All commands that utilize the data bus require 2UI on the DCA bus in order to transfer the appropriate number of command and addressing bits. This requirement is used to signal ODT control by how the chip selects are asserted for the two UI.

Table 4 — ODT Encoding on the Chip Select

DCS_n on 1st UI	DCS_n on 2nd UI	QxCS[1:0]_n	DRAM DQ Terminations
Active	Inactive	Target of command	Read: none (device drives data) Write: RTT_WR.
Active	Active	Non-Target Termination should be applied.	Read: RTT_NOM_RD Write: RTT_NOM_WR
Inactive	Inactive	DRAM ignores commands and the Parked termination will be maintained	RTT_PARK
Inactive	Active	Illegal	Illegal

The host controller will determine the termination at the time of the command, by activating the chip selects appropriately.

3.3.2.1 Data Buffer DQ Bus Termination in LRDIMM Application

The RCD supports DQ bus termination in LRDIMM applications. DDR5 does not have a discrete ODT signal. The ODT function is encoded on the Chip Select for RD, WR, and MRR commands. A RD, WR, MRW or MRR command will normally have the BCS_n signal active for only the first UI of the command. The data buffers will terminate the host bus as is appropriate for the command (RTT_WR for write, and driving the bus for reads).

3.3.2.1 Data Buffer DQ Bus Termination in LRDIMM Application (cont'd)

The DIMM terminations for DRAM and Data Buffer are shown in Table 5 and Table 6.

Table 5 — DIMM Termination Write

DCS0		DCS1		BCS		DRAM Termination		Buffer Termination
1st UI	2nd UI	1st UI	2nd UI	1st UI	2nd UI	Rank 0	Rank 1	
L	H	H	H	L	H	RTT_WR	RTT_PARK	RTT_WR
L	H	L	L	L	H	RTT_WR	RTT_NOM_WR	RTT_WR
H	H	L	H	L	H	RTT_PARK	RTT_WR	RTT_WR
L	L	L	H	L	H	RTT_NOM_WR	RTT_WR	RTT_WR
L	L	H	H	L	L	RTT_NOM_WR	RTT_PARK	RTT_NOM_WR
H	H	L	L	L	L	RTT_PARK	RTT_NOM_WR	RTT_NOM_WR
L	L	L	L	L	L	RTT_NOM_WR	RTT_NOM_WR	RTT_NOM_WR

Table 6 — DIMM Termination Read

DCS0		DCS1		BCS		DRAM Termination		Buffer Termination
1st UI	2nd UI	1st UI	2nd UI	1st UI	2nd UI	Rank 0	Rank 1	Host-side DQ
L	H	H	H	L	H	Target	RTT_PARK	Target
L	H	L	L	L	H	Target	RTT_NOM_RD	Target
H	H	L	H	L	H	RTT_PARK	Target	Target
L	L	L	H	L	H	RTT_NOM_RD	Target	Target
L	L	H	H	L	L	RTT_NOM_RD	RTT_PARK	RTT_NOM_RD
H	H	L	L	L	L	RTT_PARK	RTT_NOM_RD	RTT_NOM_RD
L	L	L	L	L	L	RTT_NOM_RD	RTT_NOM_RD	RTT_NOM_RD

If the DCS_n signal is active during the 2nd UI of a command, it indicates a non-target termination for the DIMM. The command is targeting a different DIMM and the DRAMs or data buffers should terminate with either RTT_NOM_WR for writes or RTT_NOM_RD for reads.

For a non-target operation, the DRAMs or data buffers should remain in RTT_PARK, the command will not be sent on the BCOM bus at all. The RCD will not have received any DCS_n signals active in this case and will see Deselects.

3.3.3 QCA Bus Operation

Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this:

- If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked.
- During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank.
- When DRAM interface Block MR Mode is enabled [RW01\[1\]](#) = 0.
- When CA Pass-through mode is enabled [RW00\[2\]](#) = 1.

3.3.4 QCS Operation

Under normal operation the RCD passes the DCS signals through to the QCS outputs. There are several exceptions to this:

- If the register detects a parity error with parity checking enabled, on a one-cycle command or the 1st UI of two-cycle command, the DCS signal is not passed through, and the QCS outputs remain inactive.
- If the register detects a parity error with parity checking enabled, on the 2nd UI of a two-cycle command, the same QCS outputs that were active on the 1st UI will be active on the 2nd UI. This causes the command to be canceled in the DRAM. For read and write commands it causes the command to be converted to non-target termination.
- When DRAM interface Block MR Mode is enabled $RW01[1] = 0$.
- When CA Pass-through mode is enabled $RW00[2] = 1$.

3.3.5 Output Inversion and Mirroring

Output Inversion is enabled by default, after DRST_n is de-asserted, to reduce simultaneous output switching current.

- All QACA[13:0]_[B:A] outputs will follow the equivalent inputs. All QBCA[13:0]_[B:A] outputs will be inverted. In other words, when sending commands, the “B” copy will be the invert of the “A” copy.
- When no commands are being sent, both the “A” and “B” copies will drive HIGH.
- The DRAM devices connected to the “B” outputs will un-invert the signals internally before using them. This eliminates the need for the host controller to send separate MRW commands for the two CA output sets, and allows every CA output to be inverted on the “B” set.

Address mirroring is also handled by the DRAM device, so there is no RCD requirements for mirroring.

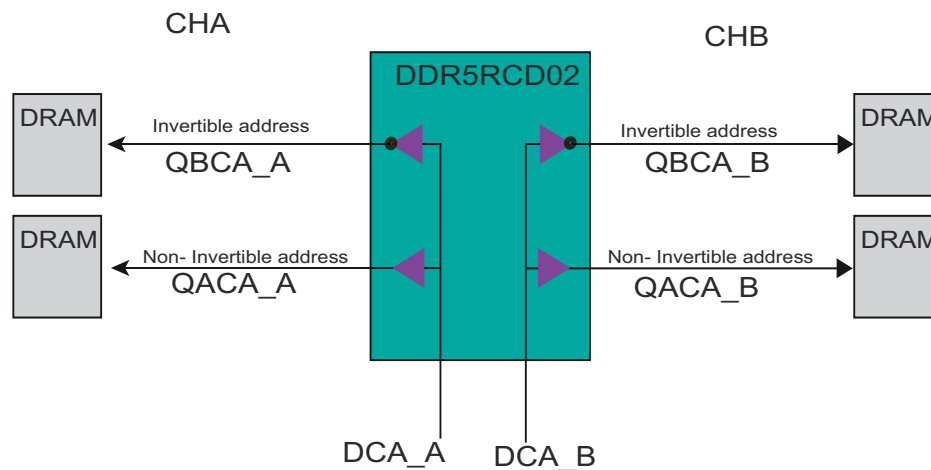


Figure 2 — RCD Output Inversion

3.3.6 ZQ Calibration

The RCD snoops the MPC command to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration commands initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the RCD's calibration procedure, and ZQCal Latch captures the result and loads it into the RCD's drivers.

A ZQCal Start command may be issued anytime the DDR5 SDRAM is not in a power-down state. There are two timing parameters associated with ZQ Calibration. t_{ZQCAL} is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. t_{ZQLAT} is the time from when the ZQCal Latch MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after t_{ZQCAL} has expired and all CA bus operations have completed. The CA Bus must maintain a Deselect state during t_{ZQLAT} to allow CA ODT calibration settings to be updated.

ZQCal commands are issued independently on a sub-channel level. After a ZQCal Start and until t_{ZQCAL} finishes, neither another ZQCal Start nor a ZQCal Latch is allowed on this same sub-channel.

To use the ZQ calibration function, a $240\ \Omega \pm 1\%$ tolerance external resistor must be connected between the ZQ pin and VSS.

3.3.7 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility, it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR5 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR5 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence, this DDR5 register mechanism does not by itself allow mixing DDR5 RDIMMs and LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR5 register supports a programmable latency adder of 0 nCK, 1 nCK, 2 nCK, 3 nCK or 4 nCK for all DRAM commands—see conceptual diagram in Figure 3. The power-up default is 0 nCK latency adder.

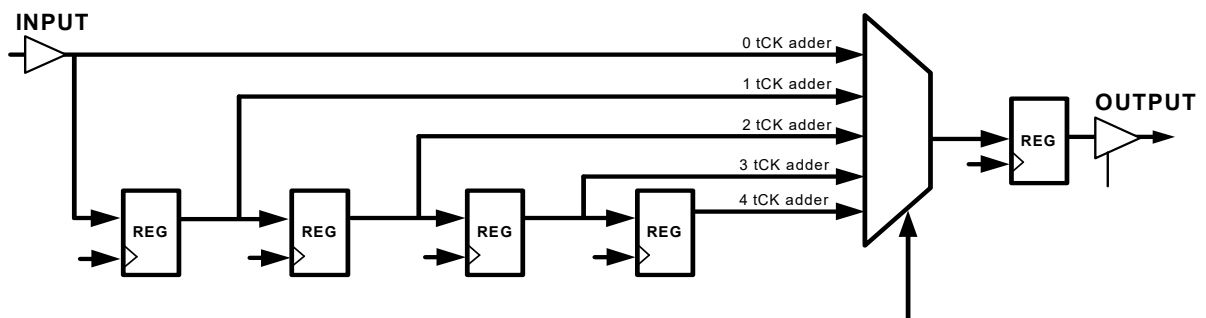


Figure 3 — Latency Equalizer Delays

With a latency adder enabled, the DDR5 register will delay assertion of the QxCsSy_N_n and QxCaY_N outputs by the corresponding number of clock cycles. The output timing is determined by the Command Latency Adder control word [RW11](#) regardless of whether the device has parity checking enabled or disabled.

3.3.8 Per-group Output Delay Control

The RCD supports output delay control for output signal groups defined and located in [RW12](#) to [RW1E](#). The output delay settings are incremental CK fractions of $1/64$ tCK. Each signal group can be enabled or disabled independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable. The output delay feature controlled by [RW12](#) to [RW1E](#) is not supported when the RCD is configured in Test Frequency mode (Band 2, [RW05\[7\] = 1](#)) or in PLL bypass mode ([RW05\[3:0\] = 1111](#)).

3.3.9 Per-bit QCA Output Delay Control

In DDR5RCD02, fine adjustment of the phase of individual QCA bit lanes relative to QCK is required. For this purpose, the host controller can utilize the per-bit QCA output delay control words in [PG\[5\]RW\[7B:60\]](#) to control the phase of A-copy and B-copy QCA bits respectively. Since all bits within a copy are generally aligned by routing, only a small range of [0, 40ps] is provided for fine-grained adjustment of individual bit lane delay differences. A positive delay in these control words means that the particular lane requires slightly more delay than the previously established QCA delay in [RW1B](#) and [RW1C](#) for the entire copy.

3.3.10 Power Down Operation

DDR5 does not have a separate CKE signal going to the DIMM or the DRAMs. Power Down Entry, including Self Refresh, is signaled via a single UI command. Following the Power Down Entry command, the CS signal effectively becomes the equivalent of the CKE signal. An inactive CS keeps the DRAM devices in the Power Down state. CS going active will take the DRAMs out of the Power Down state. A NOP command is placed on the CA bus along with CS going active so that no commands are executed by the DRAM devices. DRAMs can be put in Power Down mode with or without non-target ODT control, see Chapter 4.

3.3.11 VHost Mode

The Virtual Host mode or “VHost mode” allows a sequence of commands to be sent on the DRAM interface without receiving commands via the host interface. Commands to be sent on the DRAM interface are programmed by writing RCD control words. The intention is to operate this RCD feature via SidebandBus in a test environment. VHost mode is not intended for normal operation. A sequence of commands is programmed into the RCD, then executed by writing a START MRW bit.

Virtual host mode has the following features:

- Up to 4 commands may be programmed.
- Each command may be a 1 or 2 UI command.
- Control words specify the complete CA[13:0] bus and the two chip selects for each UI of the commands.
- There is a programmable number of clocks between commands, programmed separately for the spacing between each command.
- Command spacing can be 2, 4, 8, 16, 64, 256, or 1024 clock.
- Following the last command, the sequence may then optionally repeat starting at command 0, 1, 2, or 3.
- Shorter sequences can be supported by programming Deselects (neither chip select active) for some of the commands.
- Non-target termination can be signaled by programming the chip select to be active for both UI of a command that supports non-target termination.

Each command is programmed using four 8-bit control words, to specify the state of CA[13:0], CS0_n and CS1_n for each of the 2 UI. For a 1UI command, the 2nd UI is programmed as a Deselect, with both chip selects inactive. Note that two back to back one UI commands can be programmed instead of a 2UI command, but these will always be back to back, with no programmable spacing.

3.3.11 VHost Mode (cont'd)

There are four three-bit delay fields to specify the delay between commands 0 and 1, commands 1 and 2, commands 2 and 3, and command 3 to start of the repeat sequence.

Following the execution of command 3, the sequence will optionally repeat. The sequence can repeat starting at any command (0 through 3) and will continue again through command 3.

16 control words specify the four commands (4 registers each). Two registers specify the gap between commands. One register specifies the command to repeat from and enables repeating. One register contains a start bit for each channel. Writing a 1 to a start bit begins the sequence on that channel. Writing a 0 stops the sequence. The sequencer is common to the two channels, so the sequence cannot be started on the two channels at different times. The commands operate in either 1N or 2N mode as specified by the existing 1N/2N mode bit. VHost Commands are sent across the BCOM bus to the data buffers. VHost is not supported during SRE/PDE/Initialization or when any training mode is enabled. The commands processed by the VHost logic are not interpreted by the RCD. For example, if the programmed commands include PDE or SRE, those commands will be sent to the DRAMs but they will not cause the RCD to power down. VHost settings can-not be modified while the VHost state machine is running. The RCD will auto stop after cmd3 executes if repeat is not enabled. RST, DCK signals must be applied on the host interface during VHost mode.

3.3.11.1 VHost Lockout mode

When the RCD receives an In-band MRW to [RW01](#), the RCD will Lockout the VHost mode until the next DRST_n assertion. SMBus sideband write to RW01 will not trigger the lockout mechanism.

Suppliers must guarantee a permanent lock out with a fuse option.

3.3.12 Transparent Mode

The DDR5RCD02 supports a transparent mode feature of the data buffer that enables testing of LRDIMMs. The RCD will disable parity checking automatically when this mode is entered.

To enter transparent mode, the host first sends an MRW command with [RW82\[0\]](#) = 1 to enable transparent mode in the DDR5DB02. Then it sends an MRW command with [RW00\[7\]](#) = 1 to enable transparent mode in the RCD.

While in transparent mode, the DDR5DB02 does not interpret BCS_n and BCOM commands. For BCS_n input value of “1” and BCOM[2:0] input values of “111”, it directs the data flow from host interface to DRAM interface. For BCS_n input value of “1” and BCOM[2:0] input values of “000”, it directs the data flow from DRAM interface to host interface. Any other input values of BCS_n and BCOM[2:0] are invalid.

While in transparent mode, the RCD drives BCS_n statically to “1” and BCOM[2:0] statically to “111” (DES) when the DPAR input is LOW, and BCS_n to “1” and BCOM[2:0] to “000” when the DPAR input is HIGH. All output signals in the RCD, other than BCS_n and BCOM[2:0], continue working as they do in the normal mode of operation. In other words, all the RCD features and functions not directly related to DPAR, BCS_n and BCOM[2:0] remain operational in transparent mode. In addition, all the clock frequencies and PLL operational modes available in low-speed test mode and normal operation mode will be supported in transparent mode. Input DPAR_A controls outputs BCOM[2:0]_A and input DPAR_B controls outputs BCOM[2:0]_B, correspondingly.

To exit transparent mode, the host sends an MRW command with [RW00\[7\]](#) = 0 to exit RCD transparent mode following by issuing a Data Buffer reset command via [RW04](#) to exit DDR5DB02 transparent mode.

3.3.13 CA Validation Pass-Through Mode

To facilitate DRAM or RCD validation the RCD will be required to support a validation pass-through mode. In this mode, the DCA signals are passed through to QCA, regardless of DCS assertion. In this mode, the DCS0_n and DCS1_n signals are passed through to QCS0_n and QCS1_n respectively, regardless of DCA signal state. Parity checking must be disabled prior to and during validation pass-through mode. Validation pass-through mode is entered when [RW07\[4\]](#)=1. When [RW07\[5\]](#)=1 in CA Validation Pass-through mode, all MRW which write to the RCD are blocked and further configuration is expected via the SMBus. This SMBus is not required to be driven by the controller.

3.3.13 CA Validation Pass-Through Mode (cont'd)

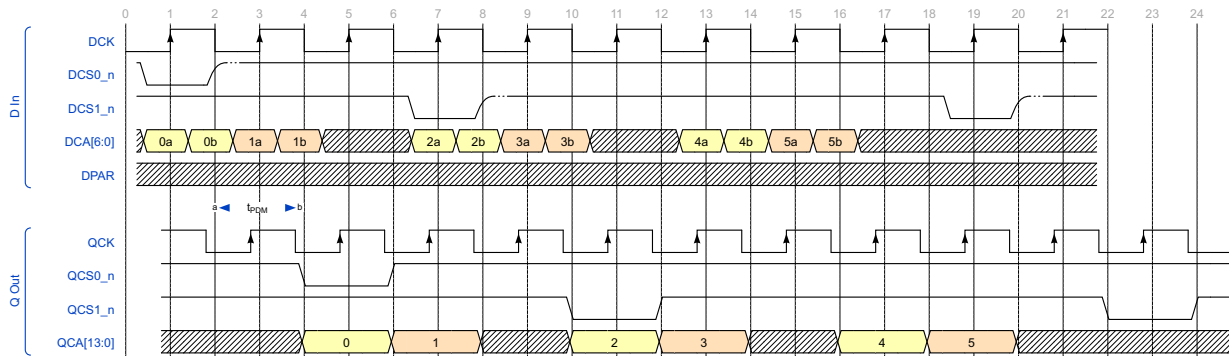


Figure 4 — Validation Pass-Through Mode - DDR

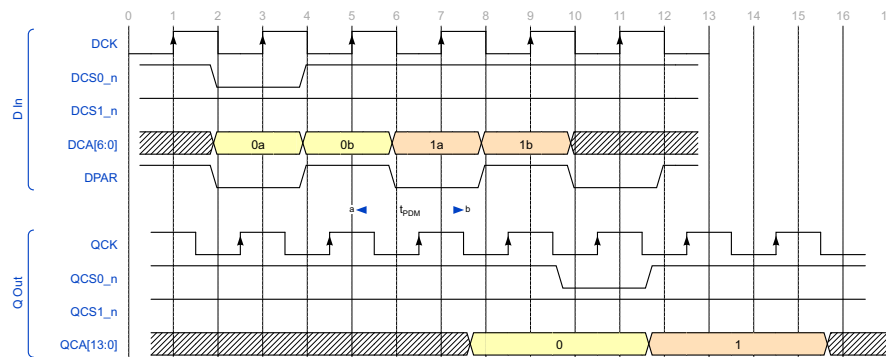


Figure 5 — Validation Pass-Through Mode - SDR1

Similar to CA Pass-Through Mode described in Section 5.2.3, when Validation Pass-Through Mode is enabled in SDR Mode, the DPAR signal will be used to indicate 1st UI QCA[6:0] (DPAR = LOW) and 2nd UI QCA[13:7] (DPAR = HIGH).

3.3.14 DRAM Interface and Data Buffer Interface Training Support

In order for the Host to train the DRAM and Data Buffer interfaces, the RCD will support two Pass Through modes: CA Pass-Through mode, described in Section 5.2.3, and BCOM Pass-Through mode, described in Section 5.2.5.

3.4 Command Address Bus

The DDR5RCD02 can support two data rates on the Host Command Address signals. The first setting is Double Data Rate (DDR) on the DCA with 1N timing on the QCA. The second is Single Data Rate (SDR) on DCA with 2N timing on the QCA to the DRAM interface. Chip Select is SDR for both settings on DCA and QCA.

Table 7 — Command Address Rates

RW00[1:0]	DCA	QCA
00	SDR1	2N timing (extra setup time)
01	DDR	1N timing
10	SDR2	2N timing (extra hold time)

3.4.1 Double Data Rate DCA

The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6.

Table 8 — DDR CA Mapping DCA to QCA

UI	DCA0	DCA1	DCA2	DCA3	DCA4	DCA5	DCA6
0	QCA0	QCA1	QCA2	QCA3	QCA4	QCA5	QCA6
1	QCA7	QCA8	QCA9	QCA10	QCA11	QCA12	QCA13

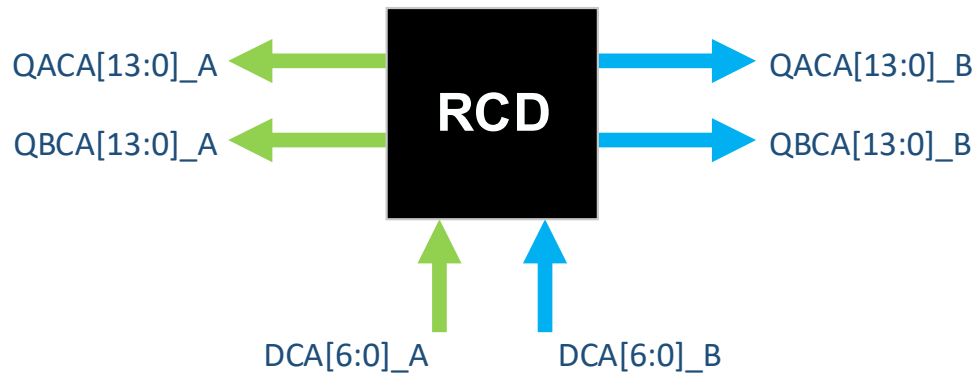
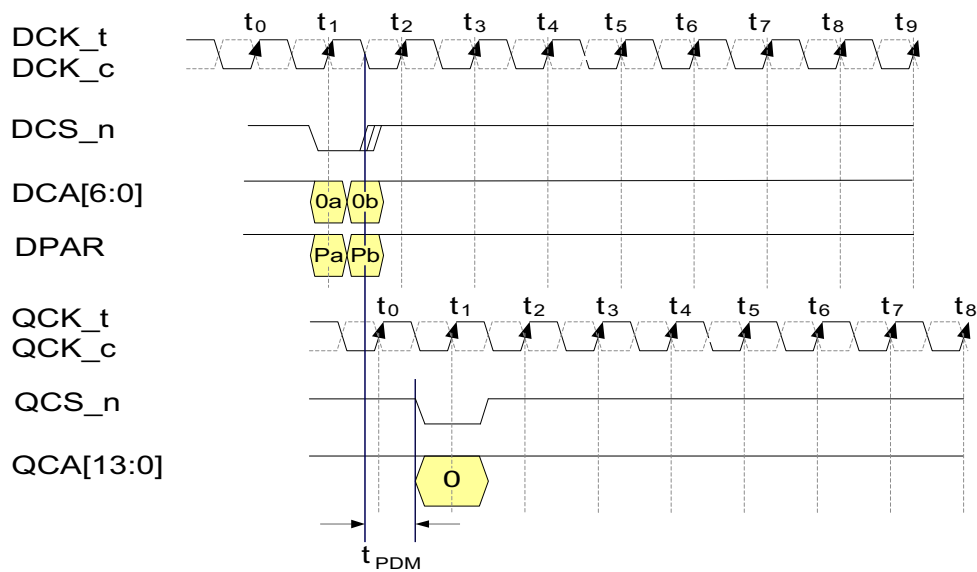


Figure 6 — RCD DCA and QCA Ports

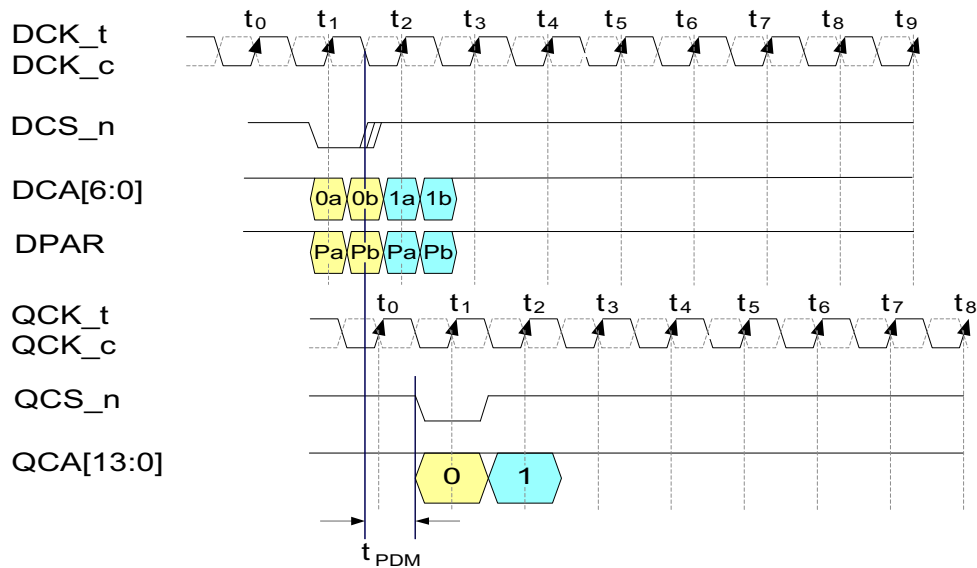
The following timing diagrams in Figures 7, 8, and 9 show the timing relationship from the Dn inputs to the Qn outputs for a 1UI command, a 2UI command, and multiple commands.

3.4.1 Double Data Rate DCA (cont'd)



NOTE Timing Diagram for 0 nCK command latency adder.

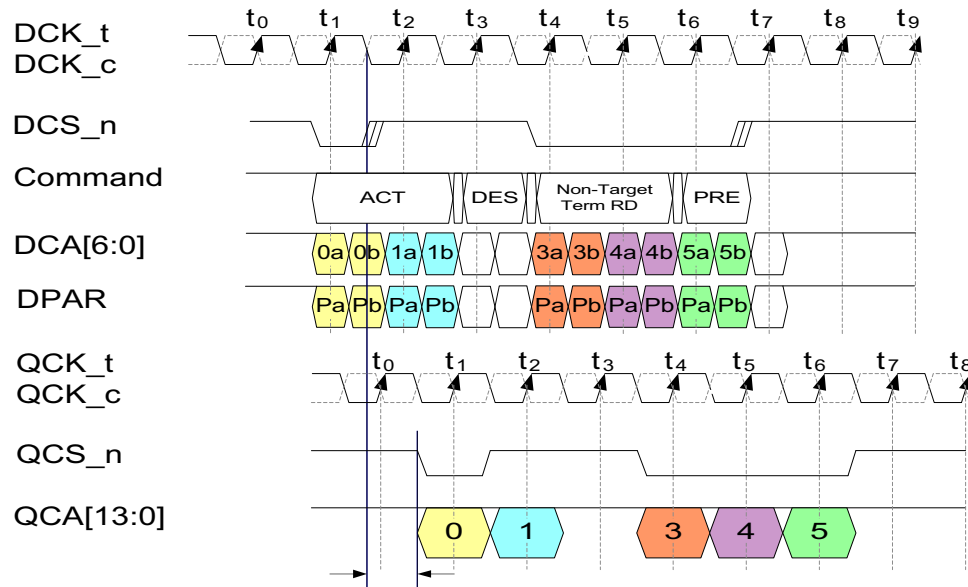
Figure 7 — One UI DRAM Command Timing Diagram



NOTE Timing Diagram for 0 nCK command latency adder.

Figure 8 — Two UI DRAM Command Timing Diagram

3.4.1 Double Data Rate DCA (cont'd)



NOTE Timing Diagram for 0 nCK command latency adder.

Figure 9 — DDR CA Multi-Command Timing Diagram Example

The DCS_n signal is SDR and is sampled by the RCD on the rising edge of DCK. See Section 13.11 on page 227 for details on DCS input receiver electrical and timing parameters. The DDR5RCD must maintain output timings to the DRAM and comply with the output tolerance skew parameter t_{QSK} as shown in Figure 10.

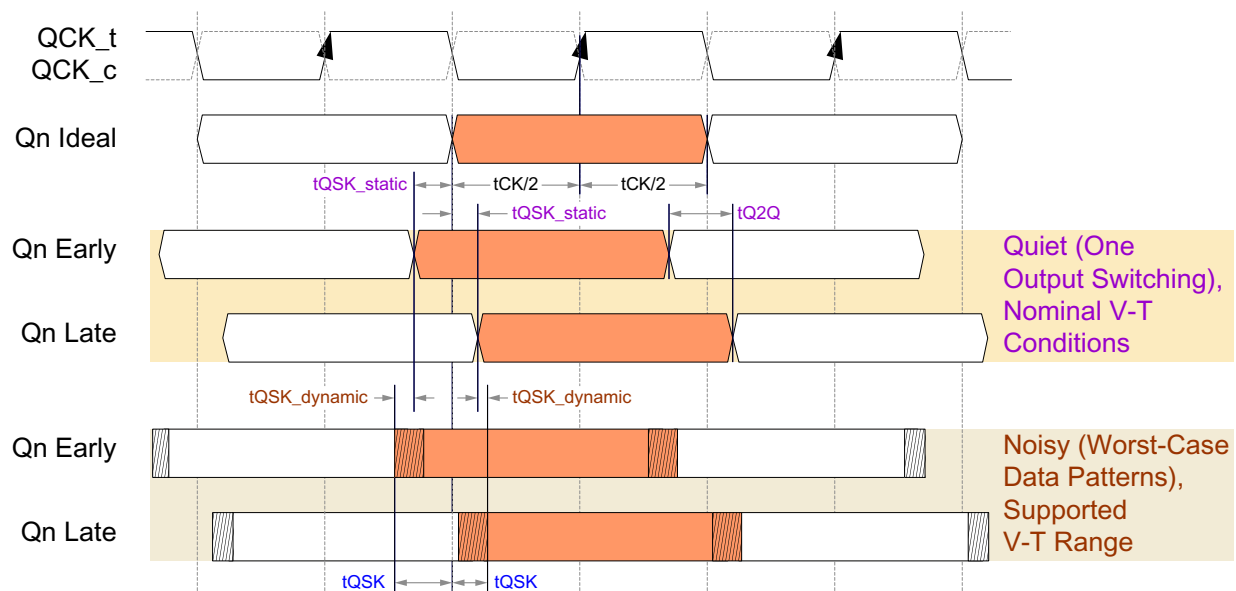


Figure 10 — Qn Output Skew

NOTE For Figure 10 outputs as specified in Table 200, “Output Timing Requirements1” Footnote 7.

3.4.2 Single Data Rate DCA

The DDR5RCD02 will support SDR (Single Data Rate) on the host-interface DCA signals. In this case, the RCD will apply 2N timing to the DRAM interface signals. This allows more setup or more hold time on the QCA bus. This mode is enabled when [RW00\[0\]](#) = 0. DDR5 has defined two-cycle commands that require the RCD to capture the commands differently between DDR and SDR modes. In both modes, the first half of the command is sampled on the rising edge of clock when the chip select is active. In SDR mode, the second half of the command is sampled on the next rising clock edge. Non-target ODT signaling (through chip select inputs) is also delayed by a clock in SDR mode. For applications that require SDR on the Host interface but do not need extra setup time on the DRAM interface, QCS pulses can be pulled earlier by one clock cycle by setting [RW00\[1\]](#) = 1.

The QCA will follow the DRAM specification for 2N mode.

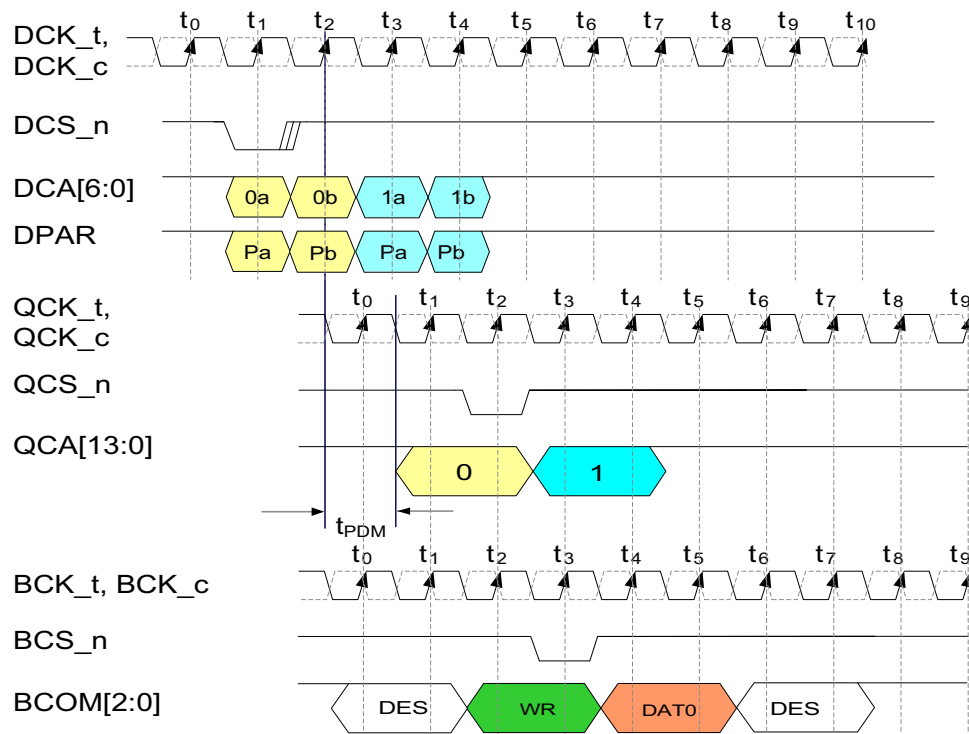


Figure 11 — SDR1 Mode Example of DRAM WR Command with [RW00\[1\]](#) = 0

3.4.2 Single Data Rate DCA (cont'd)

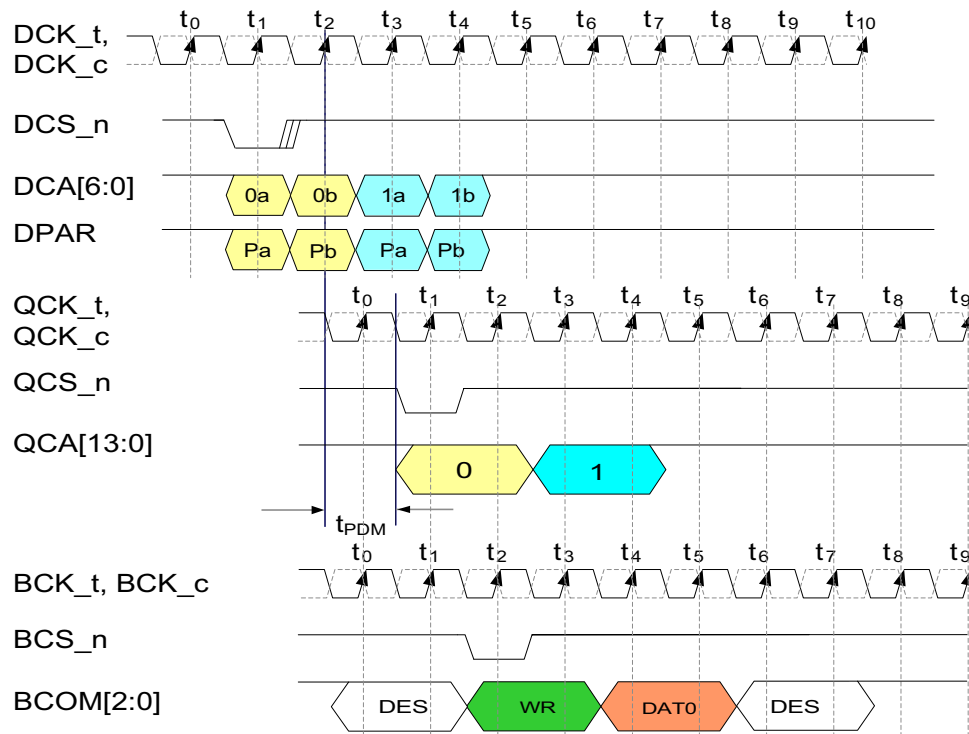


Figure 12 — SDR2 Mode Example of DRAM WR Command with $RW00[1] = 1$

3.4.3 SDR to DDR Transition

This mode will be set through SMBus during initialization between t_{STAB01} and t_{STAB02} , or after t_{STAB01} following Exit from Self Refresh Mode with Clock Stop (see Section 4.2.2 on page 47). There is no transition during normal operation. Transitions for SDR to DDR or SDR1 to SDR2 occur prior to Host Interface Training.

3.5 Parity

The Parity function in DDR5 differs from DDR4 in several ways

- The parity signal is received on the same cycle as the command/address bits rather than one cycle later.
- 2UI DRAM commands require a different protocol to block commands when the parity error is on the 2nd UI.
- No parity signal is sent on to the DRAMs.

The convention of parity is even parity across the $DCA_N[6:0]$ and $DPAR_N$ signals. The Parity is checked separately per UI on the DCA bus.

Parity is checked separately on the two sub channels. A parity error on one sub channel does not affect the operation of the other sub channel.

When DDR Command Address Rate is selected, $RW00[0] = 1$, ALERT_n will be asserted three or four input clocks after rising edge of first UI of DCA in which the erroneous command is registered.

3.5 Parity (cont'd)

In SDR mode, $RW00[0] = 0$, $ALERT_n$ will be asserted three or four input clocks after the rising edge corresponding to the second half of the erroneous command. This is the case regardless of the error being in the first, second, or both halves.

If parity checking is disabled, the register forwards sampled commands to the outputs unconditionally, the command appears on the outputs regardless of whether a parity error occurred or not.

For single and 2 UI DRAM commands, if parity checking is enabled and there is no parity error, the register will forward the sampled commands to the outputs.

3.5.1 Single UI DRAM Commands with Parity Enabled

For single UI DRAM commands, if parity checking is enabled and a parity error is detected on either UI of the DCA bus, the register will forward the command on QCA bus but will not assert any chip select to output.

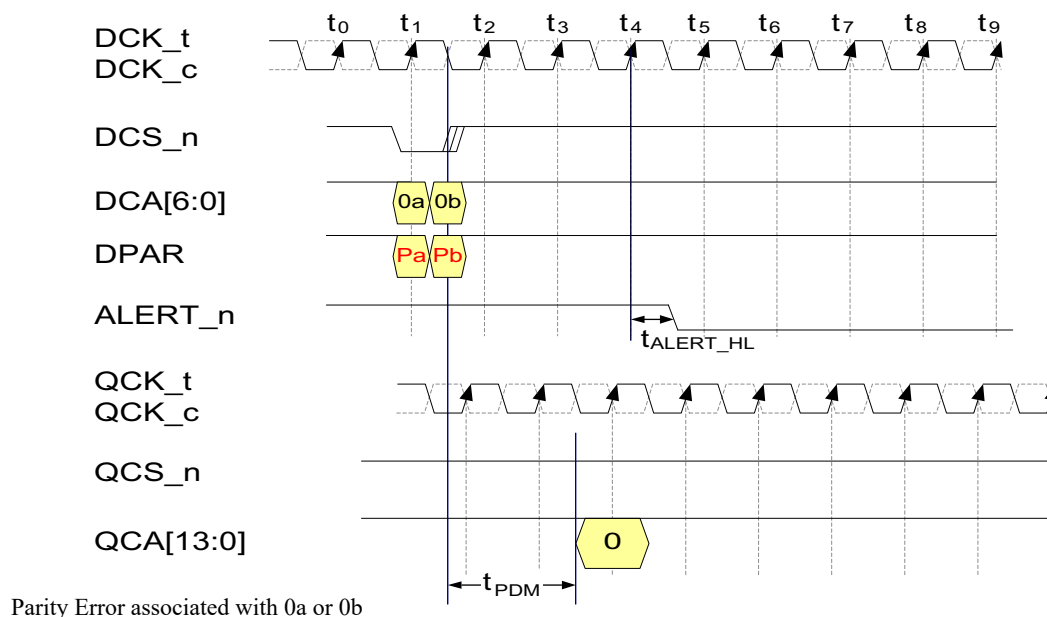


Figure 13 — 1 UI DRAM Command with Parity Checking Enabled and $CLA = 0$

3.5.1 Single UI DRAM Commands with Parity Enabled (cont'd)

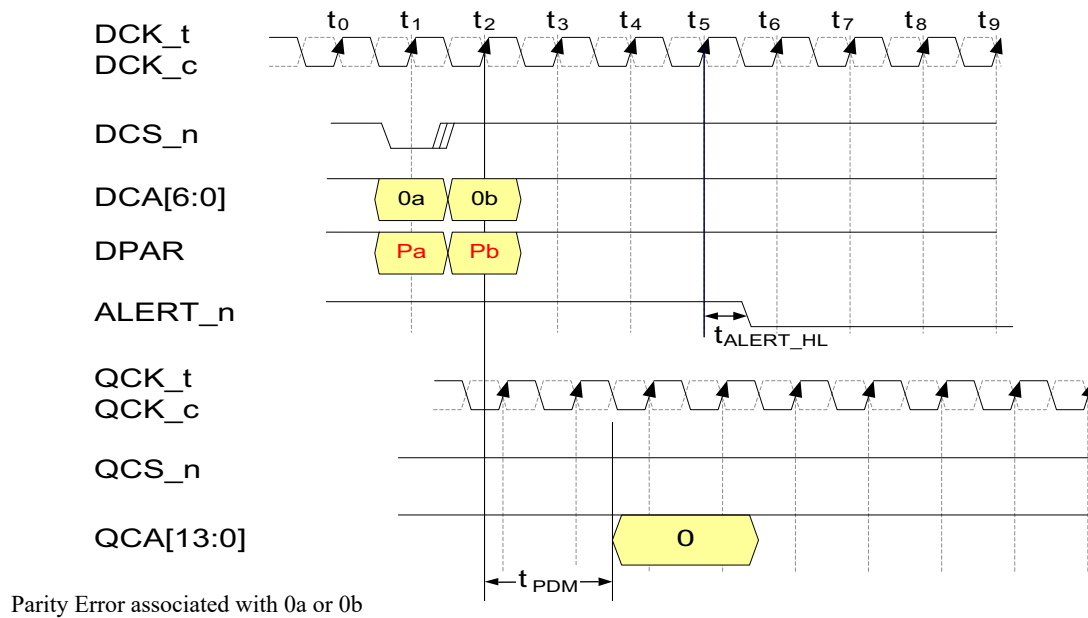
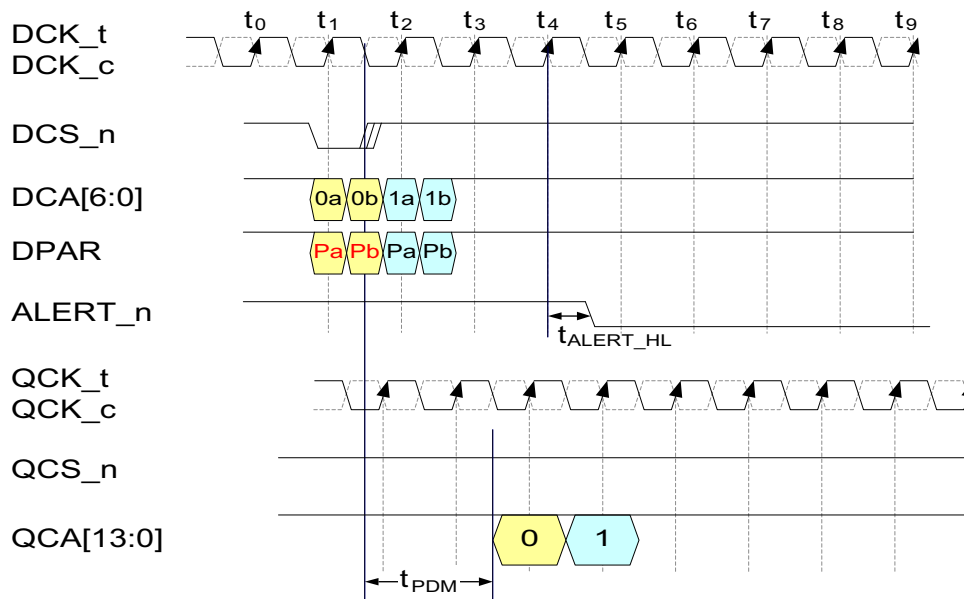


Figure 14 — SDR Mode 1 UI DRAM Command with Parity Checking Enabled and CLA = 0

3.5.2 2UI DRAM Commands with Parity Enabled

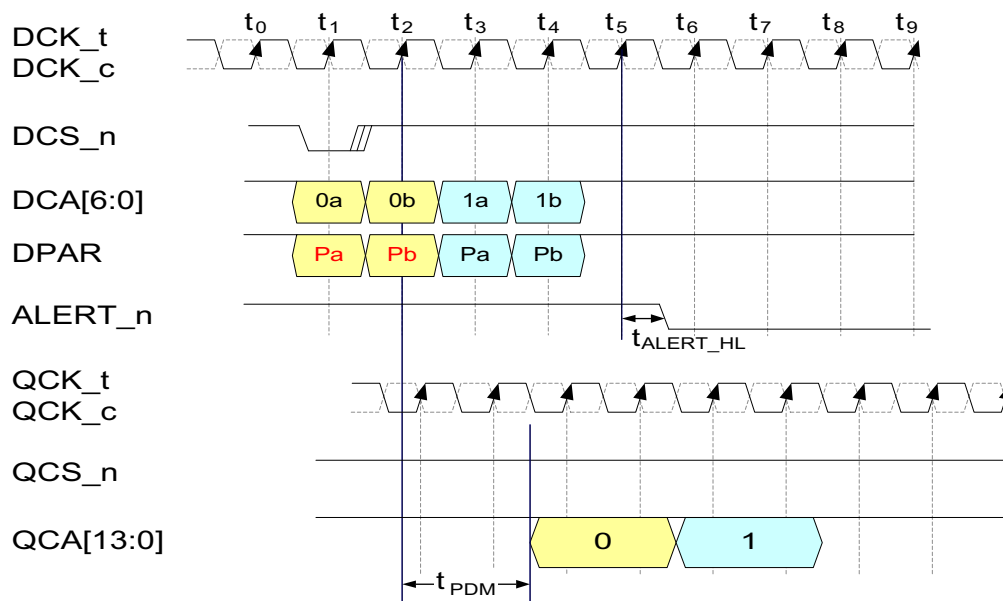
For 2UI DRAM commands, if parity checking is enabled and a parity error is detected on either UI of the DCA bus for the 1st UI of the DRAM command the register will forward the command on the QCA but will not assert any chip select output as shown in Figure 15.

3.5.2 2UI DRAM Commands with Parity Enabled (cont'd)



Parity Error associated with 0a or 0b

Figure 15 — Error in 1st UI of 2 UI DRAM Command with Parity Checking Enabled



Parity Error associated with 0a or 0b

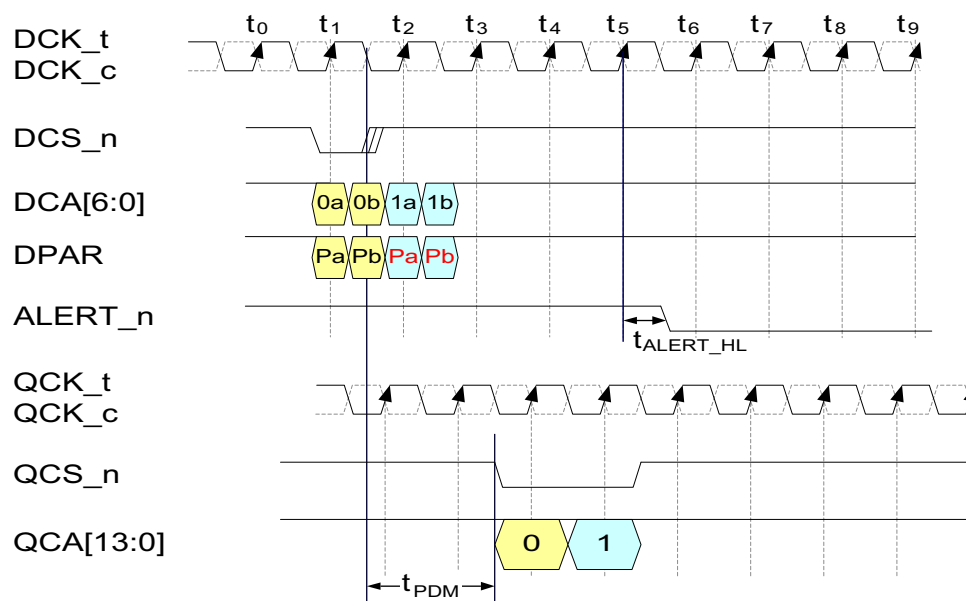
Figure 16 — SDR Mode Error in 1st UI of 2 UI DRAM Command with Parity Checking Enabled

3.5.2 2UI DRAM Commands with Parity Enabled (cont'd)

For 2UI DRAM commands, if the parity error occurs in either UI of the DCA bus for the 2nd UI of the DRAM command and the 1st had correct parity, the command will have already been sent to the DRAMs. In this case, the command itself will be known to be correct, but the additional address information contained in the 2nd UI will be incorrect. In order to prevent the command from being executed by the DRAM, the RCD will assert the chip select in the 2nd UI also for all ranks which received a chip select in the 1st UI as shown in Figure 17.

For RD, WR, and MRR commands, this will convert the command to a non-target termination encoding. All ranks receiving the chip select will terminate for this command, but no rank will execute the command.

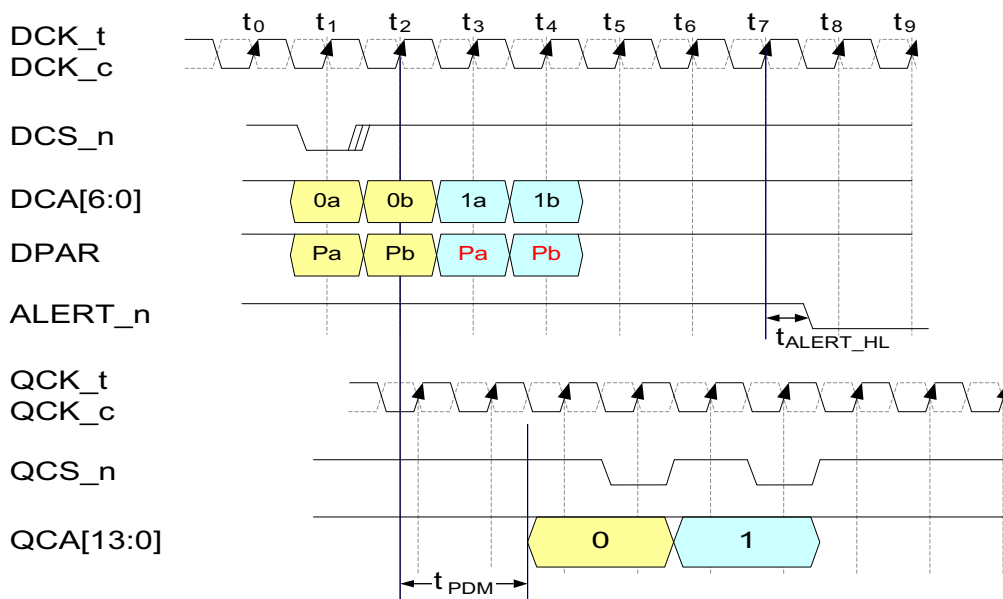
The only other 2 UI DRAM commands are the Activate, MRW, and Write Pattern commands. A DRAM seeing the chip select active for both UI of an Activate or Write Pattern command will ignore the command. Note that an MRW command will not use the data bus. The DRAM will not execute the MRW command if the chip select is asserted in both UI.



Parity Error associated with 1a or 1b

Figure 17 — Error in 2nd UI of 2 UI DRAM Command with Parity Checking Enabled

3.5.2 2UI DRAM Commands with Parity Enabled (cont'd)



Parity Error associated with 1a or 1b

Figure 18 — SDR1 Mode Error in 2nd UI of 2 UI DRAM Command with Parity Checking Enabled

If a parity error occurs on the 1st UI of a DRAM command, regardless of the command length, the command encoding itself may be corrupt. The register will be required to block all future commands until command forwarding is re-enabled. When commands are re-enabled, the register must not enable commands until it sees a UI with all CS inactive in order to avoid re-enabling in the middle of a command.

Table 9 — Blocking Commands on Parity Error

Parity error on 1st DRAM UI	Parity error on 2nd DRAM UI	Outputs
No	No	Command is forwarded to DRAM
No	Yes	First UI of command forward to DRAM. 2 nd UI of command forward to DRAM, but with QCS asserted on ALL ranks which received a DCS on the 1st UI. Future commands not sent until parity checking is re-enabled.
Yes	Yes or No	First UI and Second UI of the command forward to DRAM but QCS is not asserted. Future commands not sent until parity checking is re-enabled.

3.5.3 ALERT_n Assertion

The behavior of ALERT_n with parity checking disabled is the same as when parity checking is enabled with the exception that ALERT_n is never asserted as result of a CA parity error. However, when parity checking is disabled, ALERT_n can still be asserted as a result of an assertion of the DERROR_IN_n input.

After the RCD receives DPAR_N from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[1:0]_n signals being Active, or the 2nd UI of a 2UI DRAM Command.

3.5.3 ALERT_n Assertion (cont'd)

The convention of parity is even parity across the DCA and DPAR signals. Parity is checked independently for the two channels.

If a parity error occurs and parity checking is enabled in [RW01](#), the RCD sets the 'CA Parity Error Status' bit in [RW24](#) to '1' and disables parity checking. ALERT_n is asserted three or four input clocks after the erroneous command is registered.

If the 'CA Parity Error Status' bit is '0', the RCD logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word [RW01](#) is '0'. In this case the erroneous command and all subsequent commands are not forwarded (i.e., QxCsy_N_n are not asserted) to the DRAM until the memory controller issues a 'Clear CA Parity Error' command, which will also clear the 'CA Parity Error Status' bit in the Error Log Register.

If the 'ALERT_n Assertion' bit is '1', the ALERT_n pulse width is as defined in Table 102 on page 136 with start of the ALERT_n pulse width counted from the third or fourth input clock edge after the 1st parity error. The erroneous command and all subsequent commands are not forwarded (i.e. QxCsy_N_n are not asserted) to the DRAM until the end of the ALERT_n pulse width. After the ALERT_n pulse, the device will automatically resume forwarding commands to the DRAM.

- If the 'ALERT_n Re-enable' bit is '0', parity checking remains disabled until a 'Clear CA Parity Error' command is sent, which will also clear the 'CA Parity Error Status' bit in the Error Log Register.
- If the 'ALERT_n Re-enable' bit is '1', the device will re-enable parity checking after the ALERT_n pulse. The 'CA Parity Error Status' bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit. The other bits in the Error Log Register are not updated on this subsequent error. Both the 'CA Parity Error Status' bit as well as the '> 1 Error' bit will be cleared by sending a 'Clear CA Parity Error' command.

3.6 DCA Decision Feedback Equalization

Since the DCA will be Double Data Rate, the RCD will support a 4 Tap DFE on the DCA host-interface receivers. The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, 4 CA slicers (also called Taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each Tap. The gain control of the front end is used to ensure that the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps C1, C2, C3, C4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits. The host can enable 1, 2, 3, or 4 taps in a consecutive order always starting with Tap 1 as shown in Table 10, "DFE Tap Configurations". DFE input gain adjustment and DFE Tap Coefficients 1 through 4 are set by control words located in PG[1:0]. These DFE control words allow programming of each parameter on a DCA I/O-specific basis, and they are intended to be trained by the host. The DDR5RCD02 device does not support adaptive DFE, and it only supports DFE when its DCA host interface is configured in DDR mode (i.e., [RW00\[0\]](#) = 1).

3.6.1 DFE Tap Configurations

Table 10 — DFE Tap Configurations

RW31 OP4	RW31 OP5	RW31 OP6	RW31 OP7	Tap 1	Tap 2	Tap 3	Tap 4
0	x	x	x	Disabled	Disabled ¹	Disabled ¹	Disabled ¹
1	0	x	x	Enabled	Disabled	Disabled ²	Disabled ²
1	1	0	x	Enabled	Enabled	Disabled	Disabled ³
1	1	1	0	Enabled	Enabled	Enabled	Disabled
1	1	1	1	Enabled	Enabled	Enabled	Enabled

NOTE 1 DDR5RCD02 hardware disabled when RW31[4] = 0 and RW31[7:5] are don't care and ignored by the RCD.

NOTE 2 DDR5RCD02 hardware disabled when RW31[5] = 0 and RW31[7:6] are don't care and ignored by the RCD.

NOTE 3 DDR5RCD02 Hardware disabled when RW31[6] = 0, and RW31[7] is a don't care and ignored by the RCD.

3.6.2 DFE Gain and Tap Range

Table 11 — DFE Gain and Tap Total Control Word Range

DFE Parameter	Min	Max	Unit
Gain	-6	6	dB
Tap 1	- 150	150	mV
Tap 2	- 60	60	mV
Tap 3	- 45	45	mV
Tap 4	- 45	45	mV

Table 12 — DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin

DFE Parameter	DDR5-3200 - 5600			Unit
	Min	Typ	Max	
DFE Gain Bias Step Size ^{1,2}	1.7	2	2.3	dB
DFE Gain Bias Tolerance (INL) ^{1,2}	- 0.5	-	0.5	dB
DFE Gain Bias Step Size Tolerance (DNL) ^{1,2}	- 0.3	-	0.3	dB
DFE Gain Bias Step Time ¹	-	-	300	ns
DFE Tap Bias Step Size ^{1,2}	1	3	5	mV
DFE Tap Bias Tolerance (INL) (-150 mV to 0 mV) ^{1,2}	Min (V _{ideal} x 115%, V _{ideal} - 3 * LSB) ^{3,4}	-	Max (V _{ideal} x 85%, V _{ideal} + 3 * LSB) ^{3,4}	mV
DFE Tap Bias Tolerance (INL) (0 mV to 45 mV) ^{1,2}	V _{ideal} - 3 * LSB ^{3,4}	-	V _{ideal} + 3 * LSB ^{3,4}	mV
DFE Tap Bias Step Size Tolerance (DNL) ²	- 66.67	-	66.67	% of Step Size
DFE Tap Bias Step Time	-	-	64	tCK

NOTE 1 Host Vref fixed at 0.75 x V_{DD}, typical Voltage-Temperature condition (i.e., V_{DD} = 1.1 V, 25 °C), and default gain setting.

NOTE 2 These parameters are neither subject to silicon validation nor production testing.

NOTE 3 V_{ideal} refers to the ideal DFE Tap value based on the setting.

NOTE 4 LSB = 3 mV.

3.6.3 DCA DFE Tap Measurement

When DFE taps are enabled, they add offset to the DFE summer, which affects the input to the slicer. The feedback to the taps may be positive or negative, based on the sign of the coefficient and the level of the input, resulting in four cases, all of which must be tested. Each tap is measured individually with other tap coefficients set to 0. Other combinations can be extrapolated from the results.

3.6.3.1 HIGH-to-LOW Transition Test Method

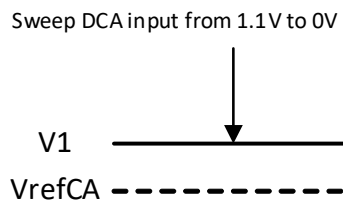
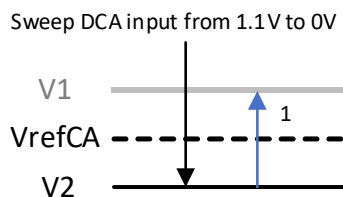
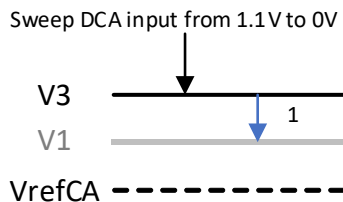


Figure 19 — HIGH-to-LOW Sweep: No DFE Applied



Note 1: Positive feedback results in an increase in voltage as seen by the slicer

Figure 20 — HIGH-to-LOW Sweep: DFE Positive Bias Applied



Note 1: Negative feedback results in an decrease in voltage as seen by the slicer

Figure 21 — HIGH-to-LOW Sweep: DFE Negative Bias Applied

1. Make sure VrefCA (RW[47:40]) is set to the default, DFE_Vref (PG[2]RW[62, 66, 6A, 6E, 72, 76, 7A, 7E]) is set to 0, power supply is 1.1V, and DFE is disabled.
2. Sweep the input signal from 1.1V to 0V to find the lowest level that produces a stable HIGH output and record this input level as V1. No overshoot is allowed on the input. See [Figure 19](#).
3. Enable DFE (RW31[0]). Enable the tap under test and all previous taps in RW31[7:4]. Set the coefficients for the previous taps to 0. All configuration in this procedure is via Sideband Bus access.
4. Configure the sign bit to 0 and the coefficient to n steps for the tap under test, where n is a loop variable.
5. Sweep the input signal from 1.1V to 0V to find the lowest level that produces a stable HIGH output and record this input level as V2. No overshoot is allowed on the input. See [Figure 20](#).

3.6.3.1 HIGH-to-LOW Transition Test Method (cont'd)

6. The DFE Tap Bias $V(+)$ = $(V1 - V2)$ for positive feedback. Validate $V(+)$ is within spec.
7. Configure the sign bit to 1 and the coefficient to n steps for the tap under test, where n is a loop variable.
8. Sweep the input signal from 1.1V to 0V to find the lowest level that produces a stable HIGH output and record this input level as V3. No overshoot is allowed on the input. See Figure 21.
9. The DFE Tap Bias $V(-)$ = $(V1 - V3)$ for negative feedback. Validate $V(-)$ is within spec.
10. Repeat steps 4-9 until all the Tap steps for Taps 1-4 are measured.

3.6.3.2 LOW-to-HIGH Test Transition Method

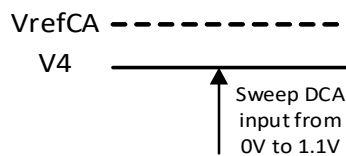
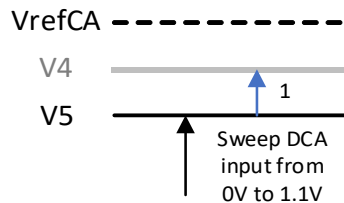
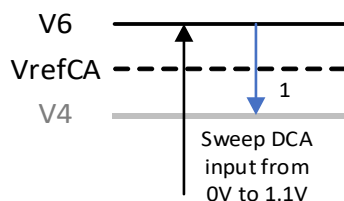


Figure 22 — LOW-to-HIGH Sweep: No DFE Applied



Note1: Positive feedback results in an increase in voltage as seen by the slicer

Figure 23 — LOW-to-HIGH Sweep: DFE Positive Bias Applied



Note 1: Negative feedback results in an decrease in voltage as seen by the slicer

Figure 24 — LOW-to-HIGH Sweep: DFE Negative Bias Applied

1. Make sure VrefCA (RW[47:40]) is set to the default, DFE_Vref (PG[2]RW[62, 66, 6A, 6E, 72, 76, 7A, 7E]) is set to 0, power supply is 1.1V, and DFE is disabled.
2. Sweep the input signal from 0V to 1.1V to find the highest level that produces a stable LOW output and record this input level as V4. No overshoot is allowed on the input. See Figure 22.
3. Enable DFE (RW31[0]). Enable the tap under test and all previous taps in RW31[7:4]. Set the coefficients for the previous taps to 0. All configuration in this procedure is via Sideband Bus access.
4. Configure the sign bit to 1 and the coefficient to n steps for the tap under test, where n is a loop variable.

3.6.3.2 LOW-to-HIGH Test Transition Method (cont'd)

5. Sweep the input signal from 0V to 1.1V to find the highest level that produces a stable LOW output and record this input level as V5. No overshoot is allowed on the input. See [Figure 23](#).
6. The DFE Tap Bias $V(+) = (V4 - V5)$ for positive feedback. Validate $V(+)$ is within spec.
7. Configure the sign bit to 0 and the coefficient to n steps for the tap under test, where n is a loop variable.
8. Sweep the input signal from 0V to 1.1V to find the highest level that produces a stable LOW output and record this input level as V6. No overshoot is allowed on the input. See [Figure 24](#).
9. The DFE Tap Bias $V(-) = (V4 - V6)$ for negative feedback. Validate $V(-)$ is within spec.
10. Repeat steps 4-9 until all the Tap steps for Taps 1-4 are measured.

3.7 Continuous Time Linear Equalization (CTLE)

3.7.1 Background

Continuous time linear equalization can be an effective method to improve signal margins at input receivers of the DDR5RCD02 device.

3.7.2 CTLE Transfer Function

The equation below represents the CTLE transfer function implemented in the DDR5RCD02 device.

$$\frac{A_{dc} \left(1 + \frac{s}{Z} \right)}{\left(1 + \frac{s}{P_1} \right) \left(1 + \frac{s}{P_2} \right)}$$

Where

- A_{dc} is the gain of the CTLE at DC,
- Z is the location of the zero,
- P_1 is the location of the first pole, and
- P_2 is the location of the second pole.

The DDR5RCD02 receivers support 16 possible combinations of CTLE parameter values as shown in Table 13 below. The device revision can only support one of the CTLE Configuration Ranges, A, B, C, or D. The host can read out the supported range from the CTLE Configuration Control Word, [RW50\[7:5\]](#). Each combination can be selected through 4-bit control word settings [RW52\[3:0\]](#) (CTLE Parameter Set A) and [RW53\[3:0\]](#) (CTLE Parameter Set B). There is a CTLE global feature enable control bit in [RW50\[0\]](#), and enable/disable controls per-pin in [RW51\[7:0\]](#). An 8-bit control word, [RW54\[7:0\]](#), provides per-pin control to determine whether a receiver uses CTLE Parameter Set A controlled by [RW52\[3:0\]](#), or Parameter Set B controlled by [RW53\[3:0\]](#).

3.7.2 CTLE Transfer Function (cont'd)

Table 13 — Supported CTLE Parameter Value Combinations

Range	CW Bits OP[3:0] in RW52 or RW53	Gain (A_{dc}) ¹	Zero (Z)	Pole 1 (P_1)	Pole 2 (P_2)
A	0000 _B	TBD	TBD	TBD	TBD
	0001 _B	TBD	TBD	TBD	TBD
	0010 _B	TBD	TBD	TBD	TBD
	0011 _B	TBD	TBD	TBD	TBD
	0100 _B	TBD	TBD	TBD	TBD
	0101 _B	TBD	TBD	TBD	TBD
	0110 _B	TBD	TBD	TBD	TBD
	0111 _B	TBD	TBD	TBD	TBD
	1000 _B	TBD	TBD	TBD	TBD
	1001 _B	TBD	TBD	TBD	TBD
	1010 _B	TBD	TBD	TBD	TBD
	1011 _B	TBD	TBD	TBD	TBD
	1100 _B	TBD	TBD	TBD	TBD
	1101 _B	TBD	TBD	TBD	TBD
	1110 _B	TBD	TBD	TBD	TBD
	1111 _B	TBD	TBD	TBD	TBD
B	0000 _B	TBD	TBD	TBD	TBD
	0001 _B	TBD	TBD	TBD	TBD
	0010 _B	TBD	TBD	TBD	TBD
	0011 _B	TBD	TBD	TBD	TBD
	0100 _B	TBD	TBD	TBD	TBD
	0101 _B	TBD	TBD	TBD	TBD
	0110 _B	TBD	TBD	TBD	TBD
	0111 _B	TBD	TBD	TBD	TBD
	1000 _B	TBD	TBD	TBD	TBD
	1001 _B	TBD	TBD	TBD	TBD
	1010 _B	TBD	TBD	TBD	TBD
	1011 _B	TBD	TBD	TBD	TBD
	1100 _B	TBD	TBD	TBD	TBD
	1101 _B	TBD	TBD	TBD	TBD
	1110 _B	TBD	TBD	TBD	TBD
	1111 _B	TBD	TBD	TBD	TBD