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DDR5 Data Buffer Definition (DDR5DB01) - Rev 1.1

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DDR5 DATA BUFFER DEFINITION (DDR5DB01)

(From JEDEC Board Ballot JCB-21-41, formulated under the cognizance of the JC-40.4 Subcommittee on Registered and Fully Buffered Memory Support Logic.)

1 Scope

This standard defines standard specifications for features and functionality, DC & AC interface parameters and test loading for definition of the DDR5 data buffer for driving DQ and DQS nets on DDR5 LRDIMM applications.

The purpose is to provide a standard for the DDR5DB01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR5DB01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

This document uses DDR5DB01, Data Buffer, DB or Buffer interchangeably throughout for the DDR5DB01 device naming.

2 Mechanical Outline

The DDR5DB01 Package is a 55 - ball Fine-Pitch BGA (FBGA) with 0.5mm ball pitch, 15 x 5 grid with 20 balls depopulated, 7.8 mm x 2.73 mm as defined in MO-276 Issue N, Variation 1007.80x2.73-5030-55Y¹. The device pinout options support the register link inputs in the center columns to support signal routing matching from alternate sides of the DIMM to the DDR5RCD01. Corresponding host side data/strobe balls are placed in a way to match the corresponding pin location on the connector if the device is mounted on the backside of an LRDIMM module. Each VDD and VSS is located close to an associated no ball position to allow low-cost via technology combined with the small 0.50 mm ball pitch.

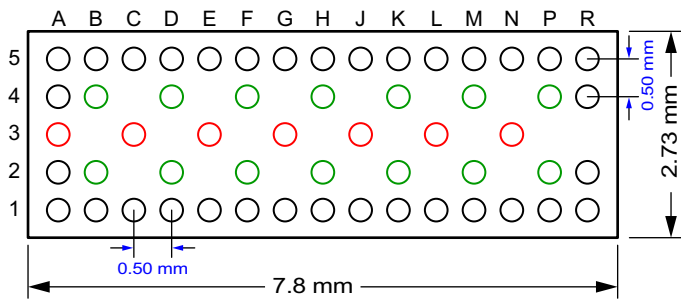


Figure 1 — 55 Ball Configuration 15 x 5 (TOP VIEW)

Ball pitch: 0.50 mm x 0.50 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm). X-ray view from topside.

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5DB01 must comply with a minimum thickness of 0.80 mm.

2.1 Pinout 15 x 5

Table 1 specifies the pinout for the DDR5DB01. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

Table 1 — Ball Assignment -55 ball FBGA, 15 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
5	MDQ7	MDQ5	MDQ6	MDQ4	MDQS1_t	MDQS1_c	BCOM0	BCOM1	BCOM2	MDQS0_c	MDQS0_t	MDQ3	MDQ1	MDQ2	MDQ0
4	BRST_n	VSS		VSS		VSS		VSS		VSS		VSS		VSS	LB TXDQ
3	VDD		VDD		VDD		VDD		VDD		VDD		VDD		
2	ZQCAL	VSS		VSS		VSS		VSS		VSS		VSS		VSS	LB TXDQS
1	DQ7	DQ5	DQ6	DQ4	DQS1_t	DQS1_c	BCK_c	BCK_t	BCS_n	DQS0_c	DQS0_t	DQ3	DQ1	DQ2	DQ0

2.2 Terminal Functions for 55-Ball Data Buffer Package Configuration

Table 2 — Terminal Functions for 55-Ball Package Configuration

Signal Group	Signal Name	Type	Description
Data buffer control inputs	BCS_n	POD V_{REF} based ¹	Chip Select Input
	BRST_n	CMOS	Level Triggered Reset, when BCOM is '000' or '111' resets device to default values, otherwise used for BCOM Strap mode defined in "BCOM Training Mode (BCOMTM) - Data Buffer Interface" on page 51.
	BCOM[2:0]	POD V_{REF} based ¹	Register communication bus for data buffer programming and control access
Clock inputs	BCK_t, BCK_c	POD differential	Differential clock input pair
Host Interface	DQ[3:0] DQ[7:4]	POD V_{REF} based bidirectional	Host side data lower nibble Host side data upper nibble
	DQS0_t DQS0_c DQS1_t DQS1_c	POD differential bidirectional	Host side data strobe for lower nibble Host side data strobe complement for lower nibble Host side data strobe for upper nibble Host side data strobe complement for upper nibble
DRAM Interface	MDQ[3:0] MDQ[7:4]	POD V_{REF} based bidirectional	DRAM side data lower nibble DRAM side data upper nibble
	MDQS0_t MDQS0_c MDQS1_t MDQS1_c	POD differential bidirectional	DRAM side data strobe for lower nibble DRAM side data strobe complement for lower nibble DRAM side data strobe for upper nibble DRAM side data strobe complement for upper nibble
Loopback	LBTXDQ LBTXDQS	POD	Loopback DQ Transmit Loopback DQS Transmit

Table 2 — Terminal Functions for 55-Ball Package Configuration

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V _{DD}	Power Input	Power supply voltage
	V _{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration

1. These receivers use the internal BVref as the switching point reference

3 Device Description and Features

3.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.1 V, V_{DD} operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR5 Register.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are V_{DD} terminated drivers optimized to drive single or dual terminated traces in DDR5 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR5DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCS_n and BCOM[2:0]. The BCOM[2:0] inputs are used to write device internal control registers. The buffer control word (RW) mechanism is described in more detail in Section 9 BCK_t, BCK_c, BCS_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 LRDIMM.

The DDR5DB01 also supports dedicated pins for ZQ calibration.

3.2 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of t_{RINIT1} in the Power-on RESET state. During this time, a static value of BCOM[2] = BCOM[1] = BCOM[0] = HIGH or LOW shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1}, t_{Strap_Hold} also applies (see Table 155 on page 163). In the Power-on RESET state all Strobe and Data input receivers are disabled and can be left floating. In the Power-on RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All Strobe and Data outputs must float. In the Power-on RESET state the data buffer is in low-power state and host interface and DRAM interface ODT terminations are disabled.

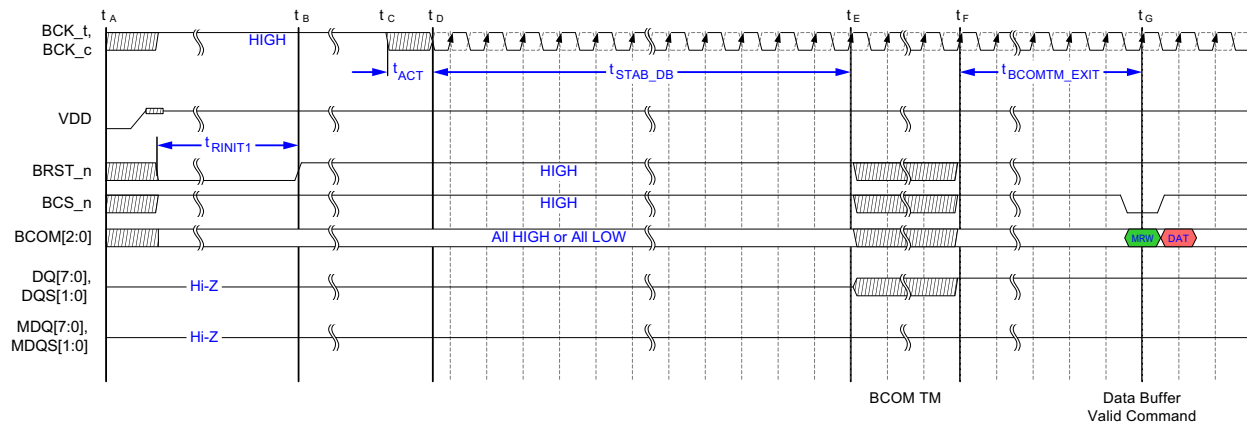


Figure 2 — Data Buffer Initialization Sequence

3.2.1 Clock Stabilization Time t_{STAB_DB}

During PLL stabilization time t_{STAB_DB} the data buffer is not fully operational. To ensure correct operation, some rules apply to the inputs of the buffer:

- BCS_n must remain HIGH.

These rules apply to any instance where stabilization time t_{STAB_DB} is required:

- Exit from Reset state
- Exit from clock stop power down
- Changing clocking related registers

Since the data buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the stabilization time (t_{STAB_DBDATA}) the DB must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs.

BCOM VREF and Command Timing settings are set through a Static mode defined in the BCOM Training section.

3.2.2 Reset Initialization with Stable Power

The timing diagram in Figure 3 depicts the initialization sequence with stable power and clock. For this sequence, the BCK continues toggling with stable phase and frequency. The data buffer remains in the RESET state for a minimum of t_{RINIT1} . During this time, a static value of $BCOM[2] = BCOM[1] = BCOM[0] = \text{HIGH or LOW}$ shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1} , t_{Strap_Setup} and t_{Strap_Hold} also apply (see Table 155 on page 163). In the RESET state, all non-sticky control registers are restored to their default states.

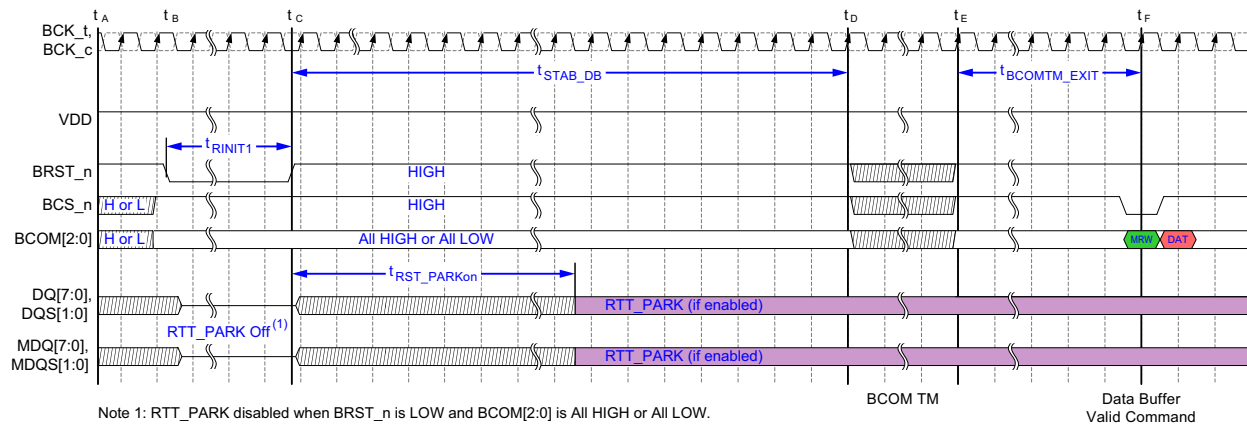


Figure 3 — Data Buffer Reset with Stable Power and Clock

Figure 4 depicts the initialization sequence with stable power and stopped clock. For this sequence, the BCK clock is allowed to stop (i.e., BCK_t = BCK_c = HIGH). The data buffer remains in the RESET state for a minimum of t_{RINIT1} . During this time, a static value of BCOM[2] = BCOM[1] = BCOM[0] = HIGH or LOW shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1} , t_{Strap_Hold} also applies (see Table 155 on page 163). In the RESET state, all non-sticky control registers are restored to their default states.

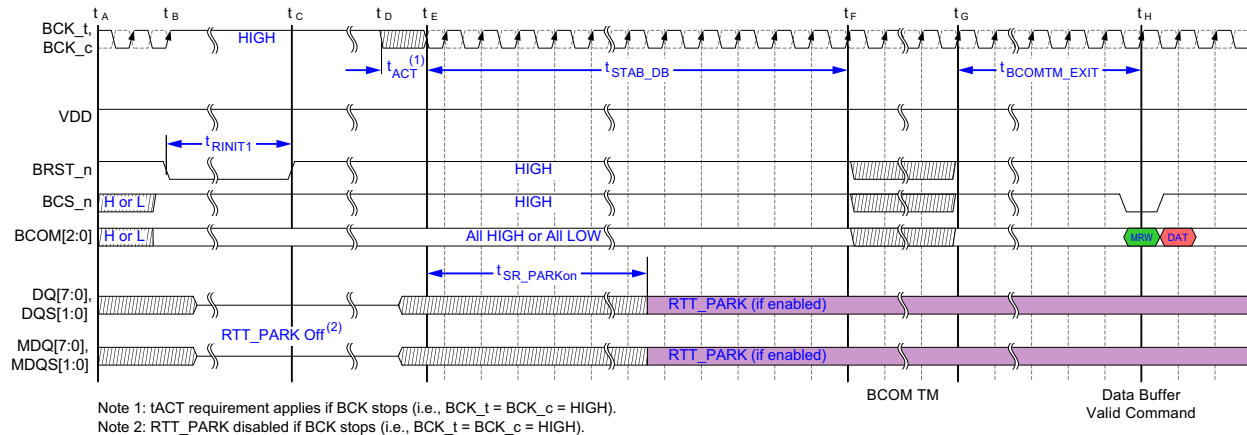


Figure 4 — Data Buffer Reset with Stable Power and Stopped Clock

3.3 Transparent Mode

Transparent mode is enabled in the DDR5DB01 by setting RW82[0] to 1. While in transparent mode, the DB does not interpret BCS_n and BCOM commands as defined in Table 12, “Data Buffer Control Bus Command Truth Table”. For BCS_n input value of “1” and BCOM[2:0] input values of “111” it directs the data flow from host interface to DRAM interface, and it enables or disables the on-die termination at the host interface based on the setting in RW82[1]. For BCS_n input value of “1” and BCOM[2:0] input values of “000”, the Data Buffer directs the data flow from DRAM interface to host interface and it enables or disables the on-die termination at the DRAM interface based on the setting in RW82[1]. Any other input values of BCS_n and BCOM[2:0] are invalid.

The Data Buffer does not support high-speed changes in direction of data flow. The host will wait for 32 clock cycles of settling time after the direction in data flow is reversed in transparent mode.

In transparent mode the Data Buffer statically enables the input receivers of the interface that is receiving signals and is permanently enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. Propagation delays for all the signals within each DQ/DQSMDQ/MDQS nibble must be matched closely enough to meet parameter D_{TPM_DQ} in Table 156. All the clock frequencies available in test mode and normal operation mode in the Data Buffer will be supported in transparent mode. DQSs are treated as differential. This means if a DQSx_t and the corresponding DQSx_c are both HIGH or both LOW, the associated MDQSx_t and MDQSx_c will be invalid. MDQSs are treated as differential as well.

In transparent mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT_PARK Buffer Control Word.

To exit transparent mode in the DDR5DB01 device, it is necessary to apply power cycle or Normal Operation RESET (as defined in Table 27, “BCOM Strap for Data Buffer Training States,” on page 52).

Table 3 — DB Termination Control in Transparent Mode

BCS_n, BCOM[2:0]	TPM Termination Control RW82[1]	Host Interface Termination	DRAM Interface Termination
= “1111”	0	ON	OFF
	1	OFF	OFF
= “1000”	0	OFF	ON
	1	OFF	OFF

3.4 DQ Pass-Through Mode

For initialization and training applications, DDR5DB01 supports DQ pass through mode.

DQ pass-through mode is enabled in the DDR5DB01 by setting [RW82\[2\]](#) to 1. While in the DQ pass-through mode, the DDR5DB01 only supports MRW BCOM commands and any commands other than MRW are not allowed.

When DQ pass-through mode is enabled, if the direction select control word bit [RW82\[3\]](#) is set to 0 (default value), then DQ pass-through mode is enabled in the Write direction from host interface DQ/DQS to DRAM interface MDQ/MDQS. The DDR5DB01 directs the data flow from host interface to DRAM interface, and it enables or disables the on-die termination at the host interface based on the setting in [RW82\[1\]](#).

When DQ pass-through mode is enabled, if the direction select control word bit [RW82\[3\]](#) is set to 1, then DQ pass-through mode is enabled in the read direction from DRAM interface MDQ/MDQS to host interface DQ/DQS. The DDR5DB01 directs the data flow from DRAM interface to host interface, and it enables or disables the on-die termination at the DRAM interface based on the setting in [RW82\[1\]](#).

In the DQ pass-through mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT_PARK Control Word. In the DQ pass-through mode, the Data Buffer statically enables the input receivers of the interface that is receiving signals and enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. Propagation delays for all the signals within each DQ/DQS-MDQ/MDQS nibble must be matched closely enough to meet parameter D_{TPM_DQ} in Table 156. All the clock frequencies available in test mode and normal operation mode will be supported. DQSs are treated as differential. This means if a DQSx_t and the corresponding DQSx_c are both HIGH or both LOW, the associated MDQSx_t and MDQSx_c will

be invalid. MDQSs are treated as differential as well.

Table 4 — DB Termination Control in DQ Pass-Through Mode¹

DQ pass through mode	Termination Control RW82[1]	Host Interface Termination	DRAM interface Termination
Enabled for write direction	0 (default)	ON	-
	1	OFF	-
Enabled for read direction	0 (default)	-	ON
	1	-	OFF

1. The DB termination control during DQ pass-through mode is irrelevant to the {BCS_n, BCOM} patterns.

After the DQ pass-through mode is enabled or disabled, the controller will wait for 32 clock cycles of data path settling time.

The DDR5DB01 exits the DQ pass-through mode when RW82[2] is set to 0.

3.5 Loopback Mode

With loopback circuit the DDR5DB01 can feed a received signal or data back out to an external receiver for debugging, testing, and/or training purposes. Loopback is necessary in order for the host memory controller or test instrument to immediately read back data that was written to the Data Buffer without having to issue multiple DRAM WRITE/READ commands. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis.

For example, at $BER=10^{-16}$:

1. There is not enough memory depth in the DRAM to store all the 10^{16} data.
2. The amount of time to perform multiple WRITE/READ commands to and from the array is prohibitively long.
3. Since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention.
4. Limited pattern depth means limited Intersymbol Interference (ISI). Loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional methods.

3.5.1 Loopback Output Definition

The Loopback circuitry requires two output pins (one single ended Loopback data, LBTXDQ, and one single ended Loopback strobe, LBTXDQS). The Loopback circuitry also consists of multiplexers to select the DQ and Phase for Loopback. Pin assignment location for Loopback pins are defined as R4 for LBTXDQ and R2 for LBTXDQS.

It is the Host's responsibility to put the device into a normal operating mode prior to sending BCOM commands.

The default RTT state for Loopback when RW8D[0] = 0 is RZQ/5 (48 Ω), designated by RW8E[2:0] = 101. In this state, both the LBTXDQS and LBTXDQ outputs are disabled. If the Loopback pins of several Data Buffer devices are connected together and some devices need disabled termination, there is RTT_OFF option available by setting RW8E[2:0] = 000.

Enabling the Loopback Output value via RW8D[0] = 1 will result in the LBTXDQS and LBTXDQ pins to transition from the RTT_Loopback state to a DB Drive State.

The LBTXDQS output will transition with the differential input crossing point of DQS_t/DQS_c, plus latency.

The LBTXDQ output will transition with the receiver data state of the DQ pin selected by [RW8D\[4:2\]](#).

Table 5 — Loopback Output Definition

Condition	LBTXDQS	LBTXDQ	NOTE
Loopback Disabled	RTT_Loopback	RTT_Loopback	
Loopback Enabled	Selected Phase	Selected Phase and Selected DQ	

3.5.2 Loopback Phase

Due to the high data rates of the DDR5 Data Buffer, Loopback is implemented with 2-way interleaved outputs. With a 2-way implementation, the DQS and selected DQ will be sampled and output every 1 CK or 2 UI. To be able to sample all bits with a 2-way interleave implementation, the Loopback Phase Select programmed in [RW8D\[5\]](#) allows selection of the DQS/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options.

Figure 5 shows an example of a Loopback implementation for 2-way interleave Data Buffer. This example requires a divided clock to produce DQS_0 (PHASE A) and DQS_180 (PHASE B). The output of the DQ slicer runs at 1/2 the speed as received data. In a 2-way interleave design, the data is received at full speed, but internally the data is latched only at half speed.

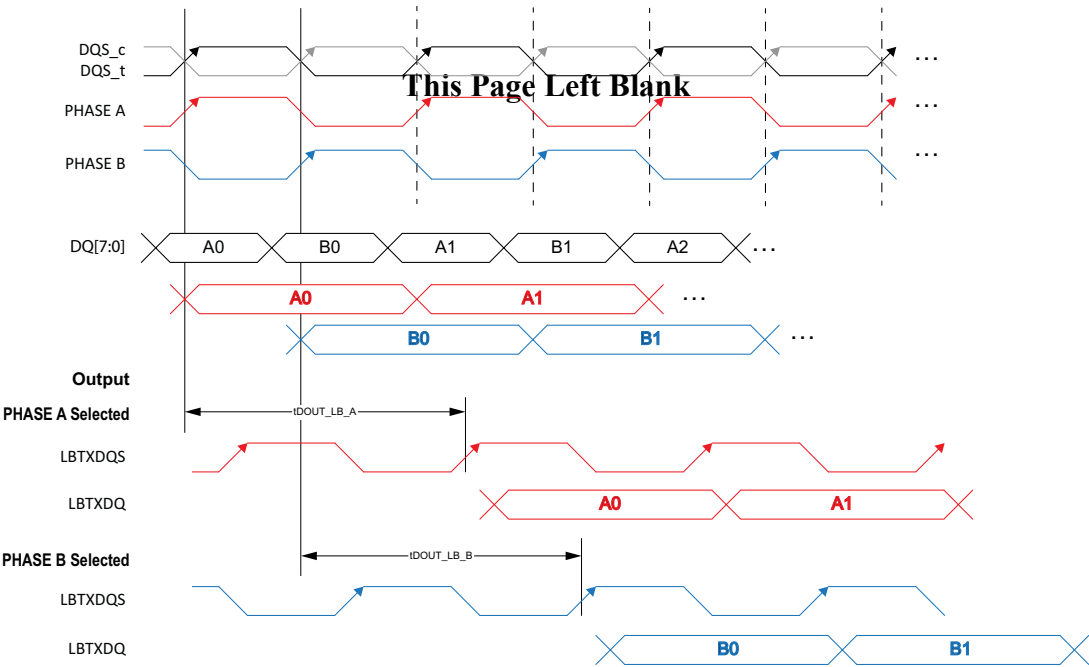


Figure 5 — Data Buffer Internal Phase Selection

3.5.3 Loopback Output Mode

Loopback Output Mode selects whether to output LBTXDQS and LBTXDQ in DQS Qualified Output Mode or WE Qualified Output Mode, based on [RW8D\[1\]](#). In the default DQS Qualified Output Mode ([RW8D\[1\]](#) = 0), the selected DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase. In WE Qualified Output Mode ([RW8D\[1\]](#) = 1), the selected DQ state will be output on LBTXDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

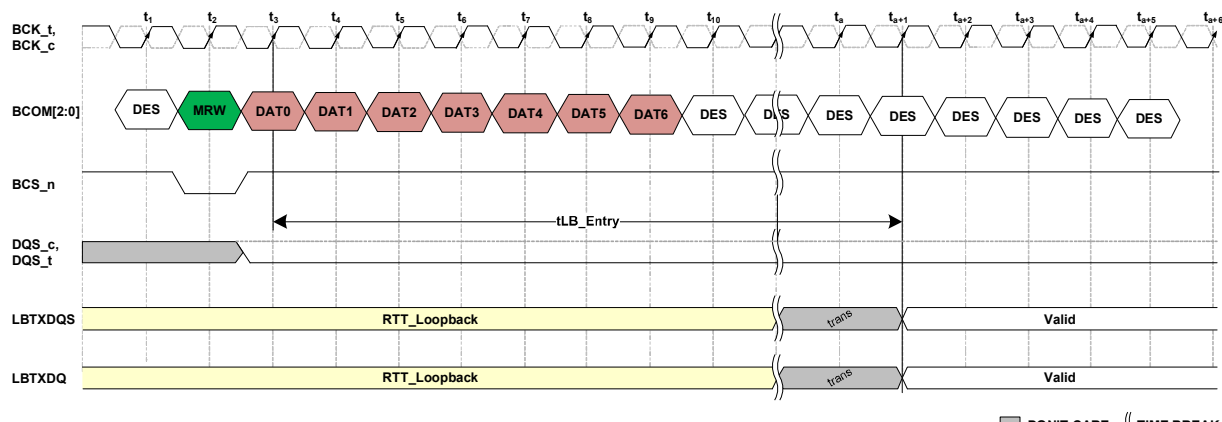


Figure 6 — Loopback Mode Entry for Output Modes Qualified by DQS or Qualified by WE

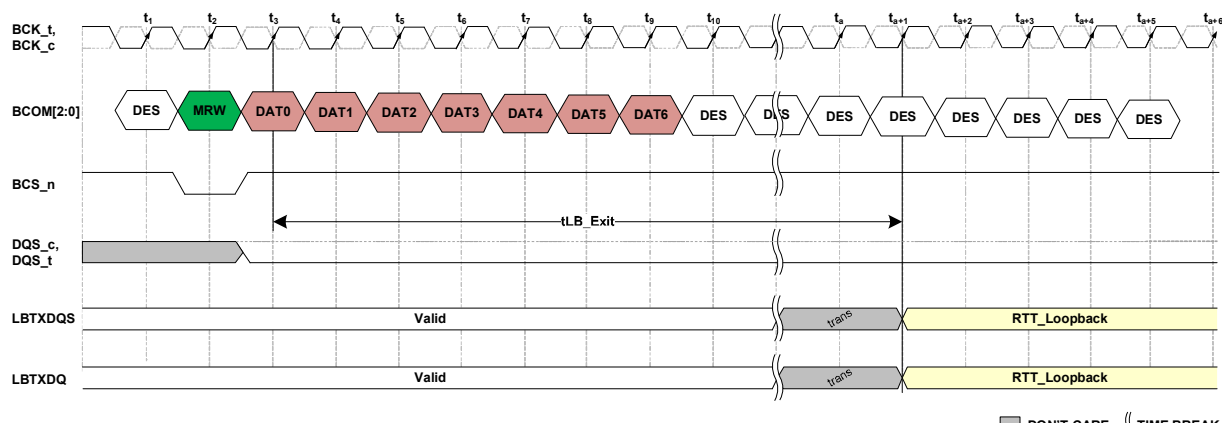


Figure 7 — Loopback Mode Exit for Output Modes Qualified by DQS or Qualified by WE

3.5.3.1 Loopback DQS Qualified Output Mode (Default)

In DQS Qualified Output Mode ($RW8D[1] = 0$), the selected DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase and output on LBTXDQ. The LBTXDQS output will be delayed by $tDOUT_LB_*$ from the selected DQS_t/DQS_c Loopback Phase. Since no Write commands are required in DQS Qualified Output Mode, MR settings pertaining to preamble, postamble, CWL are ignored by the Loopback function.

Additional requirements for DQS Qualified Output Mode:

- DQS must be driven differentially LOW (DQS_t LOW, DQS_c HIGH) prior to entry into DQS Qualified Output Mode.
- DQS_t/DQS_c must be continuously driven during Loopback operation. (Hi-Z state not allowed.)
- Only DSEL or MRW commands can be applied at BCOM[2:0]/BCS_n command pins during DQS Qualified Output Mode.

No DFE Reset is assumed after first rising edge of DQS_t. DRAM WR/RD operations are not supported after entering DQS Qualified Output Mode.

3.5.3.2 Loopback DQS Qualified Output Mode Timing Diagrams

Loopback DQS Qualified Output Mode entry and output example timing diagrams are shown below. The timing diagrams in Figure 8 and Figure 9 assume there have been other previous bursts of Loopback data.

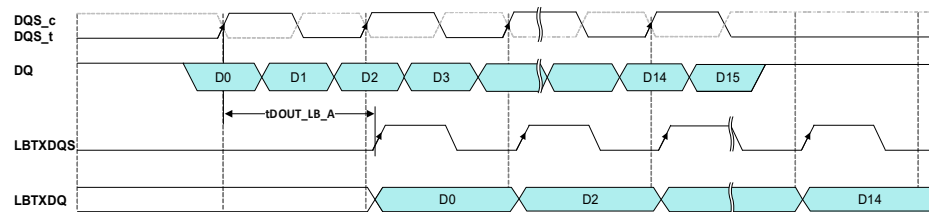


Figure 8 — Phase A is selected - DQS Qualified Output Mode

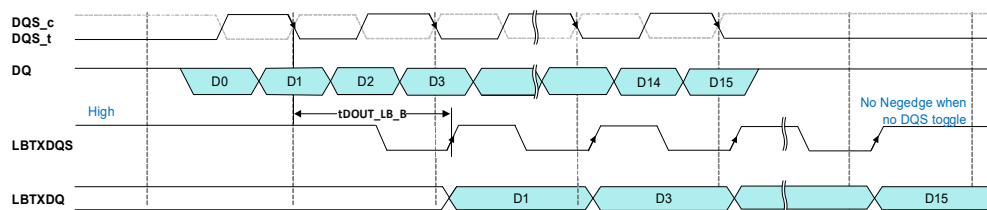


Figure 9 — Phase B is selected - DQS Qualified Output Mode

3.5.3.3 Loopback WE Qualified Output Mode

In WE Qualified Output Mode ($RW8D[1] = 1$), Loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal Write operation for the Command, DQS and DQ is assumed. MR settings pertaining to preamble, postamble, CWL apply, as they do for any Write command.

Implementation of 2-way interleave Loopback introduces complexity in Write Burst Mode when the DQS toggle is not continuous.

If the DQS toggle is continuously generated by Write commands spaced $BL/2$, Loopback will align the LBTXDQS/

LBTXDQ output with the selected phase for all write bursts. If the DQS toggle is not continuous due to gaps in Write commands spaced greater than $BL/2$, LBTXDQS/LBTXDQ may not align with the selected phase after the first write burst unless the “gap” is at least 16 CK (Write, $BL/2 + 16CK$, Write).

Table 6 — Loopback Output Phase

Write to Write Separation	Phase	NOTE
$X = BL/2$	Selected	
$BL/2 < X < BL/2 + 16$	Determined via analysis of specific conditions	1
$X \geq BL/2 + 16$	Selected	

Note 1: Specific conditions include selected phase, data rate, preamble, postamble and write burst gap duration.

In the case where continuous bursts are not issued in Loopback WE Qualified Output Mode, selection of Phase B may result in the last tHW_LBTXDQS width of a burst that does not comply with spec.

Additional requirements for WE Qualified Output Mode:

Write Leveling training is required prior to Write Burst Loopback operation.

All Write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data sent to DRAM, and the Loopback pins may not output the captured input data as expected.

3.5.3.4 Loopback WE Qualified Output Mode Timing Diagrams

Loopback WE Qualified Output Mode timing diagram examples are shown below. The timing diagrams in Figure 10 through Figure 25 assume there have been other previous bursts of Loopback data and the Loopback settings in [RW8D](#) have not been modified.

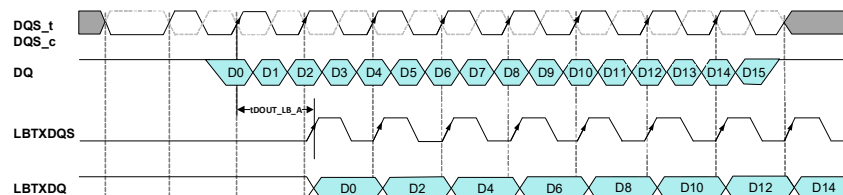


Figure 10 — Phase A: 2tCK or 3tCK Preamble – WE Qualified

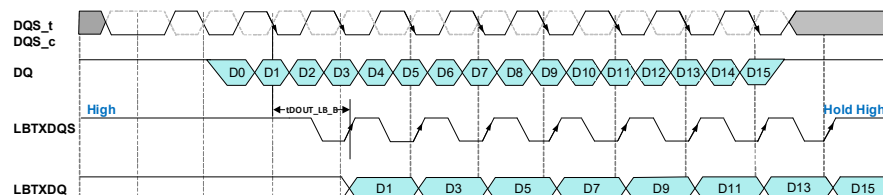


Figure 11 — Phase B: 2tCK or 3tCK Preamble – WE Qualified

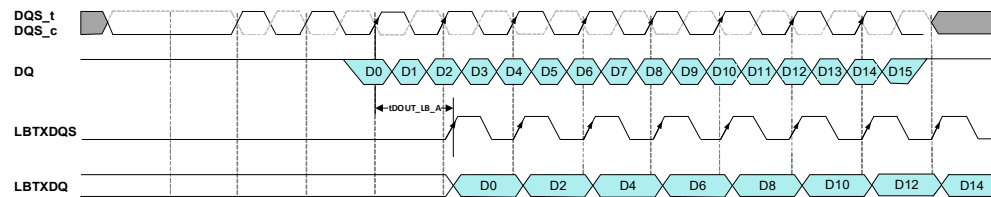


Figure 12 — Phase A: 4tCK Preamble - WE Qualified

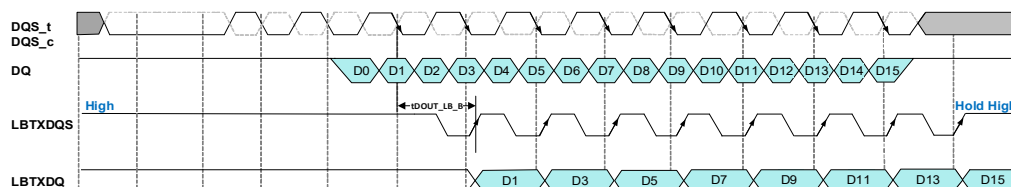


Figure 13 — Phase B: 4tCK Preamble - WE Qualified

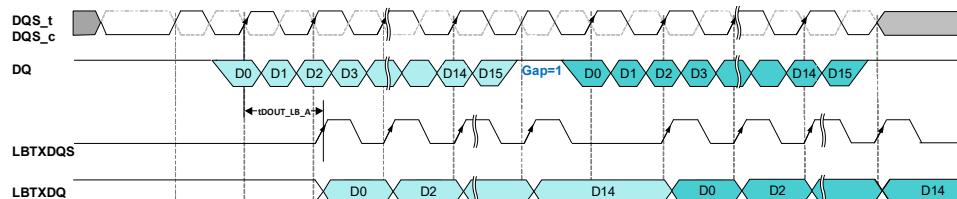


Figure 14 — Phase A: 2tCK or 3tCK Preamble and 1tCK Gap - WE Qualified

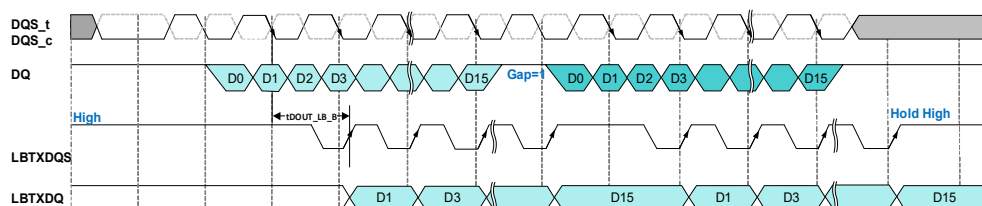


Figure 15 — Phase B: 2tCK or 3tCK Preamble and 1tCK Gap - WE Qualified

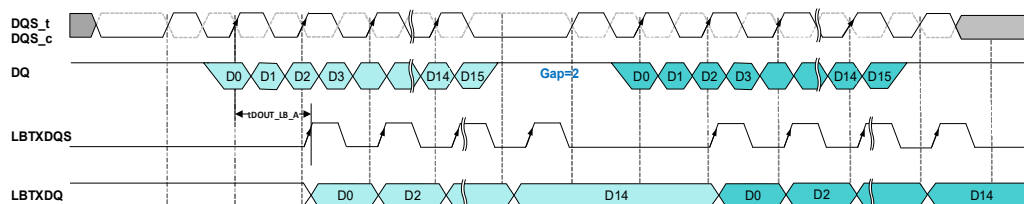


Figure 16 — Phase A: 2tCK or 3tCK Preamble and 2tCK Gap - WE Qualified

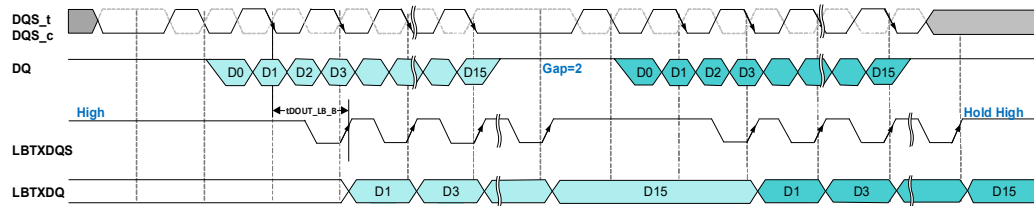


Figure 17 — Phase B: 2tCK or 3tCK Preamble and 2tCK Gap - WE Qualified

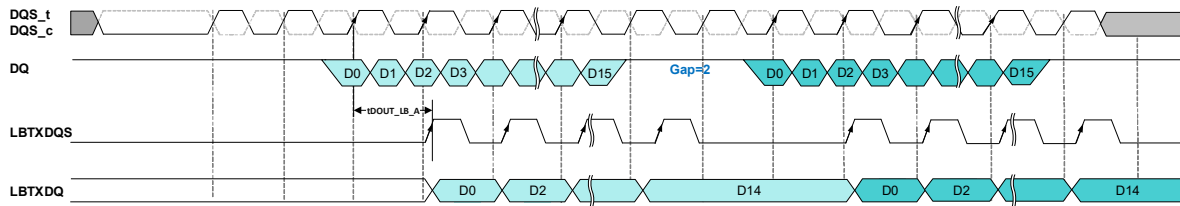


Figure 18 — Phase A: 4tCK Preamble and 2tCK Gap - WE Qualified

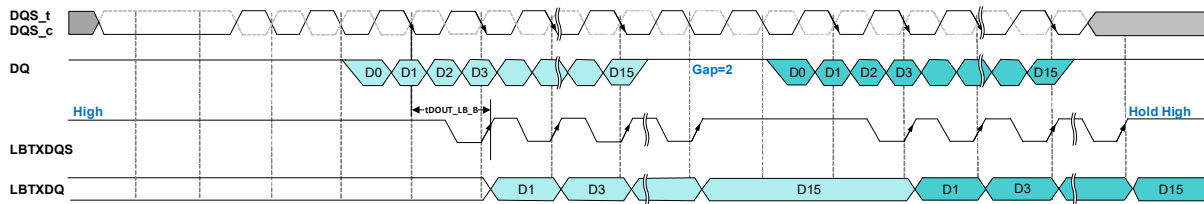


Figure 19 — Phase B: 4tCK Preamble and 2tCK Gap - WE Qualified

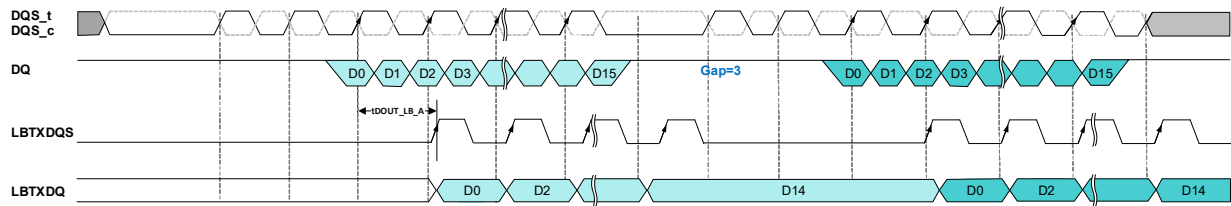


Figure 20 — Phase A: 4tCK Preamble and 3tCK Gap - WE Qualified

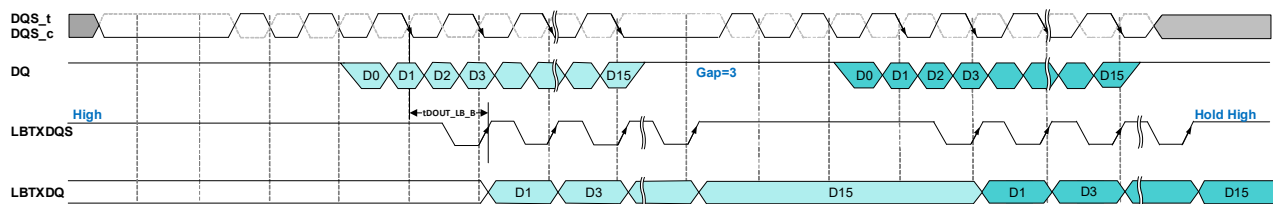


Figure 21 — Phase B: 4tCK Preamble and 3tCK Gap - WE Qualified

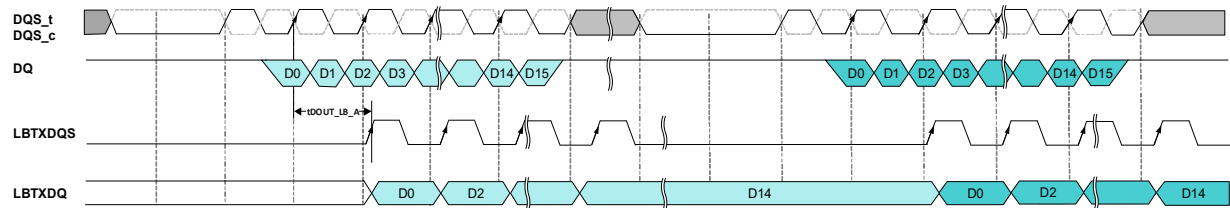


Figure 22 — Phase A: 2tCK or 3tCK Preamble without any Overlap - WE Qualified

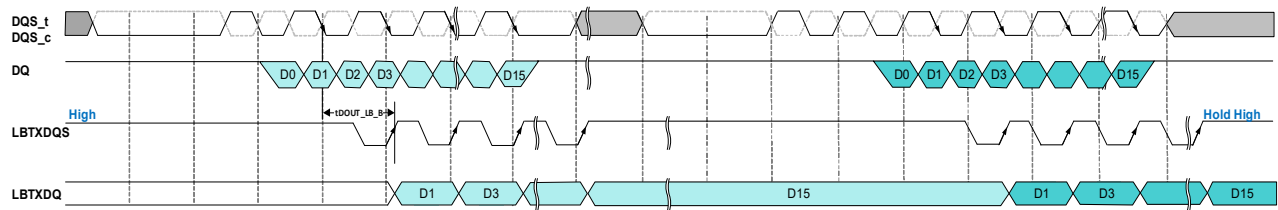


Figure 23 — Phase B: 2tCK or 3tCK Preamble without any Overlap - WE Qualified

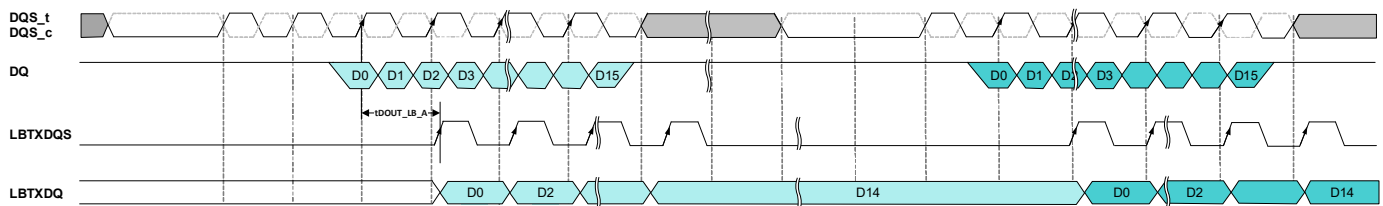


Figure 24 — Phase A: 4tCK Preamble without any Overlap - WE Qualified

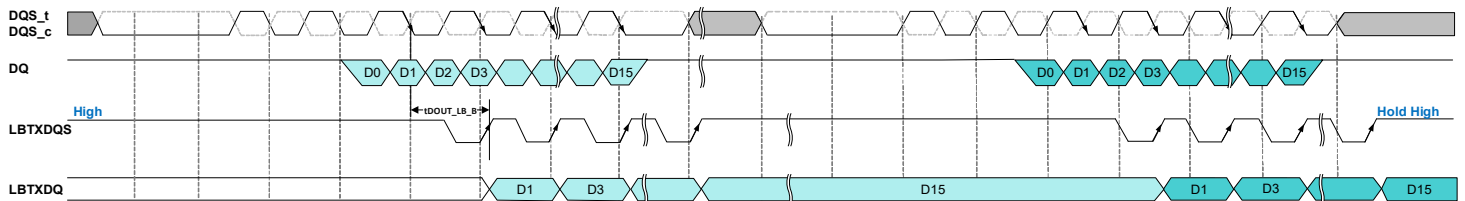


Figure 25 — Phase B: 4tCK Preamble without any Overlap - WE Qualified

3.5.4 Loopback Timing and Levels

The LBTXDQS output will be delayed from the selected DQS_t/DQS_c Loopback Phase. The timing parameter, tDOUT_LB_A/tDOUT_LB_B, is shown in Table 156, “Output timing requirements,” on page 167.

Loopback strobe LBTXDQS to Loopback data LBTXDQ relationship is illustrated in Figure 26.

- tHW_LBTXDQS describes the single-ended LBTXDQS strobe HIGH pulse width
- tLW_LBTXDQS describes the single-ended LBTXDQS strobe LOW pulse width
- tSK_LBTX describes the latest valid transition of LBTXDQ measured at both rising and falling edges of LBTXDQS
- tLBTXDQ_H describes the earliest invalid transition of LBTXDQ measured at both rising and falling edges of LBTXDQS
- tLBTXDQ_VW describes the data valid window per device per UI and is derived from (tLBTXDQ_H - tSK_LBTX) of each UI on a given Data Buffer

Table 156 on page 167 document the values for these timing parameters.

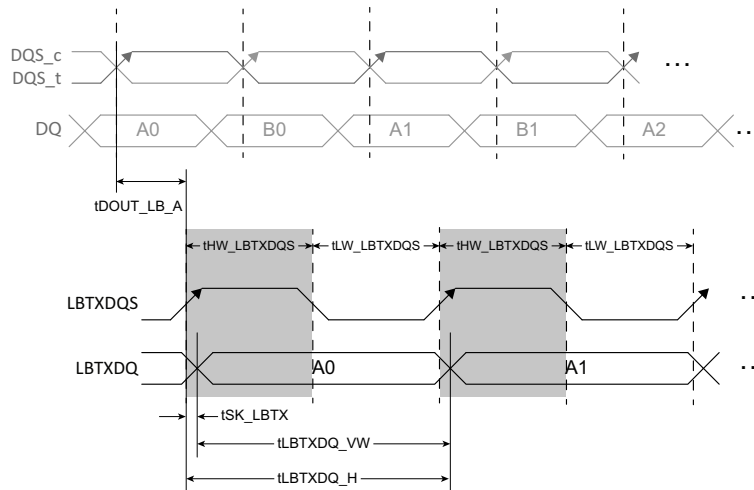


Figure 26 — Loopback Output Timing Parameters

ODT for Loopback is described in Section 14.2, “LBTXDQ/LBTXDQS On Die Termination DC Electrical Characteristics,” on page 181. Output driver electrical characteristics for Loopback is described in Section 15.2, “Output Driver DC Electrical Characteristics for LBTXDQS, LBTXDQ,” on page 198.

3.6 ZQ Calibration

The DDR5DB01 performs I/O circuit calibration when it receives a ZQ calibration in the MPC command. In order to use ZQ calibration command, a $240\ \Omega \pm 1\%$ resistor must be connected between the ZQCAL pin and V_{SS} .

Proper host interface RTT_NOM, RTT_WR, RTT_PARK DQ/DQS drive strength, DRAM interface RTT and MDQ/MDQS drive strength not guaranteed until a ZQ calibration has been performed. The host sends ZQCal Start and ZQCal Latch calibration commands through the DDR5RCD01 and forwards to DRAM and Data Buffer.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the Data Buffer's calibration procedure, and ZQCal Latch captures the result and loads it into the Data Buffer's drivers. A ZQCal Start command may be issued anytime the DB is in a state in which it can receive valid commands.

There are two timing parameters associated with ZQ Calibration. t_{ZQCAL} is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. t_{ZQLAT} is the time from when the ZQCal Latch MPC command is sent by the host to when the DQ bus can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after t_{ZQCAL} has expired and all DQ bus operations have completed. The DQ Bus must maintain a Deselect state during t_{ZQLAT} to allow ODT calibration settings to be updated.

After a ZQCal Start and until t_{ZQCAL} finishes, neither another ZQCal Start nor a ZQCAL Latch is allowed.

No other commands that cause data transfers on the host interface DQ/DQS outputs or the DRAM interface MDQ/MDQS outputs are allowed during ZQCal Latch.

The DDR5DB01 may or may not perform any calibration for its own I/O circuits on receipt of ZQCal Start.

3.7 Continuous Burst Mode

A continuous burst mode is configured with MRW to $RW90[0] = 1$. There are two usage models, one for DRAM interface test and the other for Host interface test.

For MDQ/MDQS test on the DRAM interface, the test sequence is as below:

1. Configure LFSR0 in $PG[8]RWE3$ and LFSR1 in $PG[8]RWE4$
2. Set $RW90[0]$ to 1
3. Enable MWD training mode in $RW83$
4. Send one WR command

Then the DB will start the pattern output on MDQ/MDQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW $RW90[0] = 0$ command to disable the continuous burst mode. After the WR command in Step 4 only MRW commands are allowed.

For DQ/DQS test on the Host interface, the test sequence is as below:

1. Configure LFSR0 in $PG[8]RWE3$ and LFSR1 in $PG[8]RWE4$
2. Set $RW90[0]$ to 1
3. Enable HIR training mode in $RW83$
4. Send one DB-space Short MRR command

Then the DB will start the pattern output on DQ/DQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW $RW90[0] = 0$ command to disable the continuous burst mode. After the DB-space MRR command in step 4 only MRW commands are allowed.

Using the continuous burst mode restarts the Data Pattern/LFSR. Additionally, the DB will not store the current seed value when it has exited the continuous burst mode, therefore any subsequent pattern reads will restart the seed to the programmed values of PG[8]RWE3 in PG[8]RWE4.

Once the MRW RW90[0] = 0 is registered by the DB, it will stop all pattern traffic by tCont_Exit. Since there is no min time for tCont_Exit, the DB may stop the pattern prior to tCont_Exit, potentially truncating any current burst pattern. After tCont_Exit_Delay has expired, any other valid command is then legal. All training patterns (modes) are supported in the continuous burst mode.

The DB will not store the current LFSR state when it exits continuous burst mode and it may clear the pattern values stored in PG[8]RW[E4:E3]. The host is required to program the seed/pattern again for subsequent runs.

3.8 Dynamic ODT Control on the Host interface

In certain application cases and to further enhance signal integrity on the Host interface data bus, it is desirable that the termination strength of the DB can be changed without issuing an MRW command. This requirement is supported by the “Dynamic ODT” feature as described as follows.

3.8.1 ODT Functional Description

There are four RTT values are available for DQ: RTT_NOM_RD, RTT_NOM_WR, RTT_PARK and RTT_WR. DQS only has one RTT value which is DQS_RTT_PARK.

- The value for DQ *RTT_NOM_RD* is preselected via RW88[5:3]
- The value for DQ *RTT_NOM_WR* is preselected via RW88[2:0]
- The value for DQ *RTT_WR* is preselected via RW87[5:3]
- The value for DQ *RTT_PARK* is preselected via RW87[2:0]
- The value for DQS *DQS_RTT_PARK* is preselected via RW86[2:0]
- RTT_NOM_RD & RTT_NOM_WR on/off timings are controlled via the respective NT Read and Write command and latencies.
- DQS_RTT_PARK is held static and is based on the value programmed in the RW listed above.

The combination of allowable CAS Latency settings and ODTLon offsets are shown in Table 7. Refer to the DDR5 SDRAM device specification for allowable combinations of ODTLon and ODLoft offset values.

Table 7 — Allowable CL and ODTLon Offset Combinations

		ODTLon_WR_Offset, ODTLon_WR_NT_Offset, ODTLon_RD_NT_Offset Setting					
		-4	-3	-2	-1	0	1
CAS Latency (CL)	22	Invalid	Invalid	Valid	Valid	Valid	Valid
	24	Invalid	Valid	Valid	Valid	Valid	Valid
	26	Valid	Valid	Valid	Valid	Valid	Valid
	>26	Valid	Valid	Valid	Valid	Valid	Valid

Table 8 — Latencies and Timing Parameters Relevant for Dynamic ODT when CRC is Disabled

Symbol	Parameter	Conditions	DDR5 speed bins 3200 to 4800	Unit	Note
tODTLon_WR_DB	ODT Latency On from target WRITE command to RTT Enable	From: Registering BCOM bus target write command To: Change RTT strength from Previous State to RTT WR	tODTLon_WR_DB = DB_WL(R) - tPDM_WR + ODTLon_WR_offset	ns	1,4
tODTLon_WR_NT_DB	ODT Latency On from NT WRITE command to RTT Enable	From: Registering BCOM bus NT write command To: Change RTT strength from Previous State to RTT NOM WR	tODTLon_WR_NT_DB = DB_WL(R0) - tPDM_WR + ODTLon_WR_NT_offset	ns	1,4
tODTLoFF_WR_DB	ODT Latency Off from target WRITE command to RTT Disable	From: Registering BCOM bus target write command To: Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM_RD/RTT_NOM_WR/Hi-Z	tODTLoFF_WR_DB = DB_WL(R) + BL/2 - tPDM_WR + ODTLoFF_WR_offset	ns	1,4
tODTLoFF_WR_NT_DB	ODT Latency Off from NT WRITE command to RTT Disable	From: Registering BCOM bus NT write command To: Change RTT strength from RTT_NOM_WR to RTT_PARK/RTT_NOM_RD/RTT_WR/Hi-Z	tODTLoFF_WR_NT_DB = DB_WL(R0) + BL/2 - tPDM_WR + ODTLoFF_WR_NT_offset	ns	1,4
tODTLoFF_RD_DB	Data Termination Disable	From: Registering BCOM bus target read command To: Disables the termination upon driving data	Data Termination Disable = DB_RL(R) + tPDM_RD - 1 tCK	ns	2
tODTLon_RD_DB	Data Termination Enable	From: Registering BCOM bus target read command To: Re-enables the termination after driving data	Data Termination Enable = DB_RL(R) + BL/2 + tPDM_RD	ns	2
tODTLoFF_RD_DQS_DB	Strobe Termination Disable	From: Registering BCOM bus target read command To: Disables the termination upon driving strobe	Strobe Termination Disable = DB_RL(R) - tRPRE + tPDM_RD - 1 tCK - Read DQS OFFSET	ns	2
tODTLon_RD_DQS_DB	Strobe Termination Enable	From: Registering BCOM bus target read command To: Re-enables the termination after driving strobe	Strobe Termination Enable = DB_RL(R) + BL/2 + tRPST - 0.5 tCK + tPDM_RD - Read DQS OFFSET	ns	2
tODTLon_RD_NT_DB	ODT Latency On from NT READ command to RTT Enable	From: Registering BCOM bus NT read command To: Change RTT strength from Previous State to RTT NOM RD	tODTLon_RD_NT_DB = DB_RL(R0) + tPDM_RD + ODTLon_RD_NT_offset	ns	1,4
tODTLoFF_RD_NT_DB	ODT Latency Off from NT READ command to RTT Disable	From: Registering BCOM bus NT read command To: Change RTT strength from RTT_NOM_RD to RTT_PARK/RTT_NOM_WR/RTT_WR/Hi-Z	tODTLoFF_RD_NT_DB = DB_RL(R0) + BL/2 + tPDM_RD + ODTLoFF_RD_NT_offset	ns	1,4
tADC	RTT change skew	From: Transitioning from one RTT State to the next RTT State To: RTT valid	tADC(min) = 0.2 tADC(max) = 0.8	tCK (avg)	3
Note(s): 1. All “_offset” parameters refer to the ODT Configuration Control Words in address space Page [B] . 2. For simplicity, Reads are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset control word to control it. To indicate this, it was named Data (or Strobe) Termination Disable and Enable. 3. When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained from the minimum of (RA, RB) to the maximum of (RA, RB). 4. ODT ON to Off pulse duration must be longer than the Data Burst Length (BL/2).					

3.8.2 ODT tADC Clarifications

tADC is defined as the time it takes for the Data Buffer to transition from one RTT state to the next RTT state. In case of the read, it is the time from the RTT state to the Data Buffer Drive state. Unless the RTT is specifically disabled, no High-Z state shall be allowed during tADC. During Data Buffer Drive state, the Data Buffer RON shall keep the DQ signal HIGH prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

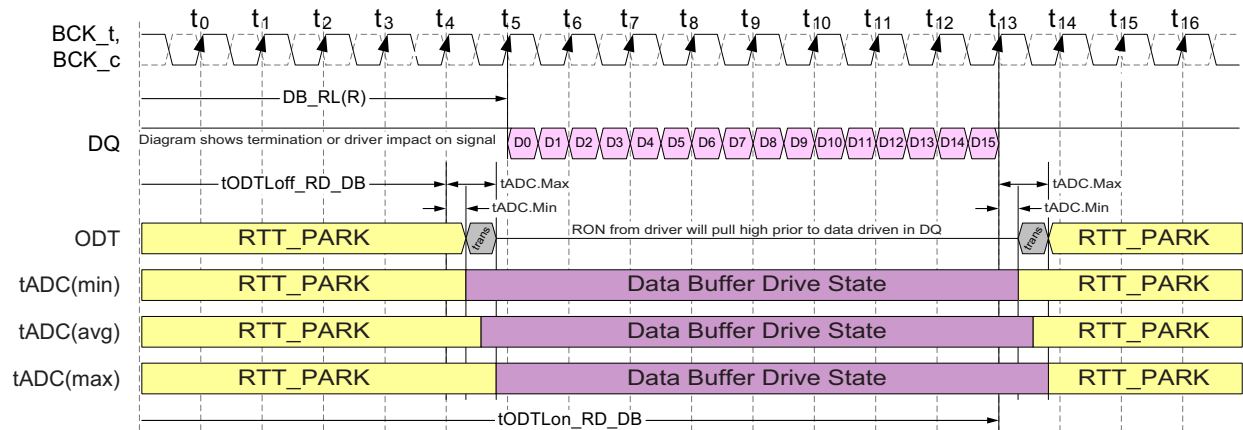


Figure 27 — Example of tADC

3.8.3 ODT Timing Diagrams

The following pages provide examples of ODT utilization timing diagrams. Examples of Write-to-Write, Read-to-Write, and Read-to-Read are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of tODL on/off times to ensure that preambles and postambles are included in the RTT ON time.

When there is a $1-t_{CK}$ ODT control gap for any ODT operation, the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

All timings noted in the figures below are just used as reference.

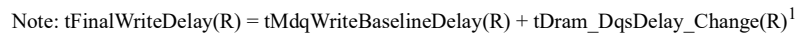


Figure 28 — Example of Burst Write Operation ODT Latencies

1. Devices are also allowed to apply the per-bit MDQ Write delay settings (PG[1:0]RW[F1:EE]) in the MDQ RTT PARK timings.

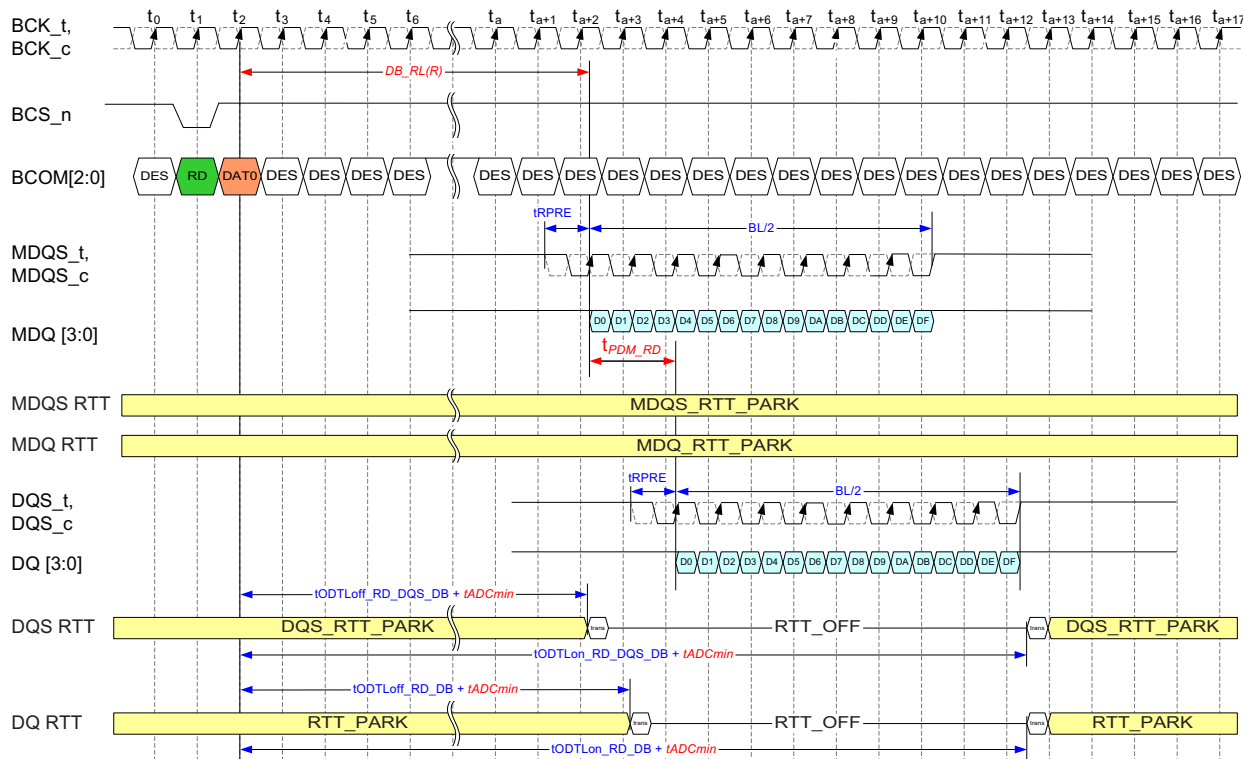


Figure 29 — Example of Burst Read Operation ODT Latencies

3.9 DRAM Periodic Update Support

To track the DRAM t_{DQS2DQ} drift per rank, a tracking mechanism is required to periodically monitor this drift and update the respective MDQ-MDQS write delay settings in the DB as required to compensate for the drift.

For the host to support this for LRDIMM, significant amounts of additional logic and MRW traffic overhead would be needed relative to the RDIMM case. An alternative is to have the Data Buffer assist the host in managing each DRAM's $t_{MDQS2MDQ}$ drift by providing most of the tracking functionality.

3.9.1 DRAM t_{DQS2DQ} Tracking Modes

- DRAM t_{DQS2DQ} tracking initialization mode
- DRAM t_{DQS2DQ} tracking mode.

Prior to performing DRAM t_{DQS2DQ} tracking, the DB requires the Host to issue an MPC to start a DQS interval oscillator measurement for each DRAM rank. The DB supports two ranks of DRAM t_{DQS2DQ} tracking per nibble.

- The *DRAM t_{DQS2DQ} tracking initialization mode* is used to calculate the initial DQS clock tree delay value for each DRAM nibble and rank in PG[A]RW[EF:E0]. The DB stores these values for later use during the DRAM t_{DQS2DQ} tracking mode. DRAM t_{DQS2DQ} tracking initialization on the DB only needs to be done by the host once after MDQ-MDQS Write Delay Training completes, since any delay adjustment due to drift is with respect to the trained values.

- The *DRAM tDQS2DQ tracking mode* is used to calculate the current DQS clock tree delay value for each DRAM nibble and rank stored in [PG\[A\]RW\[FF:F0\]](#). These are used to calculate the timing drift relative to their respective initial delay values, and then to update their respective MDQ-MDQS write delay values for drift compensation. DRAM tDQS2DQ tracking is performed periodically by the host as a function of system conditions. All operations, commands, and features are supported when tracking mode is enabled in [RWB0\[0\]](#) excepting during calculation window $t_{TrkCalcCur}$.

3.9.2 Operational Requirements

The following describes the operational requirements associated with the DRAM tDQS2DQ tracking feature:

- The DB initially enters the DRAM tDQS2DQ tracking initialization mode as a result of power-on initialization. When a DRAM-space MRR read to [MR47](#) is received, the DB will trigger a calculation update for the tracking initialization mode. It is the host's responsibility to issue the MPC command to start the DRAM DQS oscillator and to issue a DRAM-space MRR read to [MR46](#) prior to issuing a DRAM-space MRR read to [MR47](#).
- The DB supports DB-space MRW operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period. The host must make sure that these MRW operations do not interfere with any tracking-related settings or processes.
- The DB supports snooping of the DRAM-space MRW to the DRAM's DQS interval oscillator control register to obtain the DRAM's run-time count value needed for DQS clock tree calculations. The host must configure the DRAM to perform automatic stop based on its run-time count. The snooped value is loaded into the DB's DQS Interval Timer Run Time [MR45](#) register [PG\[8\]RWE7](#).
- The read data format of the DRAM-space MRR is assumed to be the same as defined for the DB-space MRR.
- The DB supports DB-space MRR operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period.
 - The initial and current DRAM DQS OSC Counter values captured by the DB from each DRAM nibble and rank are readable by the host via DB-space MRR.
 - The initial and current DRAM DQS clock tree delay values calculated by the DB for each DRAM nibble and rank are readable by the host via DB-space MRR.
- The host must read DRAM OSC Counter LSB [MR46](#) and MSB [MR47](#) registers sequentially as an {LSB, MSB} pair from the same rank. Upon issuing a DRAM-space read to [MR47](#), the host must block all transactions to all ranks for the duration of $t_{TrkCalcInit}$ if in tracking initialization mode, or for the duration of $t_{TrkCalcCur}$ if in tracking mode, to allow the DB to complete the calculation and update of the DRAM MDQ-MDQS write delay adjustment.
- Host-side read timing for rank-x is defined in the standard way as $DB_RL(Rx) + t_{PDM_RD}$ after the DAT0 cycle of the DRAM-space MRR command sequence. Data is returned using DB-space MRR read format.

3.9.3 DRAM tDQS2DQ Tracking Initialization Mode

To initialize the reference values for subsequent DRAM tDQS2DQ tracking in the DB, the host performs DRAM tDQS2DQ tracking initialization only once per rank after MDQS Write Delay Training completes. After power cycle reset the DB defaults to DRAM tDQS2DQ tracking initialization mode, or the mode can be set via a DB-space MRW to set [RWB0\[0\] = 0](#). To perform the initialization the host must first issue an MPC to start an initial DQS interval oscillator measurement for each DRAM rank (not shown).

The host will issue two sequential DRAM-space MRR commands to [MR46](#) and [MR47](#) to read the initial values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank.

When the host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register [MR46](#), the DB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in [PG\[A\]RWE0](#) for rank-0 or [PG\[A\]RWE2](#) for rank-1, and it stores the captured value for the upper nibble in [PG\[A\]RWE4](#) for rank-0 or [PG\[A\]RWE6](#) for rank-1. The DB will return a predefined value in

RWB1 to the Host.

When the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register **MR47**, the DB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in **PG[A]RWE1** for rank-0 or **PG[A]RWE3** for rank-1, and it stores the captured value for the upper nibble in **PG[A]RWE5** for rank-0 or **PG[A]RWE7** for rank-1. The DB will return a predefined value in **RWB1** to the Host.

As shown in Figure 30, the host must meet the t_{MRROD1} timing parameter between MRR operations to DRAM-space **MR46** and **MR47**. In general, MRR operations to DRAM-space **MR46** and **MR47** must also be considered as DB space MRR operations from the timing point of view since the DB returns the contents of **RWB1** to the Host.

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the DB will then calculate the initial DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the DB then stores the calculated value for the lower nibble in **PG[A]RWE8** and **PG[A]RWE9** for rank-0 or **PG[A]RWEA** and **PG[A]RWEB** for rank-1, and it stores the calculated value for the upper nibble in **PG[A]RWE C** and **PG[A]RWE D** for rank-0 or **PG[A]RWE E** and **PG[A]RWE F** for rank-1. The calculate and store operations complete within $t_{TrkCalcInit}$.

From the time when the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register **MR47** to the end of the $t_{TrkCalcInit}$ period, only DES and NOP commands are legal. Once the period has completed for the specified rank, the DB will remain in the tracking initialization mode as shown in Figure 30. The host can then execute DRAM t_{DQS2DQ} tracking initialization functions at a later time to perform the t_{DQS2DQ} tracking initialization process to the other rank.

At the end of DRAM t_{DQS2DQ} Tracking Initialization, both Initial DRAM DQS Clock Tree Delay and Current DRAM DQS Clock Tree Delay share the same value. This results in $t_{DRAM_DqsDelay_Change}$ being equal to 0 which means no change to the MDQ-to-MDQS Write Delay.

As depicted in Figure 32, the t_{DQS2DQ} Tracking Initialization Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in **PG[A]RW[E1, E3, E5, E7]**. In the case of direct MRW access, the tracking mode selection bit **RWB0[0]** is ignored and the host is required to meet applicable timing parameters in Table 155.

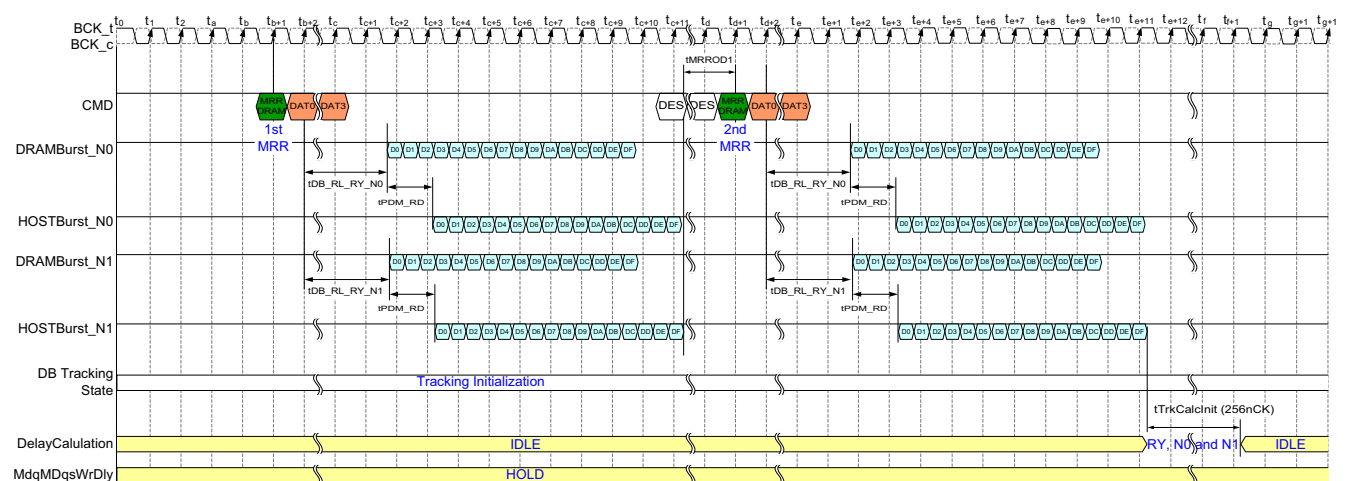


Figure 30 — DRAM t_{DQ2DQ} Tracking Initialization Mode Flow

3.9.4 DRAM tDQS2DQ Tracking Mode

DRAM tDQS2DQ tracking is performed periodically by the host as a function of system conditions. After the DRAM tDQS2DQ tracking initialization has completed, the host must set the DB in DRAM tDQS2DQ tracking mode via a DB-space MRW to set [RWB\[0\]](#) = 1. To perform the tracking the host shall issue an MPC to start a DQS interval oscillator measurement for each DRAM rank (not shown). After starting the DRAM DQS interval oscillator the host will issue two sequential DRAM-space MRR commands to [MR46](#) and [MR47](#) to read the current values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank. The read process is the same as described in the Initialization mode except that different DB registers are used for value storage.

When the host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register [MR46](#), the DB stores the captured value for the lower nibble in [PG\[A\]RWF0](#) for rank-0 or [PG\[A\]RWF2](#) for rank-1, and it stores the captured value for the upper nibble in [PG\[A\]RWF4](#) for rank-0 or [PG\[A\]RWF6](#) for rank-1. The DB will return a predefined value in [RWB1](#).

As shown in Figure 31 the host must meet the t_{MRROD1} timing parameter between MRR operations to DRAM-space [MR46](#) and [MR47](#). In general, MRR operations to DRAM-space [MR46](#) and [MR47](#) must also be considered as DB-space MRR operations from the timing point of view since the DB returns the contents of [RWB1](#) to the Host.

When the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#), the DB stores the captured value for the lower nibble in [PG\[A\]RWF1](#) for rank-0 or [PG\[A\]RWF3](#) for rank-1, and it stores the captured value for the upper nibble in [PG\[A\]RWF5](#) for rank-0 or [PG\[A\]RWF7](#) for rank-1. The DB will return a predefined value in [RWB1](#).

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the DB will then calculate the current DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the DB then stores the calculated value for the lower nibble in [PG\[A\]RWF8](#) and [PG\[A\]RWF9](#) for rank-0 or [PG\[A\]RWF8](#) and [PG\[A\]RWF9](#) for rank-1, and it stores the calculated value for the upper nibble in [PG\[A\]RWF8](#) and [PG\[A\]RWF9](#) for rank-0 or [PG\[A\]RWF8](#) and [PG\[A\]RWF9](#) for rank-1. The DB will update the applied MDQ-MDQS write delay value for each nibble of the rank based on its MDQ write baseline delay and its stored initial and current DQS clock tree delay values. The calculate, store and update operations must complete within $t_{TrkCalcCur}$. From the time when the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#) to the end of the $t_{TrkCalcCur}$ period, only DES and NOP commands are legal.

Once the $t_{TrkCalcCur}$ period has completed for the specified rank, the DB will remain in tracking mode as shown in Figure 31.

As shown in Figure 33, the tDQS2DQ Tracking Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in [PG\[A\]RW\[F1, F3, F5, F7\]](#). In the case of direct MRW access, the tracking mode selection bit [RWB0\[0\]](#) is ignored and the host is required to meet applicable timing parameters in Table 155.

3.9.5 MDQ-MDQS Adjustment Calculations

The DB is only required to support calculation for one rank at a given time, in each x4 nibble. The MDQ-MDQS write delay adjustment calculation for each nibble, N_y , of a specified rank, R_x , is as follows.

The initial count from the DRAM tDQS2DQ tracking initialization step provides the initial DRAM DQS clock tree delay in units of $t_{CK}/128$:

$$t_{Dram_DqsDelay_Initial}(R_x, N_y) = \text{Dram_RunTimeCount} * t_{CK} / (2 * \text{Dram_DQSOscCount_Initial}(R_x, N_y)).$$

For each DRAM tDQS2DQ tracking step, the current count provides the drifted DRAM DQS clock tree delay in units of tCK/128:

$$t_{\text{Dram_DqsDelay_Current}}(\text{Rx}, \text{Ny}) = \text{Dram_RunTimeCount} * t_{\text{CK}} / (2 * \text{Dram_DQSOscCount_Current}(\text{Rx}, \text{Ny}))$$

The change in the DRAM DQS clock tree delay is calculated in units of tCK/64:

$$t_{\text{Dram_DqsDelay_Change}}(\text{Rx}, \text{Ny}) = t_{\text{Dram_DqsDelay_Current}}(\text{Rx}, \text{Ny}) - t_{\text{Dram_DqsDelay_Initial}}(\text{Rx}, \text{Ny}).$$

The DB then updates the applied MDQ-MDQS write delay values as:

$$t_{\text{MdqMdqsWriteDelay}}(\text{Rx}, \text{Ny}) = t_{\text{MdqWriteBaselineDelay}}(\text{Rx}, \text{Ny}) + t_{\text{Dram_DqsDelay_Change}}(\text{Rx}, \text{Ny})$$

Each MDQ write baseline delay register is not updated from its trained value. Instead, its value is offset by its respective tDram_DqsDelay_Change value before being applied to the delay circuitry.

As an example, if the current DQS clock tree delay is larger than the initial DQS clock tree delay, the DQS clock tree delay has increased by tDram_DqsDelay_Change, so the applied MDQ-MDQS write delay needs to be increased by this amount.

For the Final Write Delay including all offset contributors such as tDRAM_DQSDelay_Change from Page PG[A] and PG[1:0]RW[EE:F1] (per-bit Write Delays), the DDR5DB01 device is only required to support the $-0.5 * t_{\text{CK}}(\text{minimum})$ to $+3.5 * t_{\text{CK}}(\text{maximum})$ delay range defined for the Write Delay baseline control words in PG[1:0]RW[E6:E7].

In cases where control words in PG[1:0]RW[E6:E7], PG[1:0]RW[EE:F1], and Page PG[A] are programmed with settings that would cause any Final Write Delay value to be outside the delay range supported by the device, the DB will saturate the effective Final Write Delay values at the maximum or minimum (as applicable) of the delay range it supports.

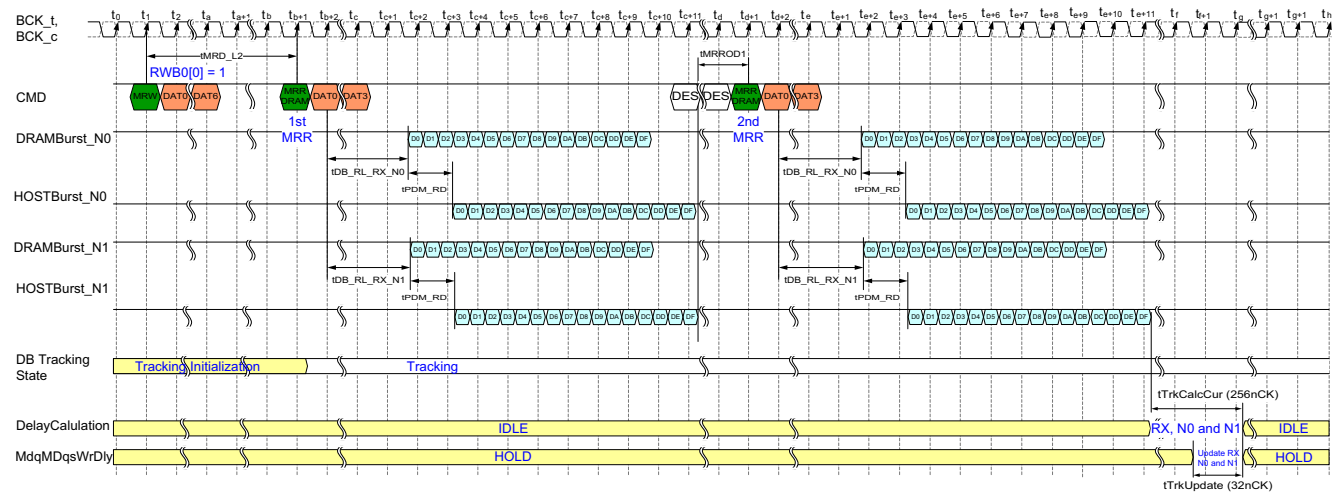


Figure 31 — DRAM tDQS2DQ Tracking Mode Flow

3.9.6 DRAM interval Oscillator Snoop Value

The DB configures PG[8]RWE7 with the snooped value from a DRAM-space MRW to the DRAM's interval oscillator control register MR45. The DB uses the snooped interval timer stop value, referred to as the run-time count value, for DRAM DQS clock tree delay calculations. The host must make sure that the DRAM's run-time count value is configured as necessary. It must also make sure that the DRAM's interval oscillator is configured for automatic stop based on its run-time count value.

Although PG[8]RWE7 can be written directly by the host, the intent is that it will not be written directly by the host after it has been configured with the snooped value. Writing to this register directly is intended for debug purposes.

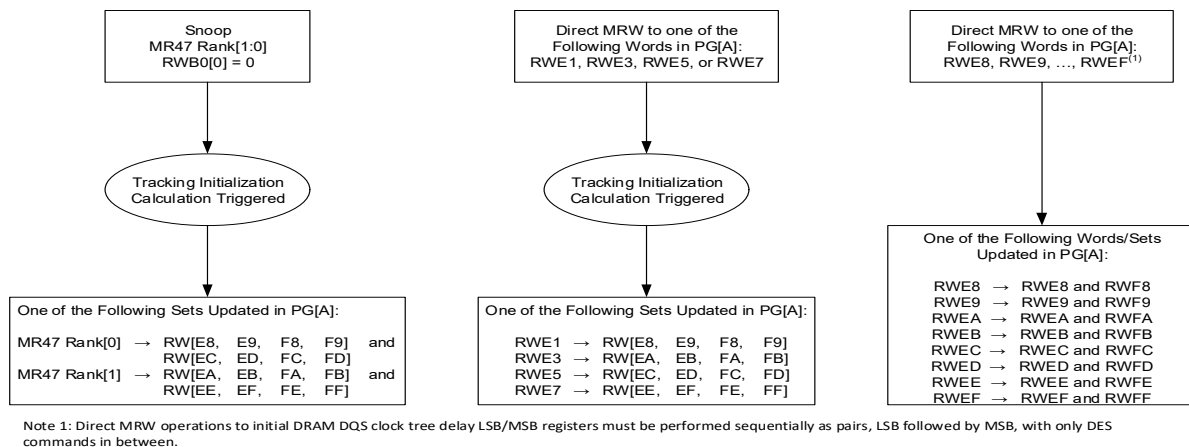


Figure 32 — tDQS2DQ Tracking Initialization Sequences

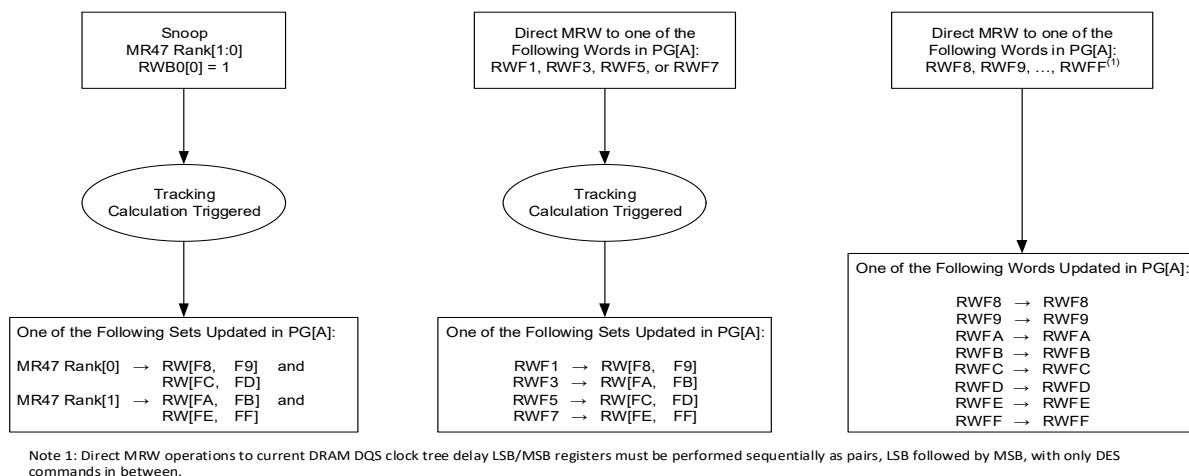


Figure 33 — tDQS2DQ Tracking Sequences

4 Power Down operation

DDR5 does not have a separate CKE signal going to the DIMM or the DBs. Power Down Entry, including self refresh, is signaled via a command sequence on the BCOM interface. A BCS_n active pulse will take the Data Buffer out of the power down state. A NOP command is placed on the BCOM bus along with BCS_n pulse so that no commands are executed by the DB devices. The DDR5DB01 can be put in power down mode with or without non-target ODT control.

4.1 Power Savings Modes

The DDR5DB01 device supports the following power saving mechanisms:

- PDE Power Down Mode.
- PDE Power Down with ODT control. In this mode ranks can be in power down mode but will still require ODT commands for termination, therefore the RCD and Data buffer will remain in normal operating mode.
- Self Refresh Modes. With and without Clock Stop.

4.1.1 PDE Power Down Mode

The DB device enters power down mode when it receives a PDE command sequence on the BCOM interface. Due to the external V_{DD} termination, all BCOM[2:0] and BCS_n inputs of the Data Buffer remain HIGH during PDE power down mode just as in Deselect operation. The DB may reduce power internally as it is able.

The PDE command is sent to the Data Buffers on the BCOM bus only when the last rank has entered PDE mode. The PDX command is sent to the Data Buffers on the BCOM bus when the first rank receives the PDX command. Therefore, the Data Buffers are in power down mode only when ALL ranks on the sub channel are in power down mode. Also, because of this, a two-cycle PDE command on the BCOM[2:0] bus can be followed immediately by a PDX command.

4.1.2 PDE Power Down Mode with ODT Control Enabled

Power Down with ODT Control Enabled when the DB receives a PDE Command DAT0 BCOM[1:0] = '10'. In PDE Power Down Mode with ODT control, the Data Buffers may still receive non-target termination commands.

While in PDE with ODT control, RD, WR, and MRR commands may be sent to the Data Buffer. It is the responsibility of the host controller to not send commands which are "Not Allowed", as defined in Table 9. The non-target termination commands must be sent to the Data Buffers when they are in PDE with ODT control.

Table 9 — ODT Control during Power Down Mode¹

Mode	NOP/PDX command	RD w/ non-target term	WR w/ non-target term	MRR w/ non-target term	All Others
PDE w/o ODT control	Allowed. Exits PDE mode	Not Allowed	Not Allowed	Not Allowed	Not Allowed
PDE w/ODT control	Allowed. Exits PDE Mode	Allowed	Allowed	Allowed	Not Allowed

1. This table applies to the commands sent from the RCD to the Data Buffer when the Data Buffer is in PDE state with ODT Control.

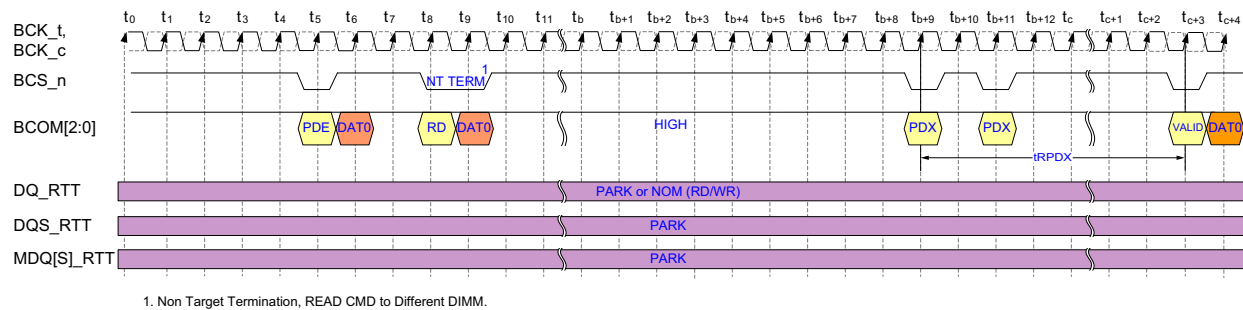


Figure 34 — Power Down with ODT Control Enabled Mode Entry and Exit

4.1.3 PDE Power Down Mode without ODT Control Disabled

Power Down with ODT Control Enabled when the DB receives a PDE Command DAT0 BCOM[1:0] = '11'. In PDE Power Down Mode without ODT control, the Data Buffers does not process any commands excepting for Power Down Exit.

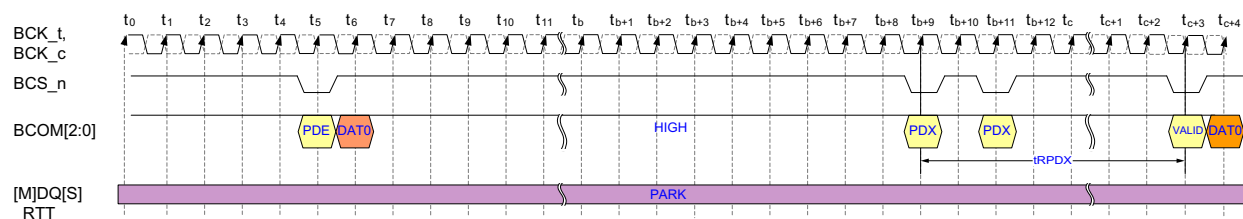


Figure 35 — Power Down with ODT Control Disabled Mode Entry and Exit

4.2 Self Refresh Modes

After the SRE command is received by the Data Buffer (i.e., PDE Command DAT0 BCOM[1] = 0), the DB input clock may stop as BCK_t = BCK_c = HIGH. When the BCK clock is running, the BCS_n signal must remain HIGH in order for the DB to stay in Self Refresh state. A BCS_n active (LOW) pulse instructs the Data Buffer to get out from SRE state.

4.2.1 Self Refresh Mode with Clock Stop Entry

Self Refresh Mode is a very low power state in which the input clocks can stop and the DB on-die terminations, including RTT_PARK, are disabled. Self-refresh entry is signaled when the RCD sends SRE command on the BCOM[2:0] control bus (i.e., PDE Command DAT0 BCOM[1] = 0). See Figure 36, “Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by PDE Command with SRE Indication,” on page 30 through Figure 39, “Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by Clock Stop Detection Circuit,” on page 31.

The DDR5DB01 uses a clock-stop detection circuit to disable the command bus BCK_t/BCK_c, BCOM[2:0], and BCS_n receivers. When the clock stops, BCK_t and BCK_c will be driven or pulled up HIGH, respectively, by the Host or by the discrete termination resistors on the module. Similarly, BCS_n, and BCOM[2:0] signals will be pulled HIGH by the Host or the termination resistors. Note that the BCS_n is NOT driven LOW when in self refresh.

The DDR5DB01 will disable DQ/DQS and MDQ/MDQS on-die terminations during Self Refresh with Clock Stop. The DB may disable on die terminations using the PDE command with SRE indication as shown in Figure 36 on page 30 and Figure 38 on page 31. The DB may also rely on the clock-stop detection circuit for this purpose as shown in Figure 37 and Figure 39 on page 31. Either method is acceptable.

4.2.2 Exit from Self Refresh Mode with Clock Stop

To exit the Clock Stop condition, the Host starts the BCK clocks with stable frequency and phase while keeping BCOM[2:0] and BCS_n signals HIGH.

On die terminations in the DB can get re-enabled either by the first NOP command following exit from Clock-Stop condition as depicted in Figure 36 and Figure 38 or by the exit from Clock-Stop condition directly as shown in Figure 37 and Figure 39.

If the BCOM[2:0] and BCS_n bus timings have not been trained for the current frequency of operation, after a wait of $t_{\text{STAB_DB}}$ from when the BCK clocks are toggling with stable phase and frequency, the host is allowed to apply the “BCOMTM Entry” strap command (see Table 27 on page 52) to train the BCOM[2:0] and BCS_n signal timings.

The BCS_n signal is allowed to pulse LOW for one cycle (with valid timings) after a wait of $t_{\text{STAB_DB}}$ from when the BCK clocks are toggling with stable phase and frequency. This BCS_n LOW pulse instructs the DDR5DB01 to exit from Self Refresh mode.

4.2.3 Self Refresh Mode without Clock Stop Entry

As seen in Figure 40 on page 32, Self Refresh without Clock Stop is similar to Self Refresh with Clock Stop mode except that the Host will not stop the BCK clock in this mode.

The DDR5DB01 device may disable on die terminations during Self Refresh without Clock Stop using the PDE command with SRE indication as a trigger as shown in Figure 40 on page 32. The DB is also allowed to keep on-die terminations (RTT_PARK) enabled as shown in Figure 41. Either method is acceptable.

4.2.4 Self Refresh Mode without Clock Stop Exit

Exiting this mode is similar to Self Refresh with Clock Stop, except that the host will not wait $t_{\text{STAB_DB}}$ upon exit, as the clock circuitry in the Data Buffer stays locked.

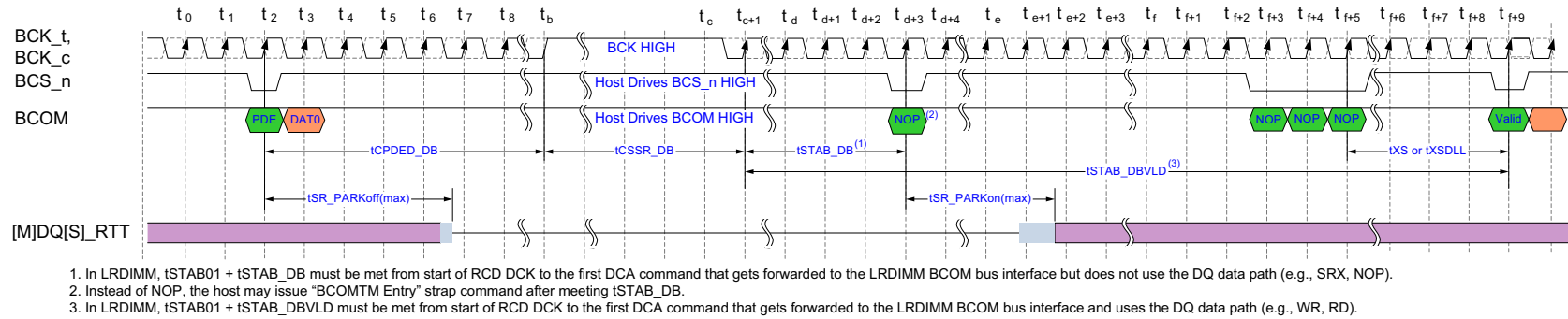


Figure 36 — Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by PDE Command with SRE Indication

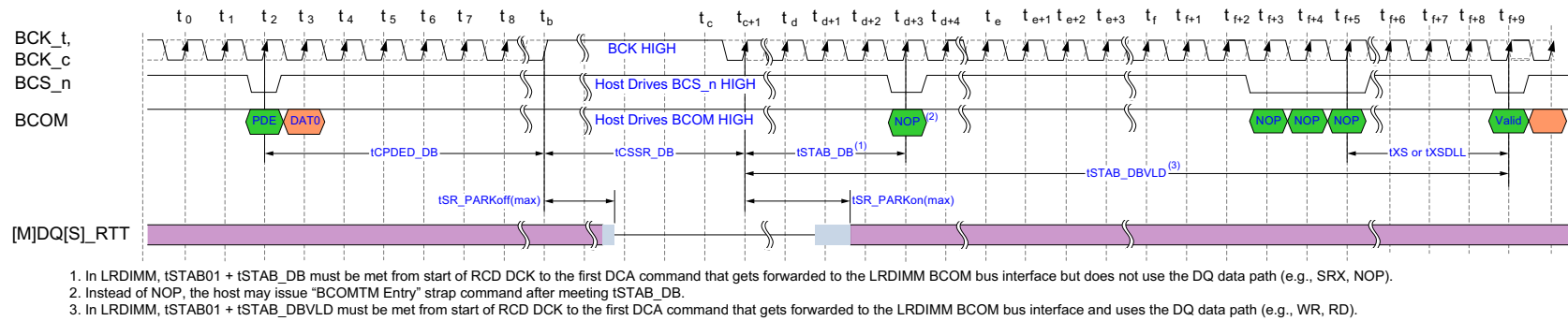


Figure 37 — Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by Clock Stop Detection Circuit

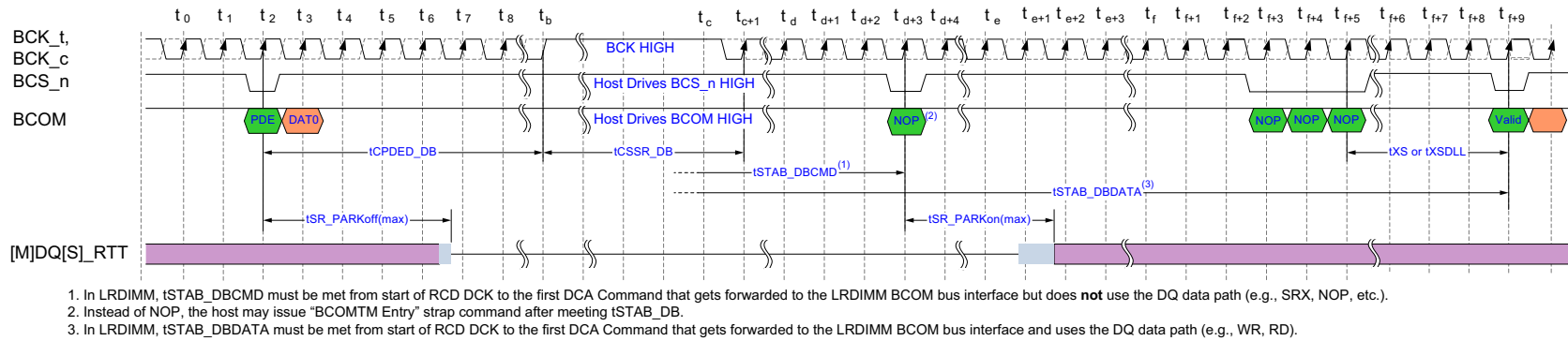


Figure 38 — Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by PDE Command with SRE Indication

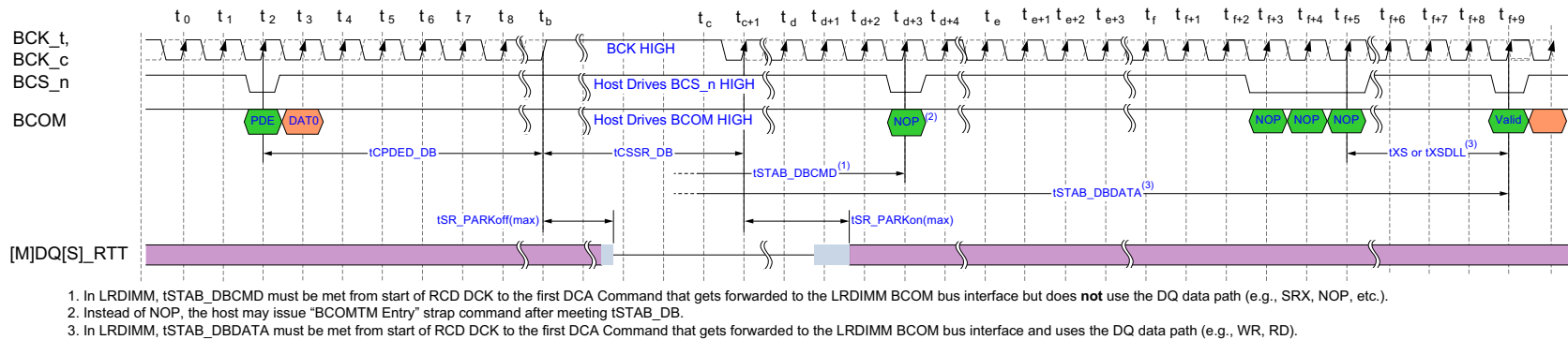


Figure 39 — Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by Clock Stop Detection Circuit

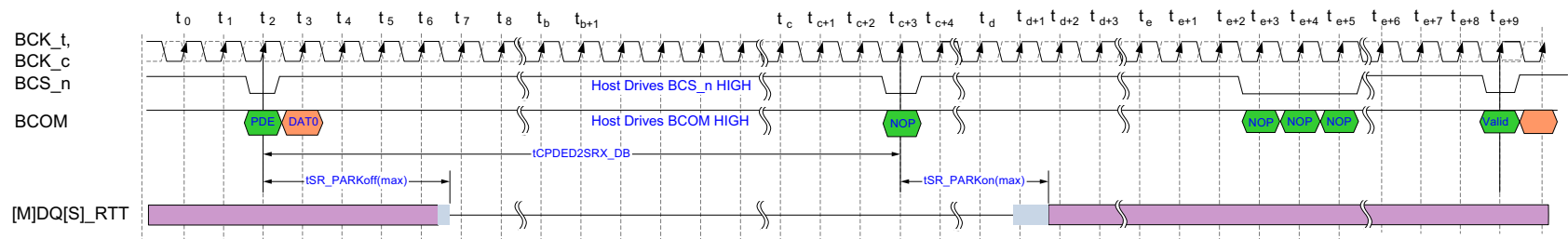


Figure 40 — Self Refresh Entry and Exit without Clock Stop – Termination Disabled by PDE Command with SRE Indication

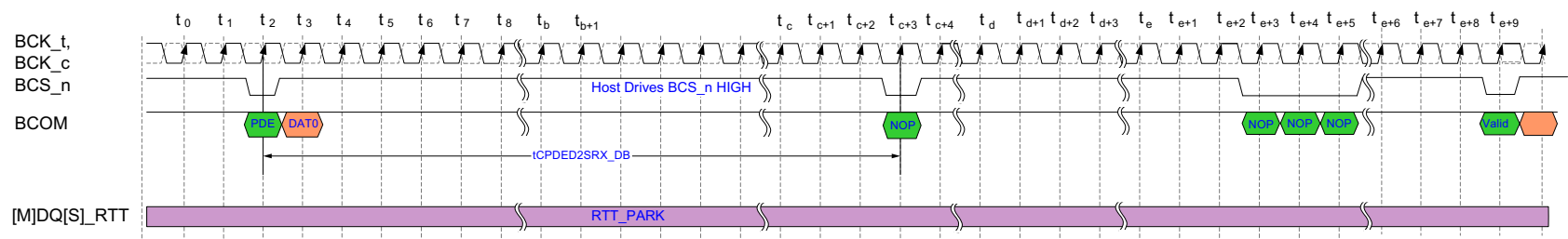


Figure 41 — Self Refresh Entry and Exit without Clock Stop – RTT_PARK Remains Enabled

5

Data Buffer Control Bus

This section describes the signals used in the DDR5 LRDIMM control bus that connects the DDR5 Register with each of the ten DDR5 Data Buffer (DB).

5.1

Control Bus Signals

Table 10 — List of Signals for Data Buffer Control Signals

Name	Description	Signal Count per channel
BCS_n	BCOM Chip Select	1
BCOM[2:0]	Data buffer command signals	3
BRST_n	BCOM Reset	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
Total		7

5.1.1

Control Bus Signal Termination

BCK_t, BCK_c, BCS_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 LRDIMM as shown in figure.

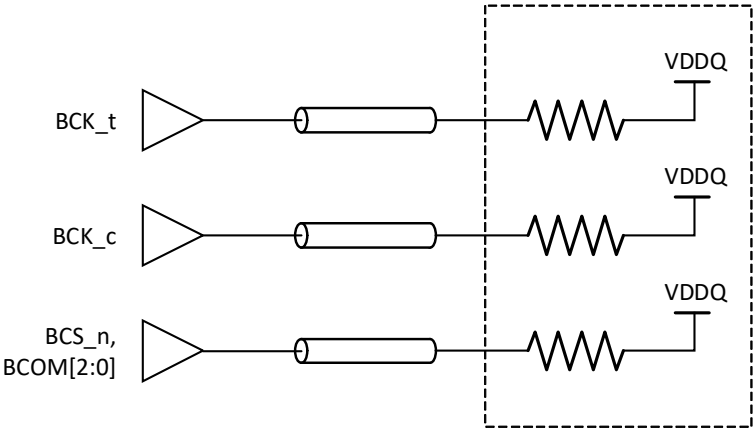


Figure 42 — Control Bus Termination

5.1.2 Control Bus Timing

The output BCOM signals are driven one clock later than the QnxCA outputs as shown in Figure 44. Like the QnxCA outputs, they are delayed by the RCD Command Latency Adder Control Word [RW11](#).

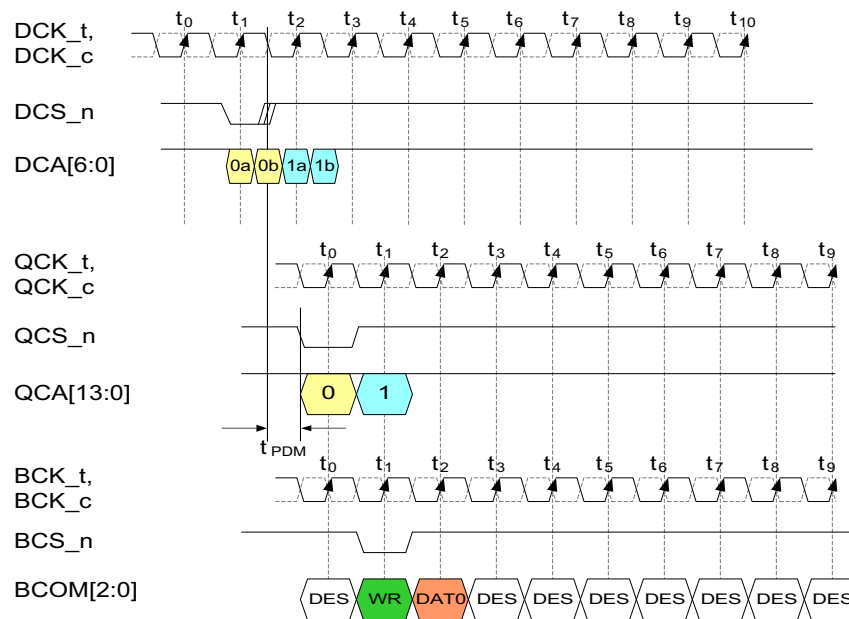


Figure 43 — Example BCOM 1N WR Command

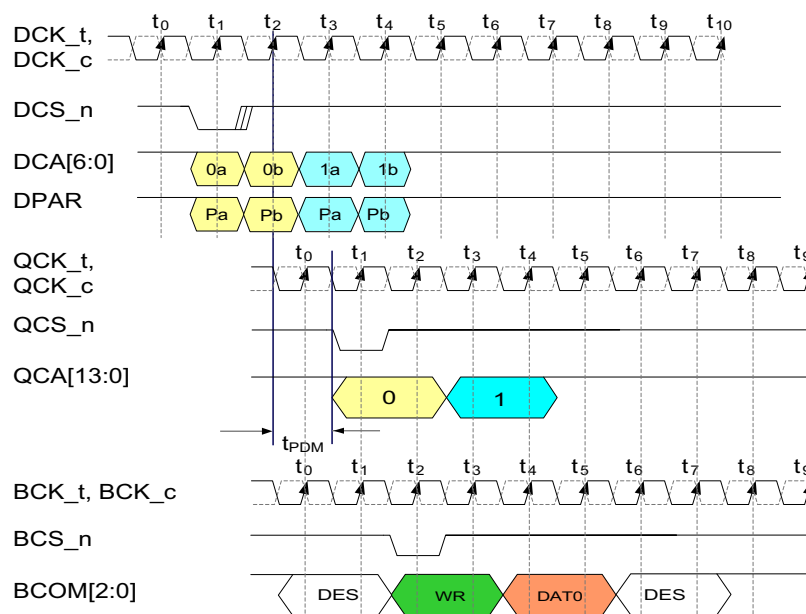


Figure 44 — Example BCOM 2N WR Command