

JEDEC STANDARD

DDR5 Clock Driver Definition (DDR5CKD01)

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DDR5 Clock Driver Definition (DDR5CKD01)

(From JEDEC Board Ballot JCB-23-55, formulated under the cognizance of the JC-40.4 sub-committee on Registered and Fully Buffered Memory Support Logic, item number 344.99D).

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR5 Clock Driver (CKD) for re-driving the DCK for CUDIMM, CSODIMM, and CAMM applications. The DDR5CKD01 Device ID is DID = 0x0531. (5 = DDR5, 3= Clock Driver, 1= rev 01)

The terms ‘DDR5CKD01, Clock Driver, ‘CKD’, or ‘device’ are used interchangeably to refer to this device in the remainder of this specification. Blue text is used to highlight Register Control words “RWxx” and font in some tables for ease of readability throughout the document.

The purpose is to provide a standard for the DDR5CKD01(see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR5CKD01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Mechanical Outline

Package options include a 35 -ball Fine-Pitch BGA (BGA) with 0.50 mm/0.50 mm ball pitch, 11 x4 grid. The package has a number of depopulated balls. Package size is 2.3 mm x 5.8 mm as defined in MO-276 Issue R, Variation PBGA-B29[36]_10p50-R2p3x4p8Z#-C0p375Z#¹.

The device pin out supports outputs on the top and outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector and DIMM Standards.

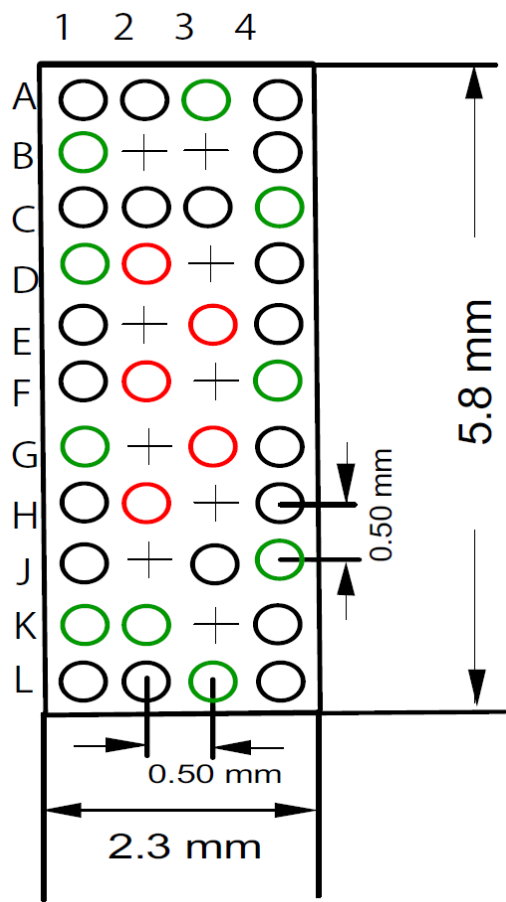


Figure 1 — Ball Configuration, TOP VIEW

Ball pitch: 0.50 mm x 0.50 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm)
X-ray view from topside

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5CKD01 must comply with a minimum thickness of 0.80 mm.

2.1 Pin Assignment

Table 1 specifies the pin assignment for the DDR5CKD01

Table 1 — Ball Assignment - TOP VIEW

	1	2	3	4	
A	DCK1_A_t	DCK1_A_c	VSS	DCK1_B_c	A
B	VSS			DCK1_B_t	B
C	Z _{QCAL}	SDA	SCL	VSS	C
D	VSS	VDDIO		QCK1_B_c	D
E	QCK1_A_c		VDD	QCK1_B_t	E
F	QCK1_A_t	VDD		VSS	F
G	VSS		VDD	QCK0_B_c	G
H	QCK0_A_c	VDD		QCK0_B_t	H
J	QCK0_A_t		DRST_N	VSS	J
K	VSS	VSS		DCK0_B_c	K
L	DCK0_A_t	DCK0_A_c	VSS	DCK0_B_t	L
	1	2	3	4	

2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description	# of Pins
Clock Inputs	DCK0_A_t/DCK0_A_c DCK0_B_t/DCK0_B_c DCK1_A_t/DCK1_A_c DCK1_B_t/DCK1_B_c	POD differential	Differential Controller clock input pair.	8
Reset Input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.	1
Outputs Clocks	QCK0_A_t/QCK0_A_c QCK1_A_t/QCK1_A_c QCK0_B_t/QCK0_B_c QCK1_B_t/QCK1_B_c	POD differential	Clock outputs to the DRAMs. Two copies per channel.	8
SidebandBus pins ¹	SDA	Open drain or push-pull I/O ^{2,3}	SidebandBus Data	1
	SCL	CMOS input ³	SidebandBus Clock	1
	V _{DDIO}	Power input	SidebandBus power input	1
Miscellaneous pins	V _{DD}	Power Input	Power supply voltage	4
	V _{SS}	Ground Input	Ground	10
	ZQCAL	Reference	Reference pin for driver calibration	1
Total Number of Pins				35
NOTE 1 SA pins are not required for DDR5CKD01 as the address will be determined by the ZQ Resistor value.				
NOTE 2 SDA driver operation is dynamic. Depending on the SidebandBus mode of operation I2C or I3C, and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.				
NOTE 3 These inputs are 0.9 to 2.1-V inputs.				

Clock Naming Convention:

Input Example:

DCKx_N - where 'x' is the input clock rank number, and 'N' is the sub-channel.

Output Example:

QCKy_N - where 'y' is the rank number, and 'N' is the sub-channel.

3 Description

The DDR5CKD01 is a registering clock driver used on DDR5 CUDIMMs, CSODIMMs, and CAMM. Its primary function is to buffer the DDR clock between the host controller and the DRAMs.

3.1 Logic Diagram Positive Logic

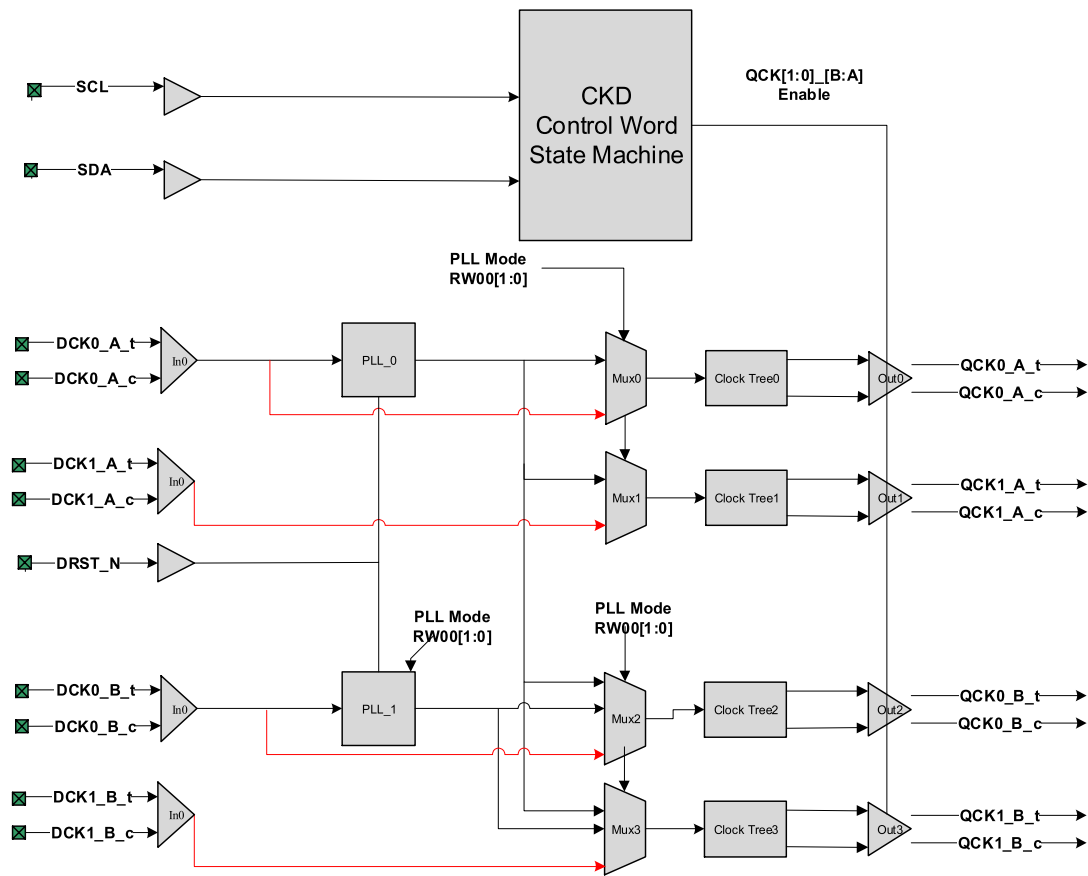


Figure 2 — Logic Diagram Positive Logic

4 Operation

4.1 CKD PLL Modes

The CKD has three clock driving modes, Single PLL Mode, PLL Bypass Mode (Legacy mode), and Dual PLL mode to generate the four output clock pairs QCK[1:0]_[B:A]_t/c.

The Host must write [RW00\[1:0\]](#) after V_{DD} has ramped and before driving any DCK clock pairs to configure the PLL mode when the device is in single or dual PLL mode.

In any of the PLL modes, the output clock frequency shall match that of the input clock in the frequency range of 1000 MHz to 4200 MHz.

Table 3 — Clock Mapping

RW00[1:0]	PLL Mode	PLL	Input Clock	Output Clock	Sub Channel
'00'b	PLL Bypass ^{1,2}	N/A	DCK0_A_t/c	QCK0_A_t/c	A
			DCK1_A_t/c	QCK1_A_t/c	
			DCK0_B_t/c	QCK0_B_t/c	B
			DCK1_B_t/c	QCK1_B_t/c	
'01'b	Single PLL ³	PLL_0	DCK0_A_t/c	QCK0_A_t/c	A
				QCK1_A_t/c	
				QCK0_B_t/c	B
				QCK1_B_t/c	
'10'b	Dual PLL ^{1,2,4}	PLL_0	DCK0_A_t/c	QCK0_A_t/c	A
				QCK1_A_t/c	
		PLL_1	DCK0_B_t/c	QCK0_B_t/c	B
				QCK1_B_t/c	

NOTE 1 When both DCK0_A and DCK0_B are toggling they cannot run at different frequencies.

NOTE 2 If one clock stops the other clock may continue to toggle within the normal frequency range.

NOTE 3 In Single PLL mode only PLL_0 is functional and PLL_1 is disabled to save power

NOTE 4 Both DCK0_A and DCK0_B must have a common reference clock and the SSC will be on the common reference clock. Due to the reference clock delay, the total DCK0_A and DCK0_B phase offset must be within t_{INCK_OFFSET}

4.1.1 PLL Bypass Mode

PLL Bypass mode normal operation is only supported for 990 MHz to 3000 MHz. Additionally, to support low speed ATE testing, PLL Bypass Mode will run below 990 MHz.

When [RW00\[1:0\] = '00'](#) PLL Bypass Mode is enabled, and the DCK[1:0]_[B:A]_t and DCK[1:0]_[B:A]_c are passed through to QCK[1:0]_[B:A]_t/c output clock pairs respectively. If only two output QCK pairs are required then QCK1_[B:A]_t/c can be disabled in [RW00](#) to save power.

The delay from DCK to QCK is $t_{staoff_PLL_BYP}$ with $t_{dynoff_PLL_BYP}$ as the dynamic variation. When Host adjusts the phase of a DCK input clock pair, the phase of the corresponding QCK output clock pairs will be adjusted with the same offset.

In this mode, the input clock termination (ICT) resistors on DCK[1:0]_[B:A]_t/c are all connected to V_{SS} with programmable values.

4.1.2 Single PLL Mode

When $RW00[1:0] = '01'$ the clock driver is in Single PLL Mode and the PLL_0 is enabled and the QCK[1:0]_[B:A]_t/c output clock pairs are re-generated by PLL_0 based on the DCK0_A_t/c input. PLL_1 is disabled. If only two QCK pairs are required, then QCK1_[B:A]_t/c can be disabled in $RW00$ to save power.

The delay from DCK0_A_t/c to QCK is t_{STAOFF} with t_{DYNOFF} as the dynamic variation. When Host adjusts the phase of the DCK0_A_t/c, the phase of all four QCK output pairs will be adjusted with the same offset.

In this mode, the input bus termination resistors on DCK0_A_t/c are all connected to V_{SS} with programmable values, and DCK1_A_t/c and DCK[1:0]_B_t/c are unused and terminated by the CKD ICT setting.

4.1.3 Dual PLL Mode

When $RW00[1:0] = '10'$ the clock driver is in Dual PLL Mode and both PLL_0 and PLL_1 are enabled. The QCK[1:0]_[A]_t/c output clock pairs are re-generated by the PLL_0 based on the DCK0_A_t/c input and The QCK[1:0]_[B]_t/c output clock pairs are re-generated by the PLL_1 based on the DCK0_B_t/c input. If only two QCK pairs are required, then QCK1_[B:A]_t/c can be disabled in $RW00$ to save power.

The delay from DCK_t/c to QCK is t_{staoft} with t_{dynoff} as the dynamic variation. When Host adjusts the phase of the DCK0_A_t/c, the phase of QCK_A output pairs will be adjusted with the same offset. When Host adjusts the phase of the DCK0_B_t/c, the phase of QCK_B output pairs will be adjusted with the same offset.

In this mode, the input bus termination resistors on DCK0_[B:A]_t/c are all connected to V_{SS} with programmable values, and DCK1_[B:A]_t/c are unused and terminated by the CKD ICT setting.

4.2 Device Initialization

To ensure defined outputs from the CKD before a stable clock has been supplied, the CKD must enter the reset state during power-up. The CKD powers up with all control words at their default state. After the voltage ramp, stable power is provided for a minimum of t_{INIT1} with DRST_n asserted. When the reset input DRST_n is LOW, all input receivers are disabled. As long as the DRST_n input is pulled LOW, the CKD is in low power state and input termination is still enabled.

When DRST_n goes HIGH, the CKD will become operational after t_{CKDOP} regardless if input clock is toggling or not. After t_{STAB} , the device is in normal operating condition for Single and Dual PLL modes. When in PLL Bypass mode, the device will be in normal operation after the last $t_{staoft_PLL_BYP}$ is met.

After initialization, the Host must write to those control registers whose contents are required for the DIMM operation.

The DDR5CKD01 device will not affect DRST_n signal voltage levels even when V_{DD} is not powered on. A CKD with V_{DD} powered off shall not prevent other devices connected to the same DRST_n net from receiving the correct HIGH and LOW logic voltage levels driven by the host on that net. Also, the CKD device will not sustain permanent damage if DRST_n is driven HIGH (to V_{IH} levels) when V_{DD} is powered off, and it must be able to support all the specified features and functions once power is restored.

4.2.1 PLL Bypass Mode Initialization Sequence in PLL Bypass Mode

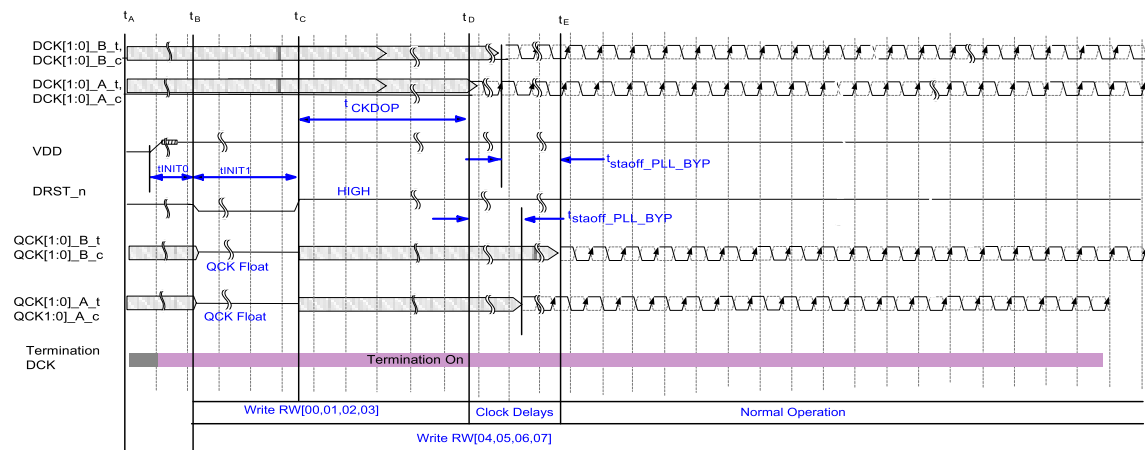


Figure 3 — Timing of Clock During Initialization Sequence in PLL Bypass Mode

- NOTE 1 The host may write **RW00[1:0]** to enable PLL Bypass mode prior to any DCK toggling.
- NOTE 2 If the host writes **RW00** control word it must do so first before any other configuration control words to ensure device is properly configured.
- NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if any required DCK is toggling or not.
- NOTE 4 QCK may toggle during t_{CKDOP} if any required DCK is toggling.
- NOTE 5 In the diagram DCK[1:0]_A starts before DCK[1:0]_B, but either clock may start toggling first.

4.2.2 Single PLL Mode Initialization Sequence

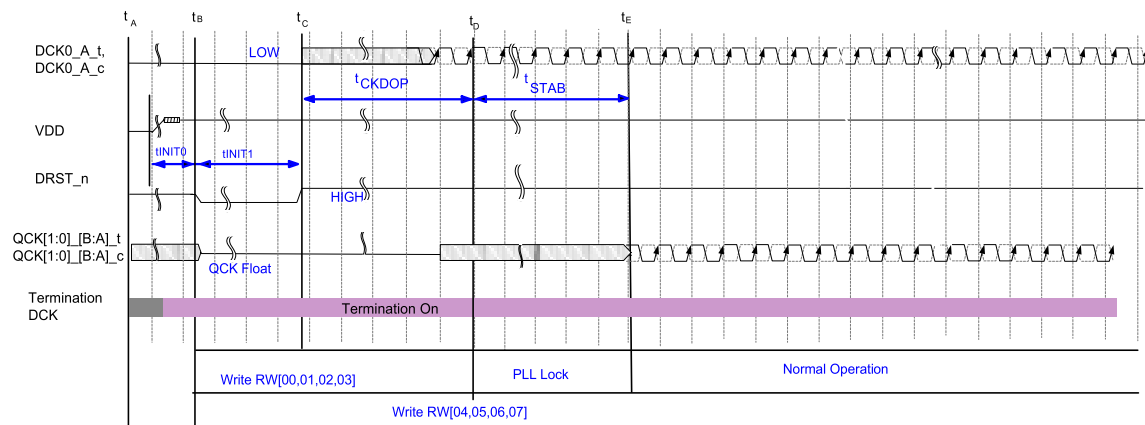


Figure 4 — Timing of Clock During Initialization Sequence in Single PLL Mode

- NOTE 1 The host must write **RW00[1:0]** to enable Single PLL mode prior to DCK0_A toggling.
- NOTE 2 The host must write **RW00** before any other configuration control words.
- NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_A is toggling.
- NOTE 4 QCK may toggle during t_{CKDOP} if DCK0_A is toggling.
- NOTE 5 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.
- NOTE 6 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.2.3 Dual PLL Mode Initialization Sequence

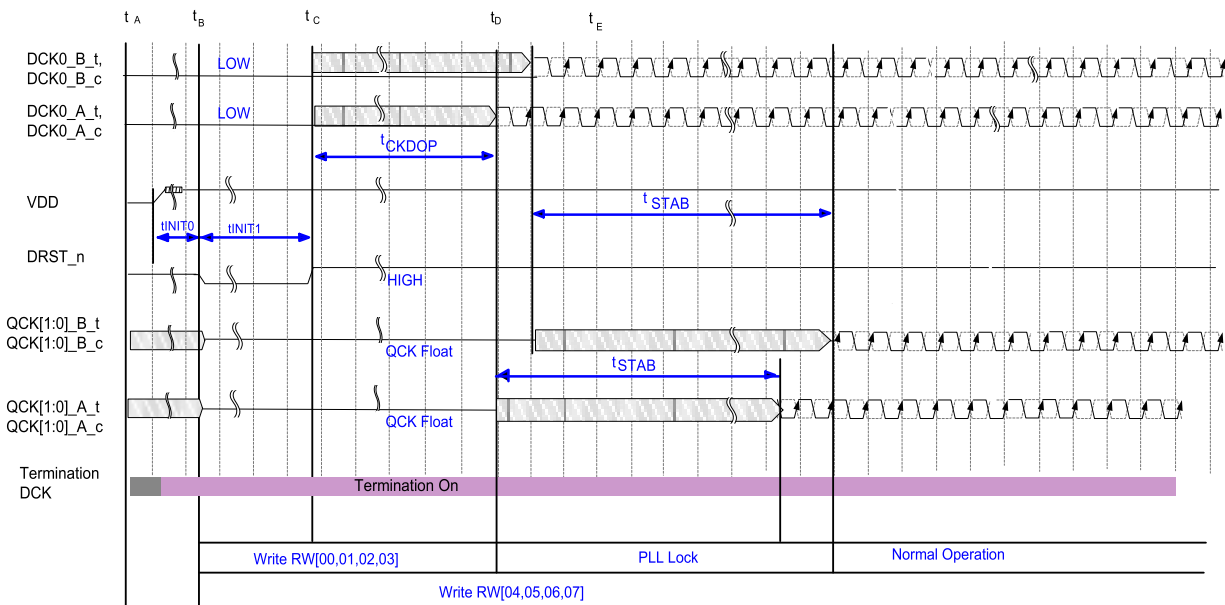


Figure 5 — Timing of Clock During Initialization Sequence in Dual PLL Mode

- NOTE 1 The host must write **RW00[1:0]** to enable Dual PLL mode prior to DCK0_[B:A] toggling.
- NOTE 2 The host must write **RW00** before any other configuration control words.
- NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_[B:A] is toggling.
- NOTE 4 QCK may toggle during t_{CKDOP} if DCK0_[B:A] is toggling.
- NOTE 5 The output clocks must be stable by the next DCK0_[B:A] rising edge after t_{STAB} max.
- NOTE 6 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.
- NOTE 7 In the diagram DCK0_A starts before DCK0_B, but either clock may start toggling first.

4.3 Reset Initialization with Stable Power

Applies to the situation when there is a soft reset in the system. All Control words are sticky cleared by power cycle not Reset.

4.3.1 PLL Bypass Mode Reset Initialization with Stable Power

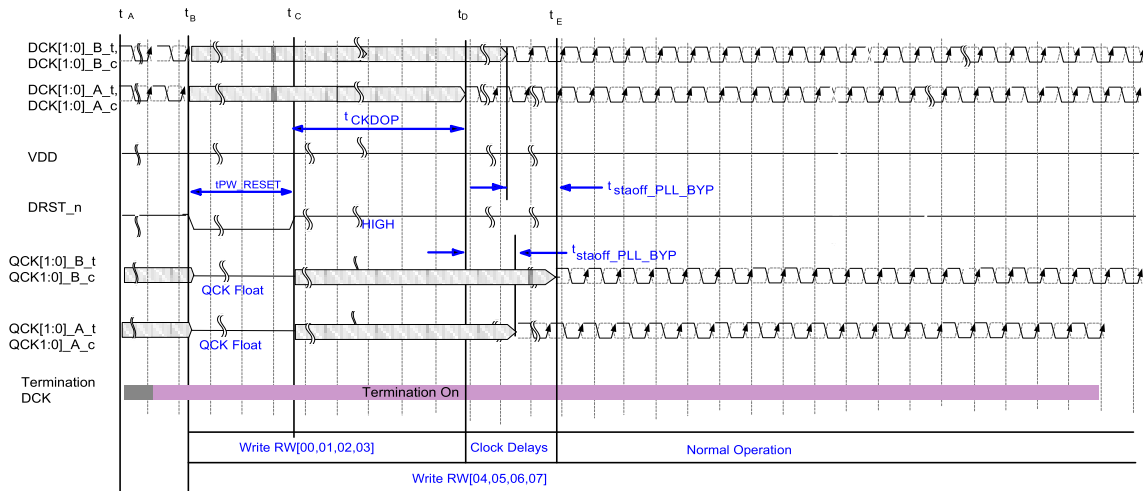


Figure 6 — Reset Initialization With Stable Power in PLL Bypass Mode.

NOTE 1 The CKD will not be operational until after t_{CKDOP} regardless if any required DCK is toggling.

NOTE 2 QCK may toggle during t_{CKDOP} if any required DCK is toggling.

NOTE 3 In the diagram DCK[1:0]_A start before DCK[1:0]_B, but any DCK clock pair may start toggling first.

4.3.2 Single PLL Mode Reset Initialization with Stable Power

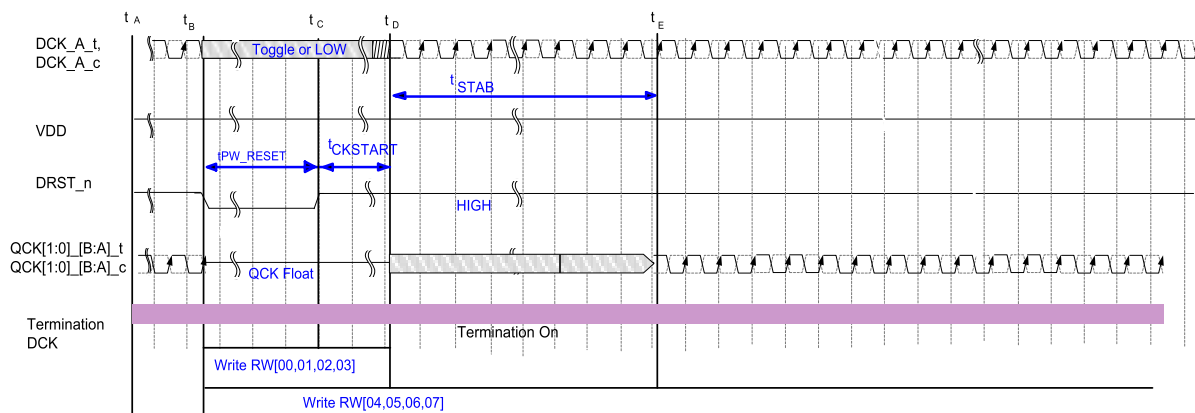


Figure 7 — Reset Initialization with Stable Power in Single PLL Mode

NOTE 1 If DCK is toggling QCK can start to toggle after DRST_n is de-asserted.

NOTE 2 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_A is toggling.

NOTE 3 QCK may toggle during t_{CKDOP} if DCK0_A is toggling.

NOTE 4 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.

NOTE 5 During t_{STAB} while the PLL is locking, QCK output states are "Don't Care".

4.3.3 Dual PLL Mode Reset Initialization with Stable Power

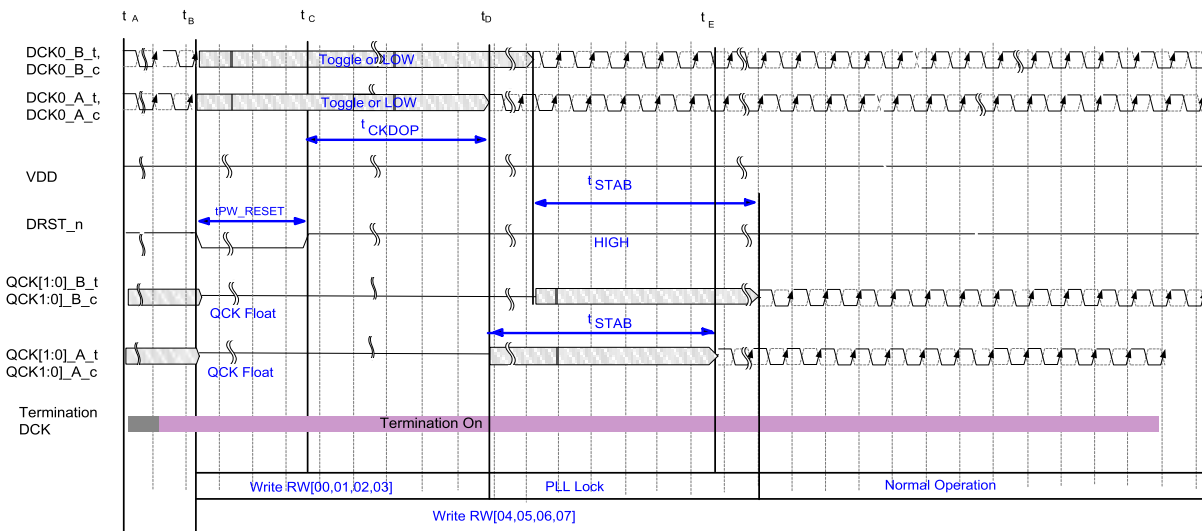


Figure 8 — Reset Initialization With Stable Power in Dual PLL Mode.

- NOTE 1 If DCK0_[B:A] is toggling QCK can start to toggle after DRST_n is de-asserted.
- NOTE 2 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_[B:A] is toggling.
- NOTE 3 QCK may toggle during t_{CKDOP} if DCK0_[B:A] are toggling.
- NOTE 4 The output clocks must be stable by the next DCK0_[B:A] rising edge after t_{STAB} max.
- NOTE 5 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.
- NOTE 6 In the diagram DCK0_A starts before DCK0_B, but either clock may start toggling first.

4.4 Clock Stop Operation

To support S3 Power Management mode or any other operation that allows output clocks to float, the CKD supports a Clock Stopped power down mode for Single and Dual PLL Modes. When inputs DCK_t and DCK_c are being held LOW for at least t_{DLOW} Min the device stops PLL operation and enters low-power static standby operation but Sideband Bus must be operational.

4.4.1 PLL Bypass Mode Clock Stopped Event

When the CKD is in PLL Bypass mode, it will remain in high powered state during clock stop event.

Note: Each Clock path works independently, input to corresponding output.

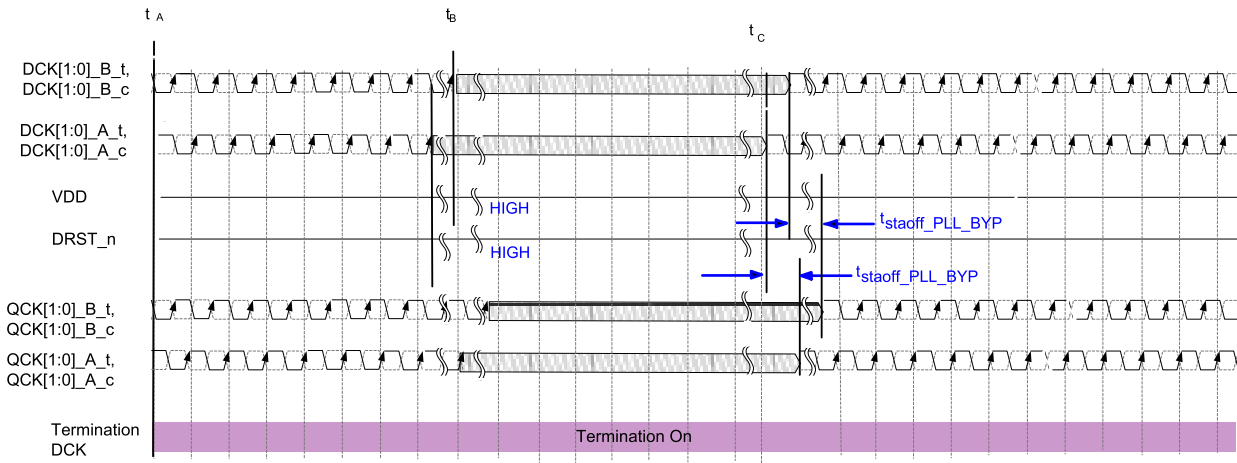


Figure 9 — PLL Bypass Mode during Clock Stop Event

4.4.2 Single PLL Mode Clock Stop Power Down

To enter Clock Stopped Power Down mode the host will stop driving (float) DCK0_A_t and DCK0_A_c. Since DCK is ODT terminated to V_{SS} the CKD receiver will see both DCK0_A_t and DCK0_A_c at a logic LOW below $V_{ILStatic_DC}$. This condition should be interpreted as clock stop power-down mode. To avoid clock glitches during clock power down, the V_{SS} termination on DCK_t/ DCK_c signals will pull the input clock signals below $V_{ILStatic}$ threshold. The CKD is now in Clock Stopped Power Down mode. The DCK0_A_t and DCK0_A_c remain active input circuits which are required to detect the wake up request from the host.

To Exit clock stop power down, a frequency and phase accurate input clock signal must be applied. The output clocks must be stable by the next DCK0 rising edge after t_{STAB} max.

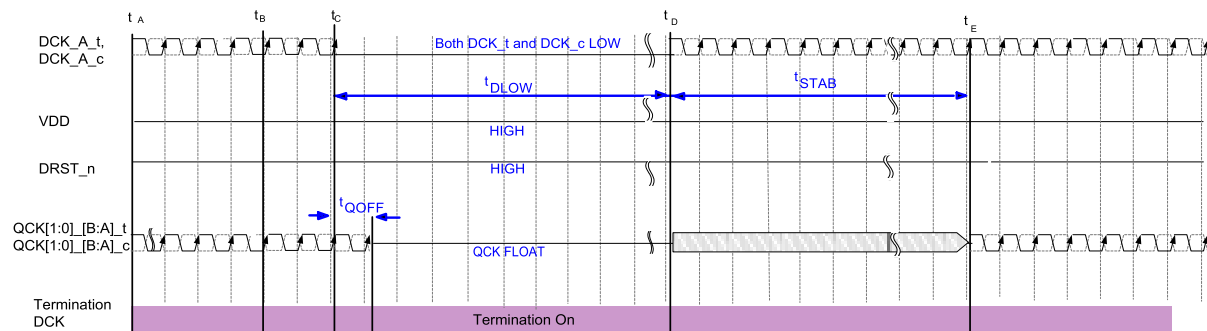


Figure 10 — Single PLL Mode Clock Stop Power Down

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

NOTE 2 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.

4.4.3 Dual PLL Mode Clock Stop Power Down

To enter CKD Clock Stopped Power Down mode, the host will stop driving (float) DCK0_[B:A]_t and DCK0_[B:A]_c. Since DCK is ODT terminated to V_{SS} the CKD receiver will see both input clock pairs DCK0_[B:A]_t and DCK0_[B:A]_c at a logic LOW. This condition should be interpreted as clock stop power-down mode. To avoid clock glitches during clock power down, the V_{SS} termination on DCK0_[B:A]_t/ DCK0_[B:A]_c signals will pull the input clock signals below $V_{ILStatic}$ threshold. The CKD is now in Clock Stopped Power Down mode. The DCK0_[B:A]_t and DCK0_[B:A]_c remain active input circuits which are required to detect the wake up request from the host.

To Exit clock stop power down wake up the CKD after entering Clock Stopped Power Down, a frequency and phase accurate input clock signal must be applied to either DCK0_A or DCK0_B. The output clocks must be stable by the next DCK rising edge after t_{STAB} max.

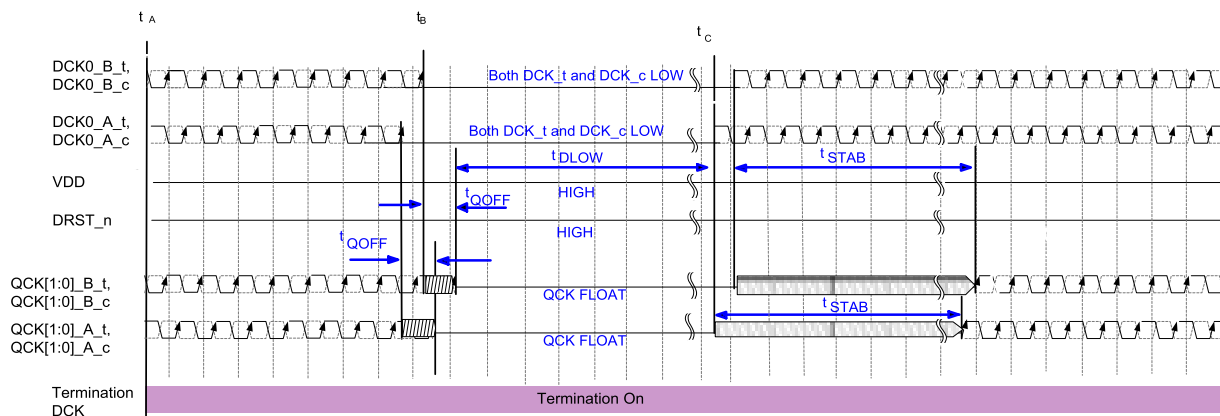


Figure 11 — Dual PLL Mode Clock Stop Power Down

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.5 Frequency Change

4.5.1 PLL Bypass Mode Frequency Change

The host can change input frequency if desired after a Clock Stop event. Once the host changes the frequency on the input DCK clocks the CKD will be required to drive stable output QCK clocks within $t_{\text{staoff_PLL_BYP}}$.

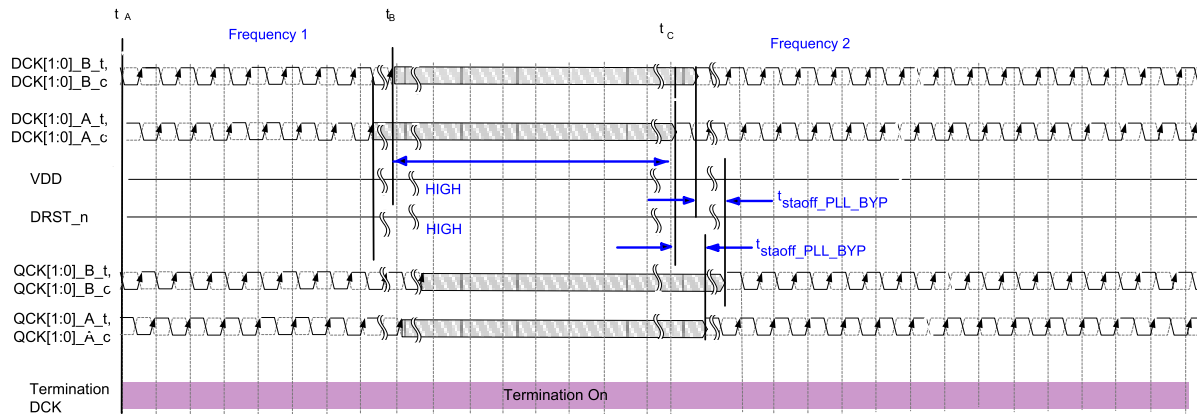


Figure 12 — Stabilization Time for Frequency Change for PLL Bypass Mode

4.5.2 Single PLL Mode Frequency Change

The host can change input frequency if desired after a Clock Stop Power Down event. Once the host changes the frequency on the incoming DCK clock, the CKD will re-lock to new frequency and will be required to drive a stable output clocks QCK within t_{STAB} .

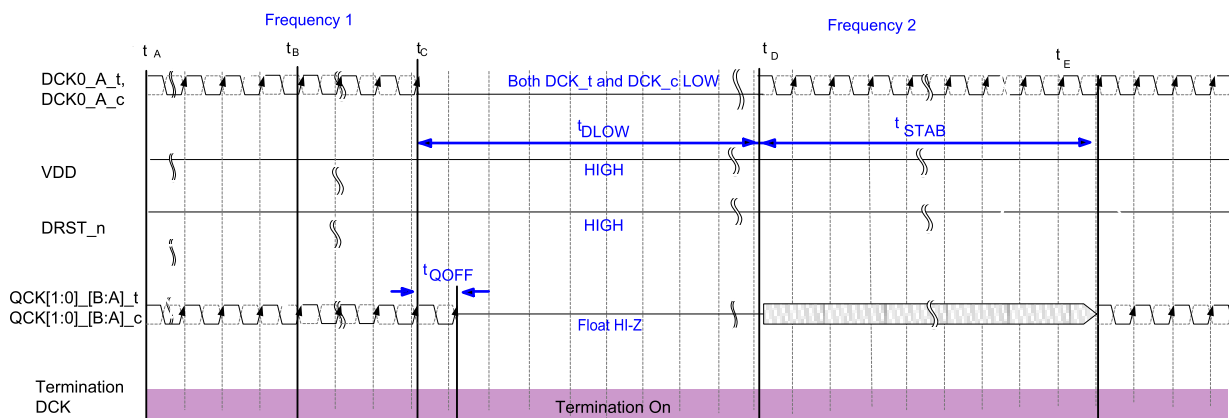


Figure 13 — Stabilization Time for Frequency Change for Single PLL Mode

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.5.3 Dual PLL Mode Frequency Change

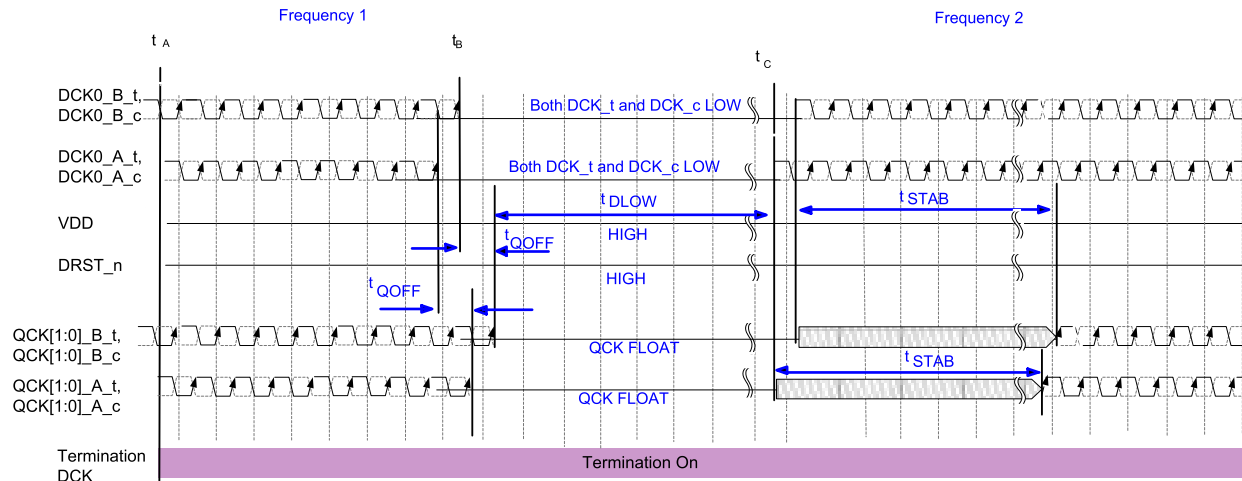


Figure 14 — Stabilization Time for Frequency Change for Dual PLL Mode

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.6 ZQ Calibration

ZQ Calibration calibrates the output driver and input termination impedance across process, temperature, and voltage. Since the CKD will not receive the ZQcal or ZQlatch commands the device will need to self-calibrate in the background while the clocks are continuously running. All specifications must be met during ZQCAL.

To use the ZQ calibration function, a $240\ \Omega$ or $480\ \Omega \pm 1\%$ tolerance external resistor must be connected between the ZQ pin and V_{SS} . For more details see Section 12.2.1, “Serial Address of CKD Device,”

4.7 Manufacturing ID

RW40 ~ RW4E are Read only control words in the DDR5CKD01 contain detailed CKD manufacturing information provided by CKD vendor. This information is programmed in OTP. The purpose is for improved manufacturing logistics management and not meant to be used by host platform to control normal operation. These registers must be accessible during run time.

4.8 Sideband

For all configuration registers, the DDR5CKD01 supports register control word access mechanisms through Sideband Bus Channel commands. The configuration registers are accessible to be written or read by software from the Sideband Bus host at any time the CKD is powered on, independent of input clock or reset. Details in Chapter 12, “Sideband Interface,”.

5 Control Words

The DDR5CKD01 device features a set of 8-bit control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle.

CKD Control Word attributes can be:

- Reserved¹
- Read Only
- Write Only
- RD/WR
- One Time Programmable
- Sticky - Cleared by power cycle not Reset

5.1 Control Word Decoding

The power-on default state of all control words is ‘0’ unless specified otherwise. **All Control words are sticky cleared by power cycle not DRST_n.** Cycling the device in and out of low-power mode will not alter the control word settings.

Table 4 — CKD Control Word Space

Address	Size (bytes)	Space	Description
00h to 5Fh	96	JEDEC	96 addressed registers
60h to FFh	160	Vendor Specific	160 addressed registers

1. Reserved control bits may not be physically implemented and they shall be written to zero to ensure forward compatibility.

5.1.1 Control Word Decoding

Table 5 — Control Word Decoding

Register Control Word	MRA [7:0] HEX	Meaning
RW00	0x00	Configuration
RW01	0x01	Output Delay Control Enable
RW02	0x02	QCK Signals Driver Characteristics
RW03	0x03	QCK Output Differential Slew Rate
RW04	0x04	Output Delay Range for QCK0_A_t and QCK0_A_c
RW05	0x05	Output Delay Range for QCK1_A_t and QCK1_A_c
RW06	0x06	Output Delay Range for QCK0_B_t and QCK0_B_c
RW07	0x07	Output Delay Range for QCK1_B_t and QCK1_B_c
RW08	0x08	Reserved
RW09 -RW27	0x09 - 0x27	Reserved
RW28	0x28	I ² C and I ³ C Basic Error Status
RW29	0x29	I ² C and I ³ C Basic Clear Error Status
RW2A-RW3F	0x2A-0x3F	Reserved
RW40	0x40	Date Code Byte 0
RW41	0x41	Date Code Byte 1
RW42	0x42	Date Code Byte 2
RW43	0x43	Vendor Specific Unique Unit Code Byte 0
RW44	0x44	Vendor Specific Unique Unit Code Byte 1
RW45	0x45	Vendor Specific Unique Unit Code Byte 2
RW46	0x46	Vendor Specific Unique Unit Code Byte 3
RW47	0x47	Vendor Specific Unique Unit Code Byte 4
RW48	0x48	Vendor Specific Unique Unit Code Byte 5
RW49	0x49	Vendor Specific Unique Unit Code Byte 6
RW4A	0x4A	Vendor ID Byte 0
RW4B	0x4B	Vendor ID Byte 1
RW4C	0x4C	Device ID Byte 0
RW4D	0x4D	Device ID Byte 1
RW4E	0x4E	Vendor Revision ID
RW4F~RW5F	0x4F~0x5F	Reserved

Control Word Naming Convention:

RWyy[z:z]
 yy = RW Number
 z = OP

5.2 Configuration Control Word

5.2.1 RW00 - CKD Configuration Control Word

Table 6 — RW00: CKD Configuration Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	PLL Mode	Bypass Mode (default)
x	x	x	x	x	x	0	1		Single PLL mode ¹
x	x	x	x	x	x	1	0		Dual PLL mode
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	ICT Input Clock Termination Settings	80 Ω (default)
x	x	x	x	0	1	x	x		60 Ω
x	x	x	x	1	0	x	x		120 Ω
x	x	x	x	1	1	x	x		Disabled ²
x	x	x	0	x	x	x	x	CHA	QCK0_A_t/QCK0_A_c clock enabled
x	x	x	1	x	x	x	x	Disable QCK0_A_t/QCK0_A_c clock ³	QCK0_A_t/QCK0_A_c clock disabled
x	x	0	x	x	x	x	x	CHA	QCK1_A_t/QCK1_A_c clock enabled
x	x	1	x	x	x	x	x	Disable QCK1_A_t/QCK1_A_c clock ³	QCK1_A_t/QCK1_A_c clock disabled
x	0	x	x	x	x	x	x	CHB	QCK0_B_t/QCK0_B_c clock enabled
x	1	x	x	x	x	x	x	Disable QCK0_B_t/QCK0_B_c clock ³	QCK0_B_t/QCK0_B_c clock disabled
0	x	x	x	x	x	x	x	CHB	QCK1_B_t/QCK1_B_c clock enabled
1	x	x	x	x	x	x	x	Disable QCK1_B_t/QCK1_B_c clock ³	QCK1_B_t/QCK1_B_c clock disabled
NOTE 1 Only PLL0 is functional and PLL_1 is disabled to save power.									
NOTE 2 This is for Testing purpose only.									
NOTE 3 Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. In PLL mode, the PLL remains locked on DCK0_t/DCK0_c unless the system stops the clock inputs to the DDR5CKD01 to enter the lowest power mode.									

5.3 QCK Output Register Control Words

5.3.1 RW01- Output Delay Control Enable Control Word

Table 7 — RW01: Output Delay Control Enable Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	CHA	Disabled (zero delay)
x	x	x	x	x	x	x	1	QCK0_A_t/QCK0_A_c Output Delay	Enabled ¹
x	x	x	x	x	x	0	x	CHA	Disabled (zero delay)
x	x	x	x	x	x	1	x	QCK1_A_t/QCK1_A_c Output Delay	Enabled ²
x	x	x	x	x	0	x	x	CHB	Disabled (zero delay)
x	x	x	x	x	1	x	x	QCK0_B_t/QCK0_B_c Output Delay	Enabled ³
x	x	x	x	0	x	x	x	CHB	Disabled (zero delay)
x	x	x	x	1	x	x	x	QCK1_B_t/QCK1_B_c Output Delay	Enabled ⁴
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x	Reserved	Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 Only valid for PLL Mode, enabled output delay feature range defined in [RW04](#)

NOTE 2 Only valid for PLL Mode, enabled output delay feature range defined in [RW05](#)

NOTE 3 Only valid for PLL Mode, enabled output delay feature range defined in [RW06](#)

NOTE 4 Only valid for PLL Mode, enabled output delay feature range defined in [RW07](#)

For details on CKD output driver strengths in this section, see Table 46, “Output Ron Drive,”.

5.3.2 RW02 - QCK Signals Driver Characteristics Control Word

Table 8 — RW02: QCK Signals Driver Characteristics Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	CHA	Light Drive (Default)
x	x	x	x	x	x	0	1	QCK0_A_t/QCK0_A_c	Moderate Drive
x	x	x	x	x	x	1	0		Strong Drive
x	x	x	x	x	x	1	1		Weak Drive
x	x	x	x	0	0	x	x	CHA	Light Drive (Default)
x	x	x	x	0	1	x	x	QCK1_A_t/QCK1_A_c	Moderate Drive
x	x	x	x	1	0	x	x		Strong Drive
x	x	x	x	1	1	x	x		Weak Drive
x	x	0	0	x	x	x	x	CHB	Light Drive (Default)
x	x	0	1	x	x	x	x	QCK0_B_t/QCK0_B_c	Moderate Drive
x	x	1	0	x	x	x	x		Strong Drive
x	x	1	1	x	x	x	x		Weak Drive
0	0	x	x	x	x	x	x	CHB	Light Drive (Default)
0	1	x	x	x	x	x	x	QCK1_B_t/QCK1_B_c	Moderate Drive
1	0	x	x	x	x	x	x		Strong Drive
1	1	x	x	x	x	x	x		Weak Drive

5.3.3 RW03 - QCK Output Differential Slew Rate Control Word

The CKD will support output slew rate control per channel, as described in the following control word.

Table 9 — RW03 - QCK Output Differential Slew Rate Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	CHA	Moderate
x	x	x	x	x	x	0	1	QCK [1:0]_A	Fast
x	x	x	x	x	x	1	0	Differential Slew Rate Setting ¹	Reserved
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	Reserved	Reserved
x	x	x	x	0	1	x	x		Reserved
x	x	x	x	1	0	x	x		Reserved
x	x	x	x	1	1	x	x		Reserved
x	x	0	0	x	x	x	x	CHB	Moderate
x	x	0	1	x	x	x	x	QCK [1:0]_B	Fast
x	x	1	0	x	x	x	x	Differential Slew Rate Setting ¹	Reserved
x	x	1	1	x	x	x	x		Reserved
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

NOTE 1 Slew Rate Control encodings of Moderate, and Fast apply to all driver strength settings. The base range values specified in Table 44 are applicable for only Ron = Strong Drive, V_{DD} = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test.