

JEDEC STANDARD

Definition of the SSTV32852 2.5-V 24-Bit to 48-Bit SSTL_2 Registered Buffer for 1U Stacked DDR DIMM Applications

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STANDARD FOR DEFINITION OF THE SSTV32852 2.5-V AND SSTVA32852 2.6-V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFERS FOR STACKED DDR DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-68, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the 32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications.

The purpose is to provide a standard for the 32852 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation 32852 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 24-bit to 48-bit registered buffer specification covers two speed grades; the faster speed grade SSTVA is backward compatible with the slower speed grade SSTV. These devices are collectively referred to as “32852” when it applies to both speed grades. These devices are intended to support the following applications:

Table 1 — 32852 Devices

Application	VDD/VDDQ Supply Voltage	32852 Part Number
PC1600 PC2100 PC2700	2.5 V $\pm$ 0.2 V	SSTV32852 or SSTVA32852
PC3200	2.6 V $\pm$ 0.1 V	SSTVA32852

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The 32852 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and

2 Device Standard (cont'd)

$\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain low.

Package options include 114 pin Low-Profile Fine Pitch BGA (LFBGA) (19 x 6 array, 16.00 x 5.50 mm body size, 0.80 mm pitch, MO-205, Variation DC).

2.2 Pinout Figure

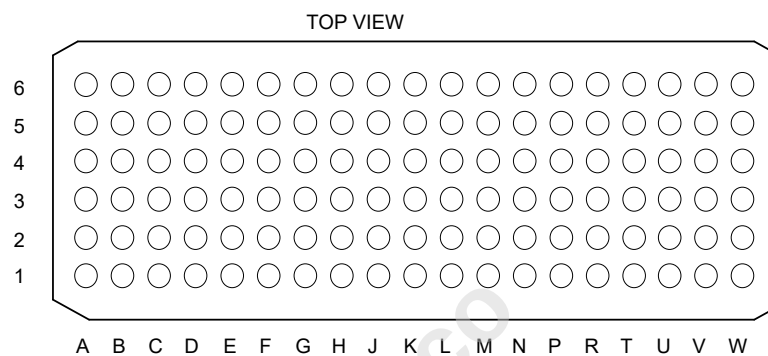


Figure 1 — 114-ball BGA Package Top View

6	Q2B	Q3B	Q5B	Q7B	Q8B	Q10B	Q12B	Q13B	Q14B	Q17B	Q18B	Q20B	Q22B	Q23B	Q24B	D14	D16	D17	D20
5	Q1B	V _{DDQ}	Q4B	Q6B	GND	Q9B	Q11B	V _{DD}	Q15B	Q16B	Q19B	V _{DDQ}	Q21B	V _{DDQ}	V _{DD}	D13	D15	D19	D21
4	$\overline{CK}$	GND	V _{DDQ}	GND	V _{DDQ}	V _{DDQ}	GND	V _{DDQ}	GND	V _{DDQ}	GND	GND	V _{DDQ}	GND	V _{REF}	D18	D22	D23	D24
3	CK	GND	V _{DDQ}	GND	V _{DDQ}	V _{DDQ}	GND	V _{DDQ}	GND	V _{DDQ}	GND	GND	V _{DDQ}	GND	RESET	D6	D10	D11	D12
2	Q1A	V _{DDQ}	Q4A	Q6A	GND	Q9A	Q11A	V _{DD}	Q15A	Q16A	Q19A	V _{DDQ}	Q21A	V _{DDQ}	V _{DD}	D1	D3	D7	D9
1	Q2A	Q3A	Q5A	Q7A	Q8A	Q10A	Q12A	Q13A	Q14A	Q17A	Q18A	Q20A	Q22A	Q23A	Q24A	D2	D4	D5	D8
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

Figure 2 — Pinout