

JEDEC STANDARD

Definition of the SSTU32864 1.8-V Configurable Registered Buffer for DDR2 RDIMM Applications

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-78, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTU32864 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTU32864 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32864 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RESET}$ and Cn inputs must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

2 Device Standard (cont'd)

2.1 Description (cont'd)

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTU32864 must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and will force the outputs low. If the $\overline{\text{DCS}}$ -control functionality is not desired, then the $\overline{\text{CSR}}$ input can be hardwired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs.

Package options include 96-ball Low Profile Fine Pitch BGA (LFBGA) (16 x 6 Array, 13.50 x 5.50 mm body size, 0.80 mm pitch, MO-205, Variation CC).

2.2 96-ball LFBGA (MO-205CC)

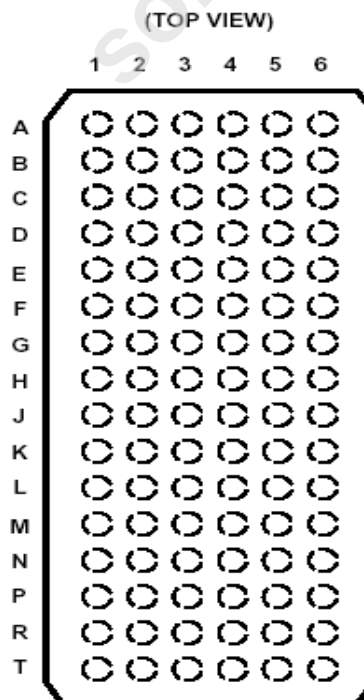


Figure 1 — Pinout Configuration

2.3 Pinout Top View for 96-ball LFBGA

NC denotes a no-connect (ball present but not connected to the die). DNU denotes a do-not-use pin (ball connected to the die but should be left open-circuit).

A	DCKE	NC	V _{REF}	V _{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{DD}	V _{DD}	Q3	Q16
D	DODT	NC	GND	GND	QODT	DNU
E	D5	D17	V _{DD}	V _{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{DD}	V _{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{DD}	V _{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{DD}	V _{DD}	Q13	Q24
T	D14	D25	V _{REF}	V _{DD}	Q14	Q25
	1	2	3	4	5	6

Figure 2 — 1:1 Register (C0=0, C1=0)

A	DCKE	NC	V _{REF}	V _{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	DODT	NC	GND	GND	QODTA	QODTB
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCSA}}$	$\overline{\text{QCSB}}$
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{DD}	V _{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{DD}	Q14A	Q14B
	1	2	3	4	5	6

Figure 3 — 1:2 Register A (C0=0, C1=1)