

JEDEC STANDARD

JEDEC Dictionary of Terms for Solid-State Technology — 6th Edition

JESD88E

(Revision of JESD88D, December 2009)

JUNE 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by
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3103 North 10th Street
Suite 240 South
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Foreword

This dictionary was originally prepared and edited by a special Working Group consisting of JEDEC consultants Fred A. Mann and Frank S. Stein, under the direction of the JEDEC Board of Directors, and is periodically updated by JEDEC Committee JC-10 on Terms, Definitions, and Symbols. After the 1st edition, regular contribution has been made by David Sweetman. Publication of the JEDEC Dictionary was approved by the JEDEC Board of Directors under Ballot JCB-00-97.

This Sixth Edition includes definitions from 14 standards that were not included in the Fifth Edition plus revised definitions from 26 additional publications and standards that have been updated. All reported errors and necessary rewording have been taken into account.

Introduction

As new or revised JEDEC and EIA publications* are issued, their definitions are considered for inclusion in this dictionary. All publications with definitions in this edition of the dictionary are listed in Annex A. The following are often not included: (1) terms having a specialized meaning only within the context of a particular publication (usually a test method), e.g., “brush: A toothbrush with a handle made up of nonreactive material ...”; and (2) concepts where the publication gives only a symbol and a term but no definition. This dictionary, like any dictionary, is primarily intended to define concepts. For an extensive list of symbols and abbreviations with the corresponding terms for many variations (dc, peak, rms, small signal, large signal, etc.), see JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices*.

All entries are reviewed for punctuation, grammar, and clarity, as well as for accuracy, and reworded if such is considered warranted. If a definition is substantially recast, the date of the source publication is followed by a pound sign (#). The editors have made every effort to ensure that the *intent* of the original definition is retained in all cases. When the same term is defined in more than one source publication in substantially different words having essentially equivalent meanings, the formulation is selected that, in the opinion of the editors, is the most completely and clearly stated, and the pound sign is applied to the references to the other publications. If the same term is defined with different meanings in two or more publications, all forms are given in alphanumeric order by publication reference. The definitions are numbered (1), (2), ... , but no order of preference is intended.

While most of the conventions used in this dictionary are self-explanatory, two may need further explanation: (1) Terms separated by semicolons (;) are synonyms. (2) Square brackets [] enclosing a part of a term and possibly parts of its definition indicate that the words placed between them may replace all or some of the preceding words. Selection of the bracketed part of the term requires the selection of the bracketed parts of the definition. This convention is used to show at first sight the construction of terms having parallel definitions.

* As used in this dictionary, the word “publication” is a generic term that includes standards.

Scope

Each term and definition in this dictionary has been included strictly for application within the solid-state industry. Many of the terms and definitions in this dictionary may have applicability beyond the scope of the JEDEC Solid State Technology Association; however, an assumption of such extended applicability is the responsibility of the user. The goal is to include the appropriate terms and definitions from all JEDEC publications and standards. At the present time, only terms and definitions from the publications listed in Annex A are included.

JEDEC DICTIONARY OF TERMS FOR SOLID-STATE TECHNOLOGY

Terms, abbreviations, letter symbols, and definitions

References

A

A: See “port A; port B”.

A; a: See “anode terminal”.

abbreviation: A shortened form of a word or expression.

JESD77D, 8/12
JESD99C, 12/12

ABD: See “avalanche breakdown diode”.

ABD array: A device having three or more terminals and containing multiple diodes within a single package, with at least one of the diodes being an ABD.

JESD77D, 8/12
JESD210, 12/07

NOTE ABD arrays can be classified as 1) devices with multiple discrete semiconductor chips; and 2) devices with multiple diode junctions diffused into a single semiconductor chip.

above-passivation layer (APL): A low-impedance metal plane, built on the surface of a die above the passivation layer, that connects a group of bumps or pins (typically power or ground).

JS-001-2012, 4/12

NOTE This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

absolute accuracy error: Synonym for “total error”.

JESD99C, 12/12

absolute maximum rated junction temperature: The maximum junction temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

JESD22-A108D, 11/10#

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated temperature: The maximum junction or ambient temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur.

JESD89-1A, 10/07
JESD89-3A, 11/07

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated voltage: The maximum voltage that may be applied to a device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

JESD22-A108D, 11/10#
JESD89-1A, 10/07#
JESD89-2A, 10/07#
JESD89-3A, 11/07#

absolute maximum rating: Synonym for “maximum rating”.

JESD77D, 8/12

ABTXXXXXX series: A BiCMOS series that includes devices whose input logic levels are TTL-compatible and whose outputs are specified at TTL levels.

JESD54, 2/96

accelerated ELF test time (t_A): The duration of the accelerated ELF test.

JESD74A, 2/07

accelerated equivalent soak: A soak at a higher temperature for a shorter time (compared to the standard soak) to provide roughly the same amount of moisture absorption.

J-STD-020D.1, 3/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

accelerated soft error rate (ASER): A soft error rate in the presence of an intense ionizing radiation source.

JESD89, 8/01

acceleration factor (A, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

JEP122G, 10/11
JEP143C, 7/12
JESD74A, 2/07#
JESD85, 7/01#
JESD91A, 8/01#
JESD94A, 7/08

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used in place of the symbol A.

acceleration factor, stress (A_s): The acceleration factor due to the presence of some stress (e.g., current density, electric field, humidity, temperature cycling).

JEP122G, 10/11
JEP143C, 7/12

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

JEP122G, 10/11
JEP143C, 7/12
JESD74A, 2/07#

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

where

E_{aa} is the apparent activation energy (eV);
 k is Boltzmann's constant (8.62×10^{-5} eV/K);
 T_1 is the absolute temperature of test 1 (K);
 T_2 is the absolute temperature of test 2 (K);
 λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
 λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electronvolts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s , λ_o is the observed failure rate at some test temperature T_t , and A_T is the temperature acceleration factor from T_t to T_s .

acceleration factor, voltage (A_v): The acceleration factor due to changes in voltage.

JEP143C, 7/12
JESD74A, 2/07

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

acceleration model: A mathematical formulation of the relationship between (1) the rate (speed) of a degradation mechanism or the time-to-failure and (2) the conditions or stresses that caused the degradation.

JEP143C, 7/12
JEP148A, 12/08

acceptance inspection: A sampling inspection or series of sampling inspections used to determine the suitability of a lot of material for shipment.

JESD16-A, 4/95

accept number: The maximum number of nonconforming components in the sample for which acceptance of the lot is allowed under the sampling plan.

JESD16-A, 4/95

access time: The time interval between the application of a specific input pulse and the availability of valid signals at an output.

JESD100-B, 12/99

ac controller: A circuit that produces, from an ac input, an ac output that is proportional to a control input.

JESD14, 11/86#

accumulator: A register in which one operand of an operation can be stored and subsequently replaced by the result of another operation. (Ref. IEC 824.)

JESD100-B, 12/99

accuracy: The difference between the sample estimate and the population parameter being estimated.

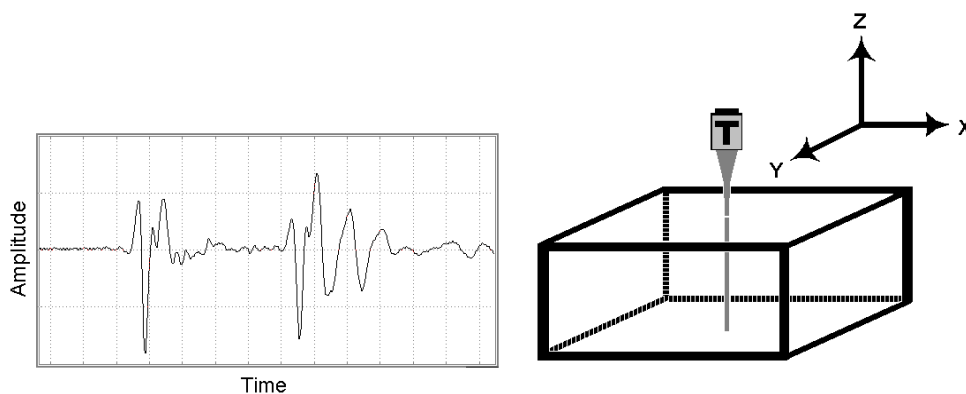
EIA-557-B, 2/06
JEP132, 7/98

ac noise margin: The maximum transient or pulse voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level.

RS-390-A, 2/81

acoustic data, A-mode: Acoustic data collected at the smallest X-Y-Z region defined by the limitations of the given acoustic microscope. An A-mode display contains amplitude and phase/polarity information as a function of time of flight at a single point in the X-Y plane.

J-STD-035, 5/99

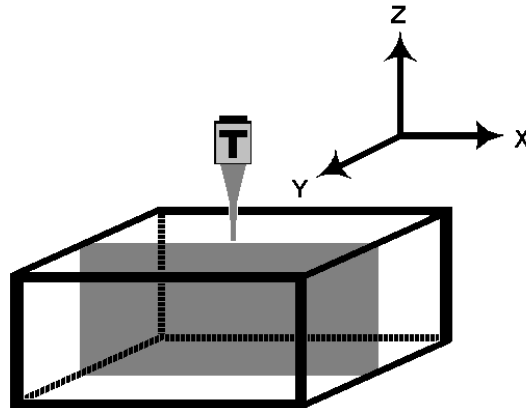
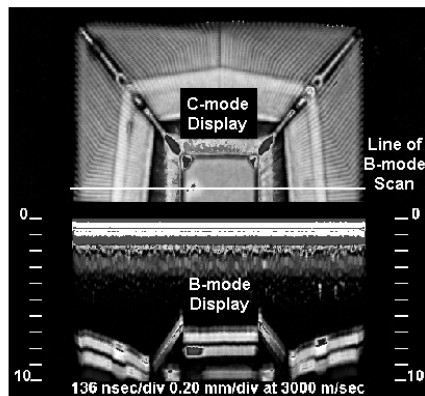


Example of A-mode display

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

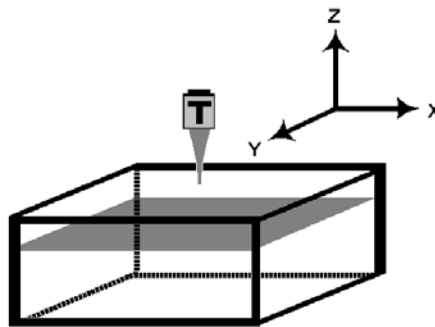
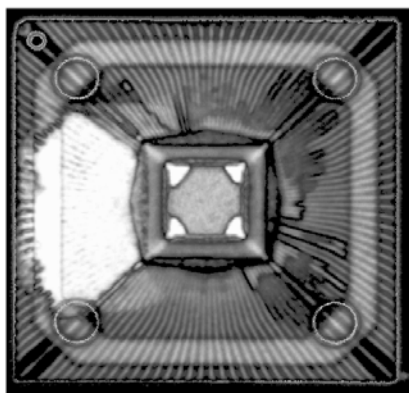
Terms, abbreviations, letter symbols, and definitions

acoustic data, B-mode: Acoustic data collected along an X-Z or Y-Z plane versus depth (Z) using a reflective acoustic microscope. A B-mode scan contains amplitude and phase/polarity information as a function of time of flight at each point along the scan line. A B-mode scan furnishes a two-dimensional (cross-sectional) description along a scan line (X or Y)..



Example of B-mode display (bottom half of picture on left)

acoustic data, C-mode: Acoustic data collected in an X-Y plane at depth Z using a reflective acoustic microscope. A C-mode scan contains amplitude and phase/polarity information at each point in the scan plane. A C-mode scan furnishes a two-dimensional (area) image of echoes arising from reflections at a particular depth (Z).



Example of C-mode display

References

J-STD-035, 5/99

J-STD-035, 5/99

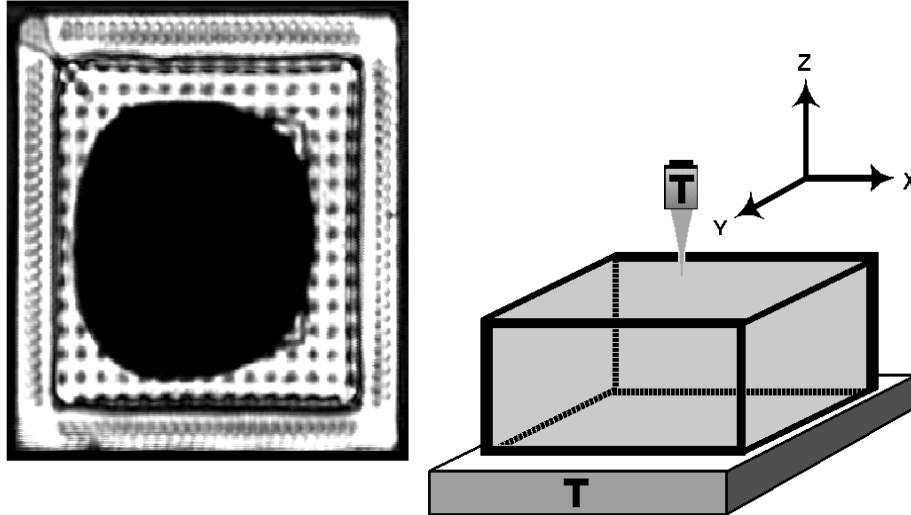
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions

References

acoustic data, through-transmission mode: Acoustic data collected in an X-Y plane throughout the depth (Z) using a through-transmission acoustic microscope. A through-transmission mode scan contains only amplitude information at each point in the scan plane. A through-transmission scan furnishes a two-dimensional (area) image of transmitted ultrasound through the complete thickness/depth (Z) of the sample or component.

J-STD-035, 5/99



Example of through-transmission display

acoustic microscope: Equipment that creates an image using ultrasound to view a specimen's surface or subsurface features,

J-STD-020D.1, 3/08

ac terminal: A terminal that is to be connected to the ac circuit.

JESD14, 11/86

ac test: The process of verifying the specified timing of a device.

JESD12-1B, 8/93
JESD99C, 12/12

NOTE Testing of propagation delays, minimum setup and hold times, minimum pulse durations, etc., can be performed by using test vectors applied at the specified operating frequency of the device. Propagation delays of critical logic paths for system operation can be measured individually.

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur.

JEP122G, 10/11
JEP143C, 7/12
JESD85, 7/01
JESD91A, 8/01

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy".

active circuit element: See "circuit element, active".

active desiccant: Desiccant that is either fresh (new) or has been baked according to the manufacturer's recommendations to renew it to original specifications.

J-STD-033C, 2/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

active device: A device in which at least one circuit element is an active circuit element.	JESD99C, 12/12
active element: See “circuit element, active”.	
active-pulldown output: A bipolar (three-state or totem-pole) output whose source-current capability significantly exceeds its sink-current capability.	JESD99C, 12/12
active-pullup output: A bipolar (three-state or totem-pole) output whose sink-current capability significantly exceeds its source-current capability.	JESD99C, 12/12
ac unbalanced voltage: The difference between the peak values of the ac voltages at the two outputs when the circuit is operating in the maximum-output-voltage-swing condition.	JESD99C, 12/12
ADC: See “analog-to-digital [A/D] converter”.	
address: (1) A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172.)	JESD100-B, 12/99
(2) To refer to a device or a data item by its address. (Ref. ANSI X3.172.)	
address data input/output [ADQ(n)]: The pins that are multiplexed three ways to serve as address input, data input, and data output pins. When the address data input/output numbering is significant for device operation, the addresses are numbered beginning with 0.	JESD21-C, 1/97
address inputs [A(n)]: Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another. When the address number is significant for device operation, the addresses are numbered beginning with 0.	JESD21-C, 1/97
address latch enable (AL): An input that, when true, allows the input address to be entered into a register and, when false, causes the address state previously entered to be latched.	JESD21-C, 1/97
address register: A register that is used to hold an address. (Ref. IEC 824.)	JESD100-B, 12/99
ADQ(n): See “address data input/output”.	
air ionizer: A source of charged air molecules (ions).	JESD625B, 1/12
AL: See “address latch enable”.	
alignment mark: Synonym for “registration mark”.	JESD99C, 12/12
“A” limit: The more positive (less negative) limit of a range of some quantity.	JESD99C, 12/12
alpha activity (of a source): The number of alpha particles produced by the decay of the alpha source per unit time.	JESD89-2A, 10/07

NOTE The preferred SI unit is the becquerel (Bq); to convert curies to becquerels, multiply the number of curies by 3.7×10^{10} Bq (exactly).

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

alternative method: For a device requirement that has a prescribed method to verify compliance, another method that has been verified through test and analysis to adequately verify compliance of the device with that requirement.

JESD93, 9/05

ALU: See “arithmetic and logic unit”.

ambient temperature; free-air temperature (T_A): The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

JESD10, 1/76
JESD77D, 8/12
RS-323, 3/66

A-mode: See “acoustic data, A-mode”.

A(n): See “address inputs”.

analog gate: A gate whose output signal is a linear function of one or more input signals.

JESD99C, 12/12

analog-to-digital [A/D] converter (ADC): A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range.

JESD99C, 12/12

NOTE This quantization procedure introduces inherent errors of $\pm\frac{1}{2}$ LSB (least significant bit) in the representation because, within this fractional range, only one analog value can be represented free of error by a single digital output code.

analog-to-digital processor: An integrated circuit providing the analog part of an analog-to-digital converter.

JESD99C, 12/12

NOTE Provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

analysis of variance (ANOVA): A statistical tool that allows for the comparison of more than two groups of data and provides valid assumptions. Computations of ANOVA involve partitioning total variation into two components: the variation from differences among group “means”, and random variations within the groups known as “error”. ANOVA provides for reliable results even when certain assumptions are violated.

JEP132, 7/98

annular ring: The metallization pad area around the top or bottom of a castellation hole.

JESD9B, 5/11

anode: (1) The p-type region from which the forward current flows within a semiconductor diode.

JESD77D, 8/12
JESD282-B, 4/00

NOTE In Schottky diodes, usually the barrier metal replaces the p-type semiconductor region and the remaining semiconductor region is n-type; however, some Schottky diodes have been made with the barrier metal replacing the n-type semiconductor region, in which case the remaining semiconductor region is p-type.

(2) A circuit element to which positive bias is applied.

JEP154, 1/08

NOTE For the purpose of JEP154, when the die is the anode the electron flow is from the substrate through the solder bump to the die.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

anode-cathode voltage; anode voltage (of a unidirectional thyristor): The voltage between the anode and cathode terminals.

JESD77D, 8/12

NOTE The anode-cathode voltage is called “positive” when the anode potential is higher than the cathode potential and called “negative” when the anode potential is lower than the cathode potential.

anode current: Synonym for “forward current”.

JESD77D, 8/12

anode terminal (A, a) (1) (general): The terminal connected to the p-type region of the p-n junction or, when two or more p-n junctions are connected in series and have the same polarity, to the extreme p-type region.

JESD77D, 8/12
JESD210, 12/07
JESD211, 12/09
JESD282-B, 4/00

NOTE 1 See note to “anode”.

NOTE 2 This definition does not apply to current-regulator diodes.

NOTE 3 For voltage-reference diodes, any temperature-compensation diodes that may be included shall be ignored in the determination of the anode terminal.

NOTE 4 For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the anode terminal.



JESD77D, 8/12

(2) (of a current-regulator diode): The terminal to which current flows from the external circuit when the diode is biased to operate as a current regulator.

JESD77D, 8/12

(3) (of a unidirectional diode thyristor): The terminal to which the current flows from the external circuit when the thyristor is in the on state.

JESD77D, 8/12

(4) (of a unidirectional triode thyristor): The main terminal to which the principal current flows from the circuit being controlled when the thyristor is in the on state.

NOTE A second anode terminal may be provided for connecting to the control circuit of an n-gate thyristor.

ANOVA: See “analysis of variance”. See also “variance components analysis”.

antistatic material: Material that inhibits triboelectric charging.

JESD625B, 1/12

NOTE The antistatic property of a material does not necessarily correlate with the resistivity or resistance of the material. Unlike the dissipative and conductive properties, antistatic is not defined by a measurable resistance range.

AOQ: See “average outgoing quality”.

APL: See “above passivation layer”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

JEP122G, 10/11
JEP143C, 7/12
JESD74A, 2/07
JESD85, 7/01#

NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature.

NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism.

NOTE 3 The apparent activation energy is empirically determined from the change in an observed time-to-failure distribution with temperature.

application requirements for quality and reliability: The quality and reliability properties of the product required for the specified use conditions.

JEP148A, 12/08

application-specific integrated circuit (ASIC): An integrated circuit developed and produced for a specific application or function and for a single customer.

JESD99C, 12/12

NOTE ASICs generally use standard cell or gate array design methodology.

application-specific standard product (ASSP): An integrated circuit developed and produced for a specific application or function but made available for multiple customers.

JESD99C, 12/12

application use conditions: The full environmental and/or operating ranges that the application is specified to function within.

JEP149, 11/04

arc: A visual anomaly that is a curved scratch.

JESD22-B118, 3/11

area array package: A package that has terminations arranged in a grid on the bottom of the package and contained within the package outline.

J-STD-020D.1, 3/08

arithmetic and logic unit (ALU): The part of a processor that performs arithmetic operations and logic operations. (Ref. IEC 824.)

JESD100-B, 12/99

arithmetic unit: The part of a processor that performs arithmetic operations. (Ref. IEC 824.)

JESD100-B, 12/99

NOTE This term is sometimes used for a unit that performs both arithmetic and logic operations.

array density (of a gate array): The number of available gates divided by the entire chip area.

JESD12-1B, 8/93
JESD99C, 12/12

NOTE Units are gates per unit area.

array, logic: Synonym for “gate array integrated circuit”.

JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

Arrhenius equation (for reliability): An equation used to calculate thermal acceleration factors for semiconductor device time-to-failure distributions:

JEP143C, 7/12
JESD91A, 8/01

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp [(-E_{aa}/k) (1/T_1 - 1/T_2)]$$

where

A_T is the acceleration factor due to changes in temperature;
 λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
 λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1});
 E_{aa} is the apparent activation energy (eV);
 k is Boltzmann's constant (8.62×10^{-5} eV/K);
 T_1 is the absolute temperature of test 1 (K);
 T_2 is the absolute temperature of test 2 (K).

NOTE 1 The original Arrhenius equation (for atomic or molecular processes and chemical reactions) used the gas constant, not an activation energy, in the exponent. The "Arrhenius equation (for reliability)", used to calculate a thermal acceleration factor for a given observed time-to-failure distribution and E_{aa} , is in the form of the quotient of two Arrhenius equations, so that the acceleration factor from one temperature to another can be calculated.

NOTE 2 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s , λ_o is the observed failure rate at some test temperature T_t , and A_T is the temperature acceleration factor from T_t to T_s .

ART: See "auto-load read transfer".

artwork: The original, accurately scaled, oversize drawings and plastic overlays of the microcircuit topological layout that are used to produce the master mask plates.

JESD99C, 12/12

NOTE Artwork has largely been supplanted by computer-produced drawings and masks.

ASER: See "accelerated soft error rate".

ASIC: See "application-specific integrated circuit".

assembled state (of a component): The state of a component that has been attached to a second-level assembly.

JEP150, 5/05
JEP156, 3/09
JEP158, 11/09

assembly, microelectronic: See "microelectronic assembly".

assignable cause: Synonym for "special cause".

associative memory: Synonym for "content-addressable memory". (Ref. IEC 748-2.)

JESD100-B, 12/99

ASSP: See "application-specific standard product".

asymmetry, full-scale (of a digital-to-analog converter with a bipolar analog range) (ΔI_{FSS} or ΔV_{FSS}): The difference between the absolute values of the two full-scale analog values.

JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

asynchronous circuit: A circuit whose changes of state are not controlled by a single clock.	JESD12-1B, 8/93 JESD99C, 12/12
ATE: Automated test equipment.	JESD89A, 10/06
attachment (noun): A capacitor, substrate cap, heat sink, etc. that is glued, soldered, or mechanically affixed to a device.	JESD22-B101B, 8/09
attribute data: Data that result from counting items or classifying items into distinct nonoverlapping categories. Examples are count data (e.g., the number of nonconforming items), ordinal data (e.g., rank: first, second; classification: excellent, good, poor), nominal data (e.g., unordered groupings such as defect type), or pass/fail data.	EIA-557-B, 2/06
attribute memory select (RG): An input that, when active (low), selects the attribute memory and, when inactive (high), selects the main memory for normal access.	JESD21-C, 1/97#
NOTE Attribute memory is a separately accessed section of memory on the card and is generally used to record capacity and other configuration and attribute information. Main memory is used to store user data.	
audit: The periodic observation of procedures and performed activities to evaluate compliance with requirements.	EIA-557-B, 2/06
autodoping: The introduction of impurities from the substrate into the epitaxial layer during the process of epitaxy.	JESD99C, 12/12
auto-load read transfer (ART): A split serial-access memory (SAM) data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.	JESD21-C, 1/97
auto-load write transfer (AWT): A split serial-access memory (SAM) data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.	JESD21-C, 1/97
automatic gain control range (AGC range): The maximum change in gain expressed in dB that may be achieved by application of a specified range of the dc voltages to the AGC input.	JESD99C, 12/12
auxiliary ground: A separate supplemental ground conductor for use other than general equipment grounding.	JESD625B, 1/12
auxiliary terminal (of a semiconductor power-control module): A terminal, other than an ac, dc, or control terminal, that may be provided for a specified purpose.	JESD14, 11/86#
available gates (in a gate array): The total number of potentially usable, unconnected gate equivalents in a given array area.	JESD12-1B, 8/93 JESD99C, 12/12
avalanche breakdown diode (ABD): A transient voltage suppressor that is a semiconductor diode with a single p-n junction (or with multiple p-n junctions none of which interact) whose operation depends in part on its breakdown characteristics.	JESD77D, 8/12 JESD210, 12/07
avalanche current, repetitive peak (I_{AR}): The peak current reached repetitively during device avalanche in an inductive-load switching circuit.	JESD24-8, 8/92#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

avalanche current, single-pulse peak (I_{AS}): The peak current reached during device avalanche in a single-pulse unclamped inductive-load switching circuit.

JESD24-5, 8/90#

avalanche duration (t_{av}): The time duration of device avalanche.

JESD24-5, 8/90
JESD24-8, 8/92

avalanche energy, repetitive (E_{AR}): The energy sustained by a device in avalanche per repetitive pulse in an inductive-load switching circuit.

JESD24-8, 8/92#

avalanche luminescent diode: A light-emitting diode that emits luminous energy when a controlled reverse current in the breakdown region is applied.

JESD77D, 8/12

avalanche voltage, drain-source ($V_{DSX(sus)}$): The effective (constant) device drain-source breakdown voltage during avalanche. The instantaneous device breakdown voltage will change with junction temperature during a test. $V_{DSX(sus)}$ can be calculated from a measurement of the avalanche duration, t_{av} .

JESD24-5, 8/90

average: The sum of the sample values divided by the number of sample values. A measure of location used to estimate the population mean.

EIA-557-B, 2/06

average charge-transfer efficiency: The n^{th} root of overall charge-transfer efficiency, where n is the number of transfers.

JESD99C, 12/12

average current: The value of a periodic current averaged over a full cycle unless otherwise specified.

JESD77D, 8/12
JESD282-B, 4/00

average dark current density (J_D): The average dark current per unit area within the active area of the device.

JESD99C, 12/12

NOTE Depending on the type of device, the active area may be defined as either the area of transfer channel or the overall area including channel-defining regions. Other names used are “average leakage current density” and “average thermal generation current density”.

average junction temperature ($T_{J(AV)}$): The average value of the virtual junction temperature of a given semiconductor device over an operating cycle.

RS-323, 3/66

average noise figure; average noise factor ($\bar{F}$ or $\bar{NF}$): The ratio of (1) the total output noise power within an output frequency band when the noise temperature of all input terminations is at the reference noise temperature, T_0 , at all frequencies that contribute to the output noise to (2) that part of (1) caused by the noise of the signal-input termination within the signal-input frequency band. (Ref. IEC 747-1.)

JESD77D, 8/12
JESD99C, 12/12
JESD311A, 11/81

NOTE 1 The abbreviation $\bar{NF}$ is often used in place of symbol $\bar{F}$; however, symbol $\bar{F}$ is preferred.

NOTE 2 This ratio may be expressed logarithmically in decibels (dB).

average outgoing quality (AOQ): The average lot fraction nonconforming, in parts per million, from a series of lots.

JESD16-A, 4/95

average pulse duration: See “pulse duration, average”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

average rectified output current, 50-Hz or 60-Hz sine-wave input, 180° conduction angle (I_O): The output current averaged over a full cycle from a rectifier with a 50-Hz or 60-Hz sine-wave input and a 180° conduction angle.

JESD77D, 8/12
JESD282-B, 4/00

average voltage: The value of a periodic voltage averaged over a full cycle unless otherwise specified.

JESD77D, 8/12
JESD282-B, 4/00

AWT: See “auto-load write transfer”.

axis of measurement (of a photoemitter): The direction from the source of radiant energy, relative to the optical axis, in which the measurement of radiometric and/or spectroradiometric characteristics is performed.

JESD77D, 8/12

B

B: See “byte”.

B: See “port A; port B”.

B; b: See “base terminal”.

b: See “bit”.

BA: See “bank address”.

back-end-of-line (BEOL) (adjective): Pertaining to the portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

JEP156, 3/09
JEP158, 11/09

back end of line (BEOL) (noun): The portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

JEP156, 3/09
JEP158, 11/09

background charge: A synonym for “bias charge”, used mainly in imaging devices.

JESD99C, 12/12

backside of flip chip die: The surface of the device opposite the face to which the solder bump interconnections are attached.

JESD22-B109A, 1/09

back-side substrate view area: The interface between the encapsulant and the back of the substrate within the outer edges of the substrate surface. (Refer to Type IV in Annex A of J-STD-035.)

J-STD-035, 5/99

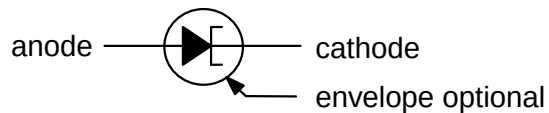
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

backward diode: A semiconductor diode in which quantum-mechanical tunneling leads to a current-voltage characteristic with a reverse current greater than the forward current, for equal and opposite applied voltages, in some voltage range centered about the origin.

JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



balanced amplifier: An amplifier in which the quiescent dc output voltage (or, if the output is a differential output, the difference between the two quiescent dc output voltages) has been reduced to zero or other specified level.

JESD99C, 12/12

ball bond: The adhesion or welding of a thin wire, usually gold, to a die pad metallization, usually an aluminum alloy, using a thermosonic wire bond process.

JESD22-B116A, 8/0
JESD99C, 12/12#

NOTE The ball bond includes the enlarged spherical, or nail-head, portion of the wire (provided by the flame-off and first bonding operation in the thermal compression and thermosonic process, or both), the underlying bonding pad and the ball bond-bonding pad intermetallic weld interface.

ball grid array (BGA) package: A package in which the external connections to the package are made via a rectangular array of ball-type connections, all on a common plane.

JESD21-C, 1/97
JESD217, 9/10

NOTE See also “grid array package”.

bandwidth (*B* or *BW*): The range of frequencies within which the gain of the amplifier is not more than 3 dB below the value of the midband gain.

JESD99C, 12/12

NOTE Midband gain is the gain at a specified frequency or the average gain over a specified frequency range.

bandwidth, maximum output swing (*B_{OM}*): The range of frequencies within which the maximum output voltage swing is above the specified value at a specified load impedance.

JESD99C, 12/12

bandwidth, unity gain: The range of frequencies within which the open-loop amplification is greater than unity.

JESD99C, 12/12

bank address (BA): In a RAM that has multiple banks in its architecture, the address used to select any one of the available banks.

JESD21-C, 1/97

bar code label: A label that includes information in a code consisting of parallel bars and spaces or a 2-D matrix format.

J-STD-033C, 2/12

NOTE 1 See also “linear bar code label”.

NOTE 2 For the purpose of J-STD-033, the bar code label is on the lowest level shipping container and includes information that describes the product, e.g., part number, quantity, lot information, supplier identification, and moisture-sensitivity level.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

bar code symbol: A symbol that gives information in a code consisting of parallel bars and spaces of various specific widths.

JESD22-B114A, 5/11

base (nonspecific): The overall combination of base region, base terminal, and the interface between them.

JESD77D, 8/12

NOTE This term should be used in this manner only when no confusion is likely to occur.

base (of a package): The part of a package that includes the surface on which a chip is intended to be mounted.

JESD9B, 5/11#
JESD99C, 12/12

base-emitter saturation voltage: See “saturation voltage, base-emitter”.

base materials: The laminates and/or the prepregs used to fabricate a PCB.

J-STD-609A.01, 2/11

NOTE A prepreg is a sheet of material that has been impregnated with a resin cured to an intermediate stage, i.e., B-staged resin. (Ref. IPC-T-50).

base metal: (1) The unplated main metal material of which the metal package, lead, or braze is constructed.

JESD9B, 5/11

(2) A metal alloy residing beneath all surface finish(es) and/or underplate.

JESD201A, 8/08

base plane (of a package): A plane parallel to the seating plane through the lowest point on the body of the package. It may coincide with the seating plane.

RS-308-A, 8/81
Rescinded 5/09

base region (of a unijunction transistor): A region of a semiconductor device into which majority carriers are injected.

JESD77D, 8/12

base region, functional: A control region through which the principal current passes and in which the concentration of principal-current charge carriers is the result of an applied base current.

JESD77D, 8/12

NOTE 1 The principal current is the result of diffusion and impurity concentration gradient drift.

NOTE 2 This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

base region, physical: (1) A region that lies between an emitter and a collector of a transistor and into which minority carriers are injected. (Ref. 60 IRE 28.S1.)

JESD10, 1/76

(2) The physical region that is located between the collector junction and the emitter junction and contains the control region.

JESD77D, 8/12

base terminal (B, b): The specified externally available point of connection to the base region.

JESD77D, 8/12

basic dimension: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. Permissible variations from the basic dimension are established by tolerances on associated dimensions, in notes, or in feature control frames.

JESD95-1, 3/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

bathtub curve: A plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (decreasing failure rate), intrinsic or useful life (relatively constant failure rate), and wearout (increasing failure rate).

JEP122G, 10/11
JEP143C, 7/12
JESD74A, 2/07
JESD85, 7/01
JESD91A, 8/01

battery voltage detect [BD(n)]: The signals BD1 and BD2 generated by the memory card as an indication of the condition of the battery on the memory card. Both signals are kept asserted when the battery is in good condition. When BD2 is negated while BD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the card is still assured. If BD1 is negated with BD2 either asserted or negated, the battery is no longer serviceable and data is lost.

JESD21-C, 1/97

baud: A unit of signaling speed equal to the number of discrete conditions or signal events per second. (Ref. ANSI X3.172.)

JESD100B.01, 12/02

NOTE For example, one baud equals one bit per second in a train of binary signals or one 3-bit value per second in a train of signals each of which can assume one of eight (2^3) different states.

BBD: See “bucket-brigade device”.

BCCD: See “buried-channel charge-coupled device”.

BCD: See “bipolar-and-CMOS-and-DMOS technology”.

BCXXX series: A BiCMOS series that includes devices whose input logic levels are TTL-compatible and whose outputs are specified at TTL levels; the low-level output voltage is specified at 24 mA and 48 mA.

JESD54, 2/96#

BD(n): See “battery voltage detect”.

BDRAM: See “burst DRAM”.

beam lead: A thick-film lead formed on and attached to the chip interconnection pattern and projecting cantilevered beyond the chip periphery for attachment to a substrate.

JESD99C, 12/12

behavioral description: The algorithms or equations defining a function.

JESD12-1B, 8/93
JESD99C, 12/12

benchmark: A standard by which something can be judged.

EIA-599-A, 6/98

BFR/CFR: See “brominated/chlorinated flame retardants”.

BG: See “byte-mode enable”.

BGA: See “ball grid array package”.

bias: (1) A voltage or current applied to an electronic device to establish a reference level for operation.

Merriam-Webster's
Collegiate Dict.

(2) The difference between the mean (or expectation) of an estimator, T , and the true value, θ , of a parameter: $E(T) - \theta$.

JESD37, 10/92

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions

References

bias charge; circulating bias charge (for analog signal applications): A charge that defines the no-signal level.

JESD99C, 12/12

NOTE This charge is inserted into all potential wells electrically or by radiation.

BiCMOS: See “bipolar-and-CMOS technology”.

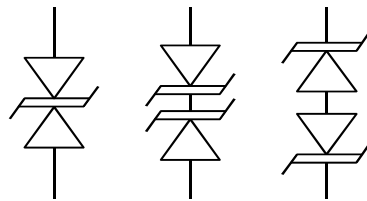
BiCMOS series: A series that includes devices combining bipolar and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

JESD54, 2/96

bidirectional ABD: A two-terminal ABD with a voltage-current avalanche breakdown characteristic in both directions, which can be either symmetrical or asymmetrical.

JESD77D, 8/12
JESD210, 12/07

NOTE Large transient currents will be clamped for voltage of either polarity across two similar p-n junctions in series connected in opposite directions. During a transient current event in this operating mode, one of the two p-n junctions is always in avalanche breakdown and the other is in the forward-conducting, low-voltage mode. The voltage across the bidirectional ABD is the sum of these two voltages. The avalanche breakdown voltage is substantially the same in both directions for a symmetrical bidirectional ABD; however, it may also be intentionally different or asymmetrical by design for special applications. Since multiple p-n junction capacitances in series reduce the overall total capacitance, the bidirectional ABD has lower capacitance than its unidirectional counterpart.

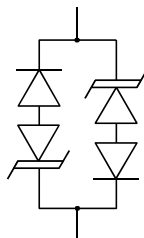


Bidirectional ABD symbol options

bidirectional low-capacitance ABD: A two-terminal device comprising two anti-parallel unidirectional-blocking low-capacitance ABD devices.

JESD77D, 8/12
JESD210, 12/07

NOTE The rectifier p-n junctions have low capacitance and must have a reverse blocking voltage greater than the avalanche breakdown voltage of the anti-parallel unidirectional ABD element.



bidirectional thyristor surge protective device: A thyristor surge protective device having substantially the same switching characteristics in the first and third quadrants.

JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

BiFET: See “bipolar-and-FET technology”.

big endian: The format in which the most significant bit of a word is transferred first and the least significant bit is transferred last.

JESD96, 4/04

BiMOS: See “bipolar-and-MOS technology”.

binomial distribution: A specific discrete probability distribution for attributes data.

EIA-557-B, 2/06

bipolar-and-CMOS-and-DMOS (BCD) technology: A technology for combining bipolar transistors, silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices, and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

JESD99C, 12/12

bipolar-and-CMOS (BiCMOS) technology: A technology for combining bipolar transistors and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

JESD55, 5/96#
JESD99C, 12/12

bipolar-and-FET (BiFET) technology: A technology for combining bipolar transistors and junction-gate field-effect transistors (JFET) in a single-chip integrated circuit.

JESD99C, 12/12

bipolar-and-MOS (BiMOS) technology: A technology for combining bipolar transistors and metal-gate metal-oxide-semiconductor (MOS) or metal-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

JESD99C, 12/12

bipolar output: An output having internal connections through two active devices to two supply voltages so that, according to the relative states of the active devices, the output can source or sink current through the load.

JESD99C, 12/12

bipolar technology: A technology for producing devices in which electrical conduction depends on the flow of both majority and minority carriers.

JESD77D, 8/12
JESD99C, 12/12

bipolar transistor (general): A transistor in which, in the operating mode, the controlling input consists of charge carriers that are injected into the control region and are of a polarity that is opposite to the polarity of the principal-current charge carriers, and in which the magnitude of the principal current depends on the magnitude of the control current.

JESD77D, 8/12

bistable logic function: A sequential logic function that has two and only two stable internal output states. (Ref. ANSI/IEEE Std 91.)

JESD99C, 12/12

bit (b): (1) In the binary numeration system, either of the digits 0 or 1. (Ref. ANSI X3.172.)

JESD100B.01, 12/02

NOTE Abbreviated form of “binary digit”.

(2) The unit of storage capacity that corresponds to a single memory cell.

bit plane: In a semiconductor memory device having a data interface that is wider than one bit, those storage cells and associated circuitry that are associated with a given bit in the data interface.

JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

bit slice; slice: A partition of a microprocessor that enables several identical units to be paralleled or cascaded and augmented by control logic to realize the central processing unit.	JESD100-B, 12/99
bit-slice processor: A central processing unit constructed of an array of identical units, each of which operates simultaneously upon one or more adjacent bits. (Ref. IEC 824.)	JESD100-B, 12/99
bit-wide device: A device that has only a single-bit data interface.	JESD21-C, 1/97# JESD100B.01, 12/02
blackbody: Ideally, a body that would absorb all and reflect none of the radiant energy falling upon it; its reflectivity would be zero and its absorptivity (and consequently, its emissivity) would be 100%. In practice, a radiator of uniform temperature whose radiant emittance in all parts of the spectrum is the maximum obtainable from any radiator at the same temperature, or a radiator whose spectral radiant emittance conforms with Planck's law of radiation.	JESD51-1, 12/95# JESD51-13, 6/09# JESD77D, 8/12
blemish: A visual anomaly that is an area of inconsistent finish.	JESD22-B118, 3/11
“B” limit: The less positive (more negative) limit of a range of some quantity.	JESD99C, 12/12
blistering: Detachment of material from a surface creating a bubble-like shape.	JESD9B, 5/11
BLM: See “under-bump metal”.	
block: A continuous range of memory addresses. (Ref. IEC 748-2.)	JESD100-B, 12/99
NOTE The number of addresses included in the range is frequently equal to 2^n , where n is the number of bits in the address.	
blocking: A term describing the state of a semiconductor device or junction that imposes high resistance to the passage of current.	JESD77D, 8/12 JESD282-B, 4/00
blocking period (of a rectifier circuit element): The part of an alternating-voltage cycle during which the current flows in the reverse direction.	JESD282-B, 4/00
NOTE The blocking period is not necessarily the same as the reverse period because of the effect of circuit parameters and semiconductor rectifier diode characteristics.	
block select (BS): A group of input signals that enable individual bit blocks of the data interface.	JESD21-C, 1/97
block write, no mask (BW): A RAM write cycle in which four bits are written into each bit plane as defined by the contents of the color register. The four bits are those locations controlled by the two least significant bits (LSB) of the column address.	JESD21-C, 1/97
block write with new mask (BWNM): A block-write cycle in which the data written is also controlled by the write mask supplied on the DQ(n) terminals in that cycle.	JESD21-C, 1/97
block write with old mask (BWOM): A block-write cycle in which the data written is controlled by the contents of the write-mask register that was previously loaded in a load-write-mask cycle.	JESD21-C, 1/97
B-mode: See “acoustic data, B-mode”.	

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

body (of a package): That part of the package or device excluding electrical terminals, studs, leads, etc.

RS-308-A, 8/81
Rescinded 5/09

body (of a semiconductor device): The semiconductor portion of a device limited by the physical extent of the crystalline or amorphous semiconductor material and including any associated oxide layers and metallization.

JESD77D, 8/12
JESD99C, 12/12

Boltzmann's constant (k): A constant equal to 1.38×10^{-23} joule per kelvin or 8.62×10^{-5} electronvolt per kelvin.

JEP122G, 10/11
JEP143C, 7/12

bond and assembly (B&A) process: A process associated with connecting chips (dice) to other package elements and assembling semiconductor-device packages.

JEP156, 3/09
JEP158, 11/09

bond, ball: See "ball bond"

bond, chip: The attachment of the circuit chip to a hybrid or package substrate.

JESD99C, 12/12

NOTE The attachment serves as a mechanical support, a thermal path, and sometimes an electrical contact.

bond, die: Synonym for "semiconductor chip bond".

JESD99C, 12/12

bond, face: A bond directly between a chip bonding pad and a mounting substrate for the purpose of making electrical contact.

JESD99C, 12/12

bond footprint (of a wedge bond): The area of the wire that has a physical bond interface (intermetallic or recrystallized) with respect to the compressed area of the wire.

JESD22-B116A, 8/09

bonding (critical) area: The surface on a lead or package to which wires will be bonded (i.e., the wire-bond area).

JESD9B, 5/11

NOTE 1 This term is not to be confused with the "die bond area" which is specified as the "die-attach area" in this specification.

NOTE 2 The critical wirebond area on a ceramic package is a metallization trace whose length is 0.381 mm (0.015 inch) and whose width is 80% of the width of the designed wire-bond trace, as specified in the applicable procurement document.

bonding surface: Either 1) the die pad metallization or 2) the package surface metallization to which the wire is ball-, wedge-, or stitch-bonded.

JESD22-B116A, 8/09

bonding trace; wire-bond trace: A metallized path on a package or substrate to which a bond wire is wire-bonded.

JESD9B, 5/11

bonding wire: A wire that is bonded to a chip bonding pad in order to connect the chip to any other point within the device package.

JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

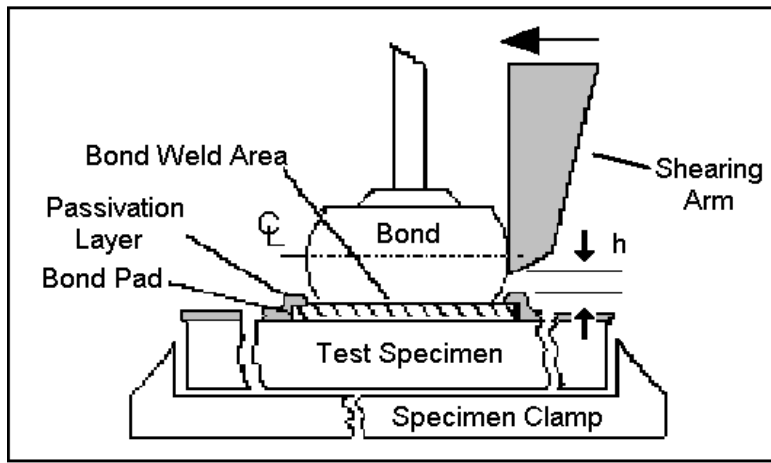
Terms, abbreviations, letter symbols, and definitions

References

bond shear: A process in which an instrument uses a chisel-shaped tool to shear or push a ball or wedge bond off the bond pad (see figure below).

JESD22-B116A, 8/09

NOTE The force required to cause this separation is recorded and is referred to as the bond shear force. The bond shear force of a gold ball bond, when correlated to the diameter of the ball bond, is an indicator of the quality of the metallurgical bond between the gold ball bond and the bond pad metallization. The bond shear force of an aluminum wedge bond, when compared to the manufacturer's tensile strength of the wire, is an indicator of the integrity of the weld between the aluminum wire and the bond pad or package surface metallization.



bond-shear code for ball and wedge bond, type 1 — bond lift: A separation of the entire wire bond from the bonding surface with only an imprint being left on the bonding surface and very little evidence of intermetallic formation or welding or of disturbance of the bonding surface metallization.

JESD22-B116A, 8/09

bond-shear code for ball and wedge bond, type 2 — bond shear: A separation of the wire bond in which 1) a thin layer of the bonding surface metallization remains with the wire bond and an impression is left in the bonding surface, 2) intermetallics remain on the bonding surface and with the wire bond, or 3) a major portion of the wire bond remains on the bonding surface.

JESD22-B116A, 8/09

bond-shear code for ball and wedge bond, type 3 — cratering: A condition under the die pad metallization in which the insulating layer (oxide or interlayer dielectric) and the bulk material (silicon) separate or chip out.

JESD22-B116A, 8/09

NOTE 1 Separation interfaces that show pits or depressions in the insulating layer (not extending into the bulk) are not considered craters.

NOTE 2 Cratering can be caused by several factors including the wire bonding operation, the post-bonding processing, and even the act of shear testing itself.

NOTE 3 Cratering present prior to the shear test operation denotes a pre-existing condition that must be addressed. Any bonds with preexisting cratering are invalid for this test method and shall not be included with the shear data.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References****bond-shear code for ball and wedge bond, type 4 — arm contacts specimen bonding surface**

JESD22-B116A, 8/09

contact: A condition produced when the shear tool contacts the bonding surface.

NOTE This condition may be due to improper placement of the specimen, a low shear height, or instrument malfunction. This bond shear type is an invalid result and shall be eliminated from the shear data.

bond-shear code for ball and wedge bond, type 5 — shearing skip: A condition produced when the shear tool removes only the topmost portion of the ball or wedge bond.

JESD22-B116A, 8/09

NOTE This condition may be due to improper placement of the specimen, a high shear height or instrument malfunction. This bond shear type is an invalid result and shall be eliminated from the shear data.

bond-shear code for ball and wedge bond, type 6 — bond pad (or bonding surface) lift: A separation between the bonding surface metallization and the underlying substrate or base material. There is evidence of bonding surface metallization remaining attached to the ball or wedge bond.

JESD22-B116A, 8/09

bond, stitch: A thermocompression bond in which a capillary tube is used for both feeding the wire and forming the bond.

JESD99C, 12/12

bond, thermocompression: A bond in which two members are joined through the combined application of heat and pressure.

JESD99C, 12/12

bond, ultrasonic: A bond in which two members are joined through the combined application of pressure and an ultrasonic oscillatory lateral motion.

JESD99C, 12/12

bond, wedge: A thermocompression bond in which a wedge-shaped tool is used to apply pressure to the wire being attached.

JESD99C, 12/12

bond, wire: The attachment between a bonding wire and a chip bonding pad or package terminal.

JESD99C, 12/12

boundary scan: A design methodology in which the I/O buffers of a circuit or functional block are observed and controlled by scan cells.JESD12-1B, 8/93
JESD99C, 12/12

NOTE The Boundary Scan standard was developed by the Joint Test Action Group (JTAG) and is embodied in IEEE Standard 1149-1.

brazed: A metallic material used to join two metals or metallized components.

JESD9B, 5/11

brazed climb: The distance from the surface of the package to the top of the brazed line on a lead, not including brazed flash.

JESD9B, 5/11

brazed flash: The brazed material that has flowed over or out of the designed contained brazed area and is less than 0.0254 mm (0.001 inch) thick.

JESD9B, 5/11

brazed run-out: The brazed material that has flowed over or out of the designed contained brazed area, not including brazed flash.

JESD9B, 5/11

brazed undercut: The brazed material recessed from the package surface at the interface of the package wall and the package base.

JESD9B, 5/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

breakdown: The phenomenon, occurring in a reverse-biased semiconductor junction, whose initiation is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current.

JESD10, 1/76
JESD24, 7/85
JESD77D, 8/12
JESD282-B, 4/00

breakdown current: A current in a breakdown region.

JESD77D, 8/12
JESD282-B, 4/00

breakdown region (1) (of a thyristor surge protective device): The portion of the characteristic that starts with the transition from the high dynamic resistance off state to a substantially lower dynamic resistance and extending to the switching point.

ESD77D, 8/12
JESD210, 12/07

(2) (of a voltage regulator diode): The portion of the voltage-current characteristic beyond the initiation of breakdown where the current increases rapidly for any additional increase in reverse voltage.

JESD211, 12/09

NOTE In this region the voltage remains essentially constant for increases in reverse current, up to a specified current and power dissipation rating.

(3) (reverse): The portion of the voltage-current characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current.

JESD10, 1/76#
JESD24, 7/85#
JESD77D, 8/12
JESD282-B, 4/00

breakdown voltage: A voltage in a breakdown region.

JESD10, 1/76#
JESD24, 7/85#
JESD77D, 8/12
JESD282-B, 4/00#

breakdown voltage, collector-base, emitter open ($V_{(BR)CBO}$) (formerly BV_{CBO}):

The breakdown voltage between the collector and base terminals when the collector terminal is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited.

JESD10, 1/76
JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References****breakdown voltage, collector-emitter, base open ($V_{(BR)CEO}$) (formerly BV_{CEO}):**

JESD10, 1/76

breakdown voltage, collector-emitter, base short-circuited to emitter

JESD77D, 8/12

($V_{(BR)CES}$) (formerly BV_{CES}):**breakdown voltage, collector-emitter, circuit between base and emitter****($V_{(BR)CEX}$) (formerly BV_{CEX}):****breakdown voltage, collector-emitter, resistance between base and emitter****($V_{(BR)CER}$) (formerly BV_{CER}):****breakdown voltage, collector-emitter, voltage between base and emitter****($V_{(BR)CEV}$) (formerly BV_{CEV}):**

The breakdown voltage between the collector and emitter terminals when the collector terminal is biased in the reverse direction* with respect to the emitter terminal, and the base terminal is, respectively,

- open-circuited.
- short-circuited to the emitter terminal.
- returned to the emitter terminal through a specified circuit.
- returned to the emitter terminal through a specified resistance.
- returned to the emitter terminal through a specified voltage.

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for npn transistors or negative for pnp transistors with respect to the emitter terminal.

breakdown voltage, drain-source, with circuit between gate and source ($V_{(BR)DSX}$):

JESD24, 7/85

The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified circuit.

breakdown voltage, drain-source, with gate short-circuited to source ($V_{(BR)DSS}$):

JESD24, 7/85

The breakdown voltage between the drain terminal and the source terminal when the gate terminal is short-circuited to the source terminal.

breakdown voltage, drain-source, with resistance between gate and source ($V_{(BR)DSR}$):

JESD24, 7/85

The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified resistance.

breakdown voltage, drain-source, with voltage between gate and source ($V_{(BR)DSV}$):

JESD24, 7/85

The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified voltage.

breakdown voltage, emitter-base, collector open ($V_{(BR)EBO}$) (formerly BV_{EBO}):

JESD10, 1/76

The breakdown voltage between the emitter and base terminals when the emitter terminal is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE Std 255.)

breakdown voltage, forward gate-source ($V_{(BR)GSSF}$): The breakdown voltage between the gate terminal and the source terminal with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.

JESD24, 7/85

NOTE The symbol $V_{(BR)GSSF}$ should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions

References

breakdown voltage, gate-source ($V_{(BR)GSS}$): The breakdown voltage between the gate terminal and the source terminal when the drain terminal is short-circuited to the source terminal.

JESD24, 7/85

NOTE The symbol $V_{(BR)GSS}$ is used primarily with junction-gate field-effect transistors.

breakdown voltage, reverse gate-source ($V_{(BR)GSSR}$): The breakdown voltage between the gate terminal and the source terminal with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.

JESD24, 7/85

NOTE The symbol $V_{(BR)GSSR}$ should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.

breakover point (of a thyristor): In a quadrant in which switching can occur, the point for which the differential resistance is zero and the off-state voltage reaches a maximum value.

JESD77D, 8/12

bridge (output): Synonym for “full-bridge (output)”.

JESD99C, 12/12

bridge rectifier circuit: A double-way rectifier circuit in which (1) each terminal of the alternating-voltage circuit is connected to the anode of one rectifier element in a set of elements whose cathodes are all connected to the positive output of the circuit, (2) each terminal of the alternating-voltage circuit is also connected to the cathode of one rectifier element in another set of elements whose anodes are all connected to the negative output, and (3) the load is connected between the positive and negative outputs.

JESD77D, 8/12

NOTE The term is derived from the similarity in layout of a single-phase four-element bridge rectifier to that of a Wheatstone bridge.

bright tin: A tin film with higher internal stresses than matte tin, grain sizes of 0.5 μm to 0.8 μm , and a carbon content of 0.2% to 1.0%.

JP002, 3/06

brominated/chlorinated flame retardants (BFR/CFR): Flame retardants that contain bromine and/or chlorine.

JS709A, 5/12

NOTE These compounds are typically added to or reacted into polymers such as certain epoxy resins and thermoplastics to reduce their flammability. Examples include, but are not limited to, tetrabromobisphenol-A (TBBPA), brominated epoxy resins, and polybrominated diphenyl ethers (PBDEs).

BS: See “block select”.

bubble, subsurface: A bubble, in the glass-to-metal seal, that is below the top surface of the seal and is not open or cannot be opened with a wood probe.

JESD9B, 5/11

bubble, surface; open-surface bubble: A bubble in the glass-to-metal seal that is the top surface of the seal and is either open or can be opened with a wood probe.

JESD9B, 5/11

bucket-brigade device (BBD): A charge-transfer device that stores charge in discrete regions in a semiconductor and transfers this charge as a packet through a series of switching devices that interconnect these regions.

JESD99C, 12/12

NOTE This term and its abbreviation may be preceded by bipolar, JFET, MOS, SIS, etc., according to the technology used for the switching devices.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

buffer: (1) An isolating circuit used to minimize the effects of a driven circuit on the driving circuit. (Adapted from ANSI/IEEE Std 100 and ANSI X3.172.)

JESD99C, 12/12
JESD100B.01, 12/02

(2) A routine or storage used to compensate for a difference in the rate of flow of data or in the time of occurrence of events, when transferring data from one device to another.
(Ref. ANSI X3.172.)

JESD100B.01, 12/02

buffered (output): An output whose on-state impedance is independent of any valid input logic conditions, both preceding and present.

JESD13-B, 5/80#

buffer storage: Storage used to compensate for a difference in the rate of flow of data between components of an automatic data processing or communications system, or in the time of occurrence of events in the components. (Adapted from ANSI X3.172.)

JESD100B.01, 12/02

built-in electric field (in a transition region): The internal electric field in the absence of bias.

JESD77D, 8/12

bulk-channel charge-coupled device (BCCD): Synonym for “buried-channel charge-coupled device”.

JESD99C, 12/12

bulk characteristics (of a semiconductor material): The characteristics of a piece of semiconductor material that has uniform properties throughout the whole piece, as measured in those parts of the piece in which the measured value of a characteristic is not modified by the proximity of the boundaries of the piece.

JESD77D, 8/12

NOTE Bulk characteristics for pieces smaller than required by the definition are those that would be measured for a sufficiently large piece having the same technological properties.

bulk current, dc (I_B): The direct current into the bulk contact.

JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

bulk reflow: Reflow of multiple components, with simultaneous attachment, by an infrared (IR), convection/IR, convection, or vapor phase reflow (VPR) process.

J-STD-033C, 2/12

bulk-source voltage, dc (V_{BS}): The dc bulk-to-source voltage.

JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

bump-limiting metal: Synonym for “under-bump metal”.

buried channel: A transfer channel beneath the surface of a semiconductor.

JESD99C, 12/12

buried-channel charge-coupled device (BCCD); bulk-channel charge-coupled device (BCCD); peristaltic charge-coupled device: A charge-coupled device that confines the flow of charges to a channel lying beneath the surface of the semiconductor.

JESD99C, 12/12

burn mark: A visual anomaly with a burned appearance.

JESD22-B118, 3/11

burr (on a package): A fragment of excess material or foreign particle adhering to a surface.

JESD27, 8/93
Rescinded 5/11

burst DRAM (BDRAM): A DRAM that has burst-mode-data capability.

JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

bus: A common path along which power or signals travel from one or several sources to one or several destinations. (Adapted from IEC 824.)	JESD100-B, 12/99
bus driver: A line driver used for fan-out to multiple receivers via a transmission line.	JESD99C, 12/12
bus receiver: A line receiver intended to be driven from a bus.	JESD99C, 12/12
busy (BY): The output that, on some devices, signifies that some internal asynchronous operation is still in process and that the device is not available for normal functions. This signal is normally implemented so that multiple devices can be OR-tied.	JESD21-C, 1/97
busy signal: Synonym for “wait signal”.	JESD100-B, 12/99
BW: See “bandwidth”.	
BW: See “block write, no mask”.	
BWNM: See “block write with new mask”.	
BWOM: See “block write with old mask”.	
Bxxx: A device name (e.g., BDRAM) whose first letter (B) indicates that the device has a “burst” data capability.	JESD21-C, 1/97#
BY: See “busy”.	
byte (B): (1) A binary character string operated upon as a unit and usually shorter than a computer word. (Ref. ANSI X3.172.)	JESD100-B, 12/99
NOTE A byte is usually eight bits.	
(2) The unit of storage capacity equal to eight bits.	
byte-mode enable (BG): An input that, when true, causes a word-wide device to operate in the byte mode and to present the high or low byte on a predefined data pin set. Truth tables are provided to define the details of the operation.	JESD21-C, 1/97
byte-wide device: A device that has a parallel data interface of eight bits, possibly with additional bits appended to provide parity or error-detection capability.	JESD21-C, 1/97# JESD100-B, 12/99
byte [word] identifier (x): In the pin names and their definitions in section 2 of JESD21-C, an alphabetic identifier for the byte [word] being accessed.	JESD21-C, 1/97

C

C: See “output clock”.

C; c: See “collector terminal”.

CA: See “column address”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

cache memory: A special buffer storage, smaller and faster than main storage, that is used to hold a copy of data or instructions that have been obtained automatically from main storage and are likely to be needed soon by the processor. (Adapted from ANSI X3.172.)

JESD100-B, 12/99

NOTE It is placed between the CPU and main storage to make main storage look like fast memory.

CAM: See “content-addressable memory”.

can package: Generally, a cylindrical package whose terminals exit from one end parallel to the axis of the package.

JESD30E, 8/08

capability: The natural variation of the process due to common causes.

EIA-557-B, 2/06
EIA-599-A, 6/98

capability analysis: The study of a process to determine the probability that the characteristics of its output will fall within a previously defined set of constraints.

JEP132, 7/98

capability index: A measure of the relationship between the specification limits and the capability. See EIA-738, *Guideline on the Use and Application of Cpk* and *The Use and Abuse of Cpk* by Berton H. Gunter.

EIA-557-B, 2/06

capacitance: The capacitance between the two terminals of a diode at a specified voltage.

JESD211, 12/09

card detect [CD(n)]: The two signals, CD1 and CD2, that provide for proper memory card insertion detection and are positioned at opposite ends of the connector to facilitate the detection process. The signals are connected to ground internally on the memory card; thus they will be forced low whenever a card is placed in a host socket. The host socket interface circuitry shall provide 10-kΩ pull-up resistors to VCC on each of these signal pins.

JESD21-C, 1/97

carrier: A pocket tape, tray, tube or other fixture used to store and transport devices and components.

JESD22-B101B, 8/09#
J-STD-033C, 2/12#

carrier, (charge) (in a semiconductor): A mobile (i.e., free) conduction electron or mobile hole. (Ref. IEC 747-1.)

JESD77D, 8/12

CAS: See “column enable”.

case: Synonym for “package”.

case temperature (T_C): The temperature measured at a specified location on the case of a device.

JESD10, 1/76
JESD77D, 8/12

case-to-ambient thermal resistance: See “thermal resistance, case-to-ambient”.

CAS latency (for an SDRAM): Synonym for “read latency”.

JESD100-B, 12/99

castellation: A semicircular or crown-shaped metallized surface.

JESD9B, 5/11

catastrophic failure: A failure that has serious consequences for the failed device or other components associated with it in the circuit (e.g., input shorted to power supply or ground, power-supply-to-ground short circuit, destructive latch-up, etc.).

JEP134, 9/98

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

cathode: (1) The n-type region to which the forward current flows within a semiconductor diode.

JESD77D, 8/12
JESD282-B, 4/00

NOTE In Schottky diodes, usually the barrier metal replaces the p-type semiconductor region and the remaining semiconductor region is n-type; however, some Schottky diodes have been made with the barrier metal replacing the n-type semiconductor region, in which case the remaining semiconductor region is p-type.

(2) A circuit element to which negative bias is applied.

JEP154, 1/08

NOTE For the purpose of JEP154, when the die is the cathode, the electron flow is from the die through the solder bump to the substrate.

cathode current: Synonym for “reverse current”.

JESD77D, 8/12

cathode terminal (K, k) (1) (general): The terminal connected to the n-type region of the p-n junction or, when two or more p-n junctions are connected in series and have the same polarity, to the extreme n-type region.

JESD77D, 8/12
JESD210, 12/070
JESD211, 12/09
JESD282-B, 4/00

NOTE 1 See note to “cathode”.

NOTE 2 This definition does not apply to current-regulator diodes.

NOTE 3 For voltage-reference diodes, any temperature-compensation diodes that may be included shall be ignored in the determination of the cathode terminal.

NOTE 4 For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the cathode terminal.

JESD77D, 8/12

(2) **(of a current-regulator diode):** The terminal from which current flows into the external circuit when the diode is biased to operate as a current regulator.

JESD77D, 8/12

(3) **(of a unidirectional diode thyristor):** The terminal from which the current flows to the external circuit when the thyristor is in the on state.

JESD77D, 8/12

(4) **(of a unidirectional triode thyristor):** The main terminal from which the principal current flows to the circuit being controlled when the thyristor is in the on state.

NOTE A second cathode terminal may be provided for connecting to the control circuit of a p-gate thyristor.

cause-and-effect diagram: A tool for individual or group problem-solving that uses a graphic description of the various process elements to analyze potential sources of process variation. Also called a “fishbone diagram” (after its appearance) or “Ishikawa diagram” (after its developer).

JEP132, 7/98
EIA-557-B, 2/06

cavity package: A package containing a cavity that is intended to be occupied by a chip.

JESD22-B103B, 6/02#
JESD22-B104C, 11/04#

CBGA: Ceramic ball grid array package.

JESD217, 9/10

CCD: See “charge-coupled device”.

CCGA: Ceramic column grid array package.

JESD217, 9/10

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

CDM: See “charged-device model”.

CD(n): See “card detect”.

CE: See “column enable”.

cell-based integrated circuit: An integrated circuit fabricated with a unique full set of mask information and comprising one or more macrocells that can be selectively placed and interconnected to perform an electrical function.

JESD12-1B, 8/93
JESD99C, 12/12

cell compiler: A tool that automatically generates the physical layout to meet the specified parameters and that may generate a symbol and timing and functional models.

JESD12-1B, 8/93
JESD99C, 12/12

censored data: A set of data for which a portion of the test samples had testing discontinued prior to failing or survived until the end of the test.

JEP154, 1/08

centerline: A reference line on a control chart about which the chart points are expected to cluster in the absence of a special cause. It is usually set at the average, median, or mode of the points being plotted, or (for a tunable process) at an achievable target value (to detect deviations from the value thought most desirable).

EIA-557-B, 2/06

central processing unit; processing unit (CPU): A functional unit that consists of one or more processors and their internal storage. (Ref. ANSI X3.172.)

JESD100-B, 12/99

certified process: A process that, through demonstration and validation, has been determined to produce product capable of consistently achieving or exceeding customer requirements.

EIA-599-A, 6/98

CFF: See “cumulative fraction failing”.

C⁴D: See “conductivity-connected charge-coupled device”.

change, (product or process): An alteration to the product or process, which may be a major change or a minor change.

JESD46D, 12/11

NOTE 1 A major change is a change that may affect the form, fit, or function of the product or adversely affect the quality or reliability of the product.

NOTE 2 A minor change is a change that does not affect the form, fit, function, quality, or reliability of the product.

channel: (1) A thin semiconductor layer, between the source region and the drain region, in which the current is controlled by the gate potential.

JESD24, 7/85

(2) A region of semiconductor material in which current flow is influenced by a transverse electrical field.

JESD99C, 12/12

NOTE 1 A channel may physically be an inversion layer, a diffused layer, or bulk material.

NOTE 2 The type of channel, i.e., p-channel or n-channel, is determined by the type of majority carrier during conduction.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

channel: Both a set of physically discrete connections within the Wide I/O interface and a logically discrete, independently controlled partition of the Wide I/O interface.

JESD229, 12/11

NOTE The Wide I/O interface supports four physical and four logical channels. Each physical channel contains all the control, data, and clock signals necessary to independently control each of the four logical channels in the Wide I/O interface. Aside from a few global configuration options, each logical channel has its own set of mode registers, can have different DRAM pages open, can be independently clocked, and can even be in different power states. The physical channel also contains power and ground signals, but all power and ground signals on all physical channels must be at their appropriate levels for any portion of the Wide I/O device to operate correctly. The physical channel also contains a reset signal, but the Wide I/O interface defines reset to be per slice rather than per channel.

channeled gate array: A gate array configuration that contains a predetermined and dedicated area for logic interconnection.

JESD12-1B, 8/93
JESD99C, 12/12

channelless gate array: A gate array configuration that contains no predetermined and dedicated area for logic interconnection.

JESD12-1B, 8/93
JESD99C, 12/12

channel region (1) (of an IGFET): A control region through which the principal current passes and in which the concentration of principal-current charge carriers is determined by voltage applied to a gate, the principal current being the result of an applied drift field.

JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

(2) (of a JFET): A control region through which the principal-current charge carriers pass and whose cross-section is determined by the voltage applied to a gate, the principal current being the result of an applied drift field.

JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

characteristic: (1) A distinguishing feature of a process or its output on which variables or attributes data can be collected.

EIA-557-B, 2/06
EIA-599-A, 6/98
JEP131B, 4/12
JEP132, 7/98
JESD659B, 2/07

(2) An inherent and measurable property of a device. (Ref. IEC 134.)

JESD77D, 8/12
JESD99C, 12/12

NOTE Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear and may be expressed as a value for stated or recognized conditions.

(3) A set of related values, usually shown in graphical form. (Ref. IEC 134.)

JESD77D, 8/12
JESD99C, 12/12

characteristic life (for the Weibull distribution)(η): The time at which $F(t)$ equals $(1 - e^{-1})$ ($\approx 63.2\%$).

JESD74A, 2/07

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

characteristic, (static) (1) (of a bidirectional diode thyristor): A function, usually represented graphically, relating the thyristor voltage to the thyristor current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium.

JESD77D, 8/12

NOTE The word “static” is usually omitted except when a distinction between static and dynamic characteristics is necessary.

(2) (of a unidirectional diode thyristor): A function, usually represented graphically, relating the anode voltage to the anode current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium.

JESD77D, 8/12

NOTE The word “static” is usually omitted except when a distinction between static and dynamic characteristics is necessary.

characterization: A description of the characteristics of a product or process by mathematical modeling, design of experiments, or statistical data evaluation.

EIA-557-B, 2/06
JEP153, 1/08

NOTE Methods of statistical data evaluation are described in EIA-557 and JEP132.

charge-coupled device (CCD): A charge-transfer device that stores charge in potential wells and transfers this charge almost completely as a packet by translating the position of the potential wells.

JESD99C, 12/12

charge-coupled image sensor: A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

JESD99C, 12/12

charged-device model (CDM): A specified circuit characterizing an electrostatic discharge (ESD) event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

JESD22-C101E, 12/09

charge-handling capacity; full-well capacity: The maximum amount of charge that can be stored in a potential well and transferred without overflow into adjacent wells.

JESD99C, 12/12

charge packet: The portion of the total charge that is transferred from one position to the next position.

JESD99C, 12/12

charge pump: (1) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected in series with that source to make available a voltage greater than that of the source.

JESD99C, 12/12

NOTE This type of dc-to-dc converter is sometimes called a voltage doubler or, when several stages are cascaded, a voltage multiplier.

(2) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected to make available a voltage whose polarity is opposite to that of the source.

charge-regeneration stage (of a digital circuit): A region of a charge-transfer device that is used to refresh stored digital information.

JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

charge-transfer device (CTD): A device in which operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface or through the interconnections on the semiconductor surface.

JESD99C, 12/12

charge-transfer efficiency (CTE) (η): The fraction of the signal charge that is transferred from one storage region to the next storage region.

JESD99C, 12/12

charge-transfer inefficiency (CTI) (ε); incomplete charge-transfer coefficient: The fraction of the signal charge that fails to be transferred from one storage region to the next storage region.

JESD99C, 12/12

charge-transfer loss (δ): The fractional loss of signal charge that occurs when a charge packet is transferred from one storage region to the next storage region and that packet is preceded by one or more packets of zero charge.

JESD99C, 12/12

NOTE The loss of charge is that charge necessary to replenish all interface states or bulk traps that have emptied since the last passage of charge through the device. It is not charge that is left behind as it is in the case of charge-transfer inefficiency.

charge-transfer time (of a charge-transfer device): The time required to move a specified fraction of a charge packet from one storage region to the next.

JESD99C, 12/12

check list: A simplified listing of the specified criteria that may be checked off during an audit or inspection.

EIA-557-B, 2/06

check sheet: A form for data collection.

EIA-557-B, 2/06

chip (1) (semiconductor): A separated part of a wafer (or, in some cases, a whole wafer) intended to perform a function or functions in a device.

JESD77D, 8/12
JESD99C, 12/12

(2) (in a package): An area along an edge or corner where some material has broken off.

JESD27, 8/93
Rescinded 5/11

chip attach(ment): See “die bond”.

chip, beam-lead: A chip employing electrical terminations in the form of tabs extending beyond the edge of the chip for direct bonding to a mounting substrate.

JESD99C, 12/12

chip carrier: A package whose chip cavity or mounting area occupies a major fraction of the package area and whose terminals consist of metal pad surfaces (on leadless versions) or leads formed around the sides and under the package or out from the package (on leaded versions).

JESD99C, 12/12

NOTE The term “chip carrier” has been replaced by “quad flatpack” (for terminals on three or four sides) and “small-outline package” (for terminals on one or two sides).

chip enable (E): The input that, when true, permits active operation including the input and/or output of data and, when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

chip-enable input: A control input that, when active, permits operation of the integrated circuit and, when inactive, causes the integrated circuit to be in a reduced-power standby mode. (Ref. IEC 748-2.)

JESD100-B, 12/99

NOTE A chip-enable input is a clock or strobe input that significantly affects the power dissipation of the integrated circuit. For example, it may be the cycle control input of a dynamic memory or a power-reduction input of a static memory.

chip, face-down: A chip whose electrical terminations are on the side that is intended to be attached to the mounting substrate.

JESD99C, 12/12

chip, face-up: A chip whose electrical terminations are on the side opposite the one that is intended to be attached to the mounting substrate.

JESD99C, 12/12

chip, flip: A chip with bump contacts spaced around the device and intended for face-down mounting.

JESD99C, 12/12

chip-out (1) (in a package): An area where a crack has allowed a portion of the insulator to break away, leaving a void in the insulator at the metal interface.

JESD9B, 5/11

(2) (in a wafer or die): A visual anomaly that is a pit resulting from the removal of a volume of material by mechanical impact.

JESD22-B118, 3/11

chip-package interaction (CPI): (1) The interaction between the semiconductor package stresses and the semiconductor device.

JEP156, 3/09

NOTE Package stresses are caused by thermal, mechanical, or chemical mechanisms.

(2) For the purpose of JEP158, the interaction between stresses induced by the semiconductor package and the semiconductor chip whether alone or within the semiconductor 3-D chip stack.

JEP158, 11/09

chip-scale package: A package whose area is generally no greater than 120% of the area of the semiconductor device it contains.

JESD30E, 8/08

NOTE The package size does not necessarily change with changes in the size of the die.

chip select [S(n)(x)]: The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating, Z) for MOS and TTL devices and low (L) for ECL devices, and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the value of "a", "b", "c", etc.

JESD21-C, 1/97

chip-select input: A control input that, when active, permits operation of the integrated circuit and, when inactive, prevents input or output of data to or from the integrated circuit. (Ref. IEC 748-2.)

JESD100-B, 12/99

chip stack: A group of interconnected silicon chips stacked vertically to make a 3-D structure.

JEP158, 11/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

chip-to-chip interconnect; level D interconnect: The structure that connects one chip in a 3-D stack to another chip in that 3-D stack.

JEP158, 11/09

NOTE Examples of this structure include, but are not limited to, solder bumps and copper pads

chip-to-substrate-interconnect; level 1 (L1) interconnect: The structure that connects a chip to a substrate.

JEP156, 3/09

JEP158, 11/09

NOTE 1 Examples of this structure include, but are not limited to, solder bumps and copper columns.

NOTE 2 Level 1 (L1) interconnect is not associated with JP001 Foundry Level 1 Qualification (L1).

circuit element: Any constituent part of a circuit that contributes directly to its operation and performs a definable function.

JESD12-1B, 8/93#

JESD93, 9/05

JESD99C, 12/12

NOTE 1 Examples include transistors, resistors, capacitors, inductors, and interconnections.

NOTE 2 The definition in JESD12-1B excludes interconnections.

circuit element, active: A circuit element that contributes qualities to a circuit function other than those contributed by a passive circuit element, e.g., rectification, switching, gain, or conversion of energy from one form to another.

JESD93, 9/05

JESD99C, 12/12

NOTE 1 Examples include diodes, transistors, active integrated circuits, and light-sensing or light-emitting devices.

NOTE 2 Active physical circuit elements may also be used to act as passive physical circuit elements, e.g., to provide resistance and/or capacitance to a circuit function.

circuit element, parasitic: A circuit element that is an unavoidable adjunct of one or more other circuit elements.

JESD99C, 12/12

circuit element, passive: A circuit element primarily contributing resistance, capacitance, inductance, ohmic interconnection, or a combination of these to a circuit function.

JESD93, 9/05

JESD99C, 12/12

NOTE Examples include resistors, capacitors, inductors, passive filters, and interconnections.

circuit initialization: A sequence of stimuli that set internal nodes of a circuit to a predictable state.

JESD12-5, 8/88

circulating bias charge: Synonym for “bias charge”.

JESD99C, 12/12

CISC: See “complex-instruction-set computer”.

CK: See “input and output clock”.

CKE: See “clock enable”.

CL: See “clear (CL)”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

clamped package: A package for high-current devices, in the form of a cylinder with a flat, circular, high-current terminal on each end, that is intended to be clamped between two busbars acting as heat sinks.

JESD30E, 8/08

class: A categorization of similar characteristics for the purpose of reporting ppm nonconforming. Examples of classes include functional (ppm1), electrical (ppm2), visual/mechanical (ppm3), and hermetic (ppm4).

JESD16-A, 4/95

classification temperature: The maximum body temperature at which the component manufacturer guarantees the component moisture sensitivity level as noted on the caution and/or bar code label per J-STD-033.

J-STD-020D.1, 3/08

clear: To preset a storage or memory device to a prescribed state, usually that denoting zero. (Ref. IEEE Std 100.)

JESD100-B, 12/99

NOTE In the field of nonvolatile memories, “clear” conventionally means to set the outputs of the memory to the high logic level.

clear (CL): An input that, when true, causes all cells in the memory array to be cleared to their zero state.

JESD21-C, 1/97

clear algorithm (for a flash EEPROM): The timed sequence of signals necessary to clear the memory.

JESD100-B, 12/99

clearance distance: The shortest external distance measured through air from the anode terminal to the cathode terminal of a rectifier diode, or from the anode terminal to the cathode or gate terminal of a thyristor.

JESD4, 11/83

clear disturb: The corruption of data in one location caused by the clearing of data at another location.

JESD100-B, 12/99

clock cycle: The time period, generally derived from an oscillator, that is used for sequencing data flow and synchronizing one or more functions. (Ref. IEC 824.)

JESD100-B, 12/99

clock distribution network: The structure by which clock signals are distributed within a device.

JESD12-1B, 8/93
JESD99C, 12/12

clock driver: A driver intended for use with clock signals.

JESD99C, 12/12

clock enable (CKE): In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.

JESD21-C, 1/97

clock frequency, maximum ($f_{\max}$): The highest frequency at which a clock input of an integrated circuit can be driven while maintaining proper operation.

JESD12-1B, 8/93
JESD99C, 12/12

clock skew: The difference in the arrival times of a common clock edge at any two circuit elements.

JESD12-1B, 8/93
JESD99C, 12/12

C-mode: See “acoustic data, C-mode”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

CMOS-and-DMOS (C/DMOS) technology: A technology for combining complementary metal-oxide-semiconductor (CMOS) field-effect devices and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

JESD99C, 12/12

coaxial package: A transistor package designed to mount directly into coaxial lines.

RS-435, 4/76

cold plate: A heat absorber usually operating at some known or fixed temperature.

JESD51-1, 12/95
JESD51-13, 6/09

collected charge: The charge collected at a particular device node during and immediately after the passage of a particle.

JESD89A, 10/06

NOTE 1 This amount of charge is determined by measurement immediately after the passage of a particle.

NOTE 2 The amount of collected charge is dependent on the geometry and doping of the node, the particle mass, energy, and trajectory, and the density and type of material in the volume penetrated by the incident radiation.

collecting junction: A semiconductor junction in an operating condition in which the net flow of charge carriers of each type across the junction is in the direction from the region where they are minority carriers to the region where they are majority carriers, i.e., in the direction of the force resulting from the internal electric field.

JESD77D, 8/12

collection region (within a semiconductor device): A functional region that receives the principal current leaving the control region.

JESD77D, 8/12

collector (nonspecific): The overall combination of collector transition region, collector region, collector terminal, and the interface between them.

JESD77D, 8/12

NOTE This term should be used in this manner only when no confusion is likely to occur.

collector-base time constant ($\tau_b'C_c$): The product of the intrinsic base resistance and collector capacitance under specified small-signal conditions.

JESD10, 1/76

collector-base voltage, emitter open (V_{CBO}): The voltage between the collector and base terminals when the emitter terminal is open-circuited.

JESD10, 1/76
JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

collector cutoff current, base open (I_{CEO}):

collector cutoff current, base short-circuited to emitter (I_{CES}):

collector cutoff current, circuit between base and emitter (I_{CEX}):

collector cutoff current, resistance between base and emitter (I_{CER}):

collector cutoff current, voltage between base and emitter (I_{CEV}):

The dc current into the collector terminal when it is biased in the reverse direction* with respect to the emitter terminal, and the base terminal is, respectively,

- open-circuited.
- short-circuited to the emitter terminal.
- returned to the emitter terminal through a specified circuit.
- returned to the emitter terminal through a specified resistance.
- returned to the emitter terminal through a specified voltage.

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for npn transistors or negative for pnp transistors with respect to the emitter terminal.

collector cutoff current, emitter open (I_{CBO}): The dc current into the collector terminal when it is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited.

collector-emitter saturation voltage: See “saturation voltage, collector-emitter”.

collector junction (of a thyristor): The junction across which the polarity of the voltage reverses when switching occurs. (Ref. EIA-397.)

collector region, functional: A collection region that acquires principal-current charge carriers from a controlling base region through an associated collecting junction.

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal. In the normal operating mode, this functional region is located in the collector region; in the inverse operating mode, it is located in the emitter region.

collector region, physical: (1) A region through which a primary flow of charge carriers leaves the base. (Ref. 60 IRE 28.S1.)

(2) The physical region that is designed by the manufacturer to contain the collection region in the normal operating mode and, in a simple discrete transistor, is externally accessible by the designated collector terminal.

collector terminal (C, c): The specified externally available point of connection to the collector region.

color temperature: The temperature of a blackbody having the same visible color as that of a given non-blackbody radiator.

column address (CA): In an address-multiplexed DRAM, the address field that is captured by the column enable clock, CAS. When the column address numbering is significant for device operation, the addresses are numbered beginning with 0.

JESD10, 1/76
JESD77D, 8/12

JESD10, 1/76
JESD77D, 8/12

JESD77D, 8/12

JESD77D, 8/12

JESD10, 1/76

JESD77D, 8/12

JESD77D, 8/12

JESD77D, 8/12

JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

column enable (CAS; CE): An enable signal that on some dynamic RAMs actuates only the column-oriented internal circuits and the data input/output circuits. Most devices normally require the RAS signal to be present for the CAS signal to be effective. In some newer designs, however, special sequences of the RAS and CAS signals are used to actuate certain special device control functions. For devices that have one CAS per output, the CASs are numbered beginning with 0. For two-byte devices that have one CAS per byte, the CASs are designated LCAS and UCAS. LCAS affects DQ0–DQ7, and UCAS affects DQ8–DQ15. For devices that have more than two bytes and one CAS per byte and for all modules that have one CAS per byte, the CASs are numbered beginning with 0. CAS0 affects DQ0–DQ7, CAS1 affects DQ8–DQ15, CAS2 affects DQ16–DQ23, and CAS3 affects DQ24–DQ31.

JESD21-C, 1/97

combinational fault: A functional fault that is not affected by the sequence of the input stimuli.

JESD12-5, 8/88

combinational logic function: A logic function in which there exists one and only one resulting combination of states of the outputs for each possible combination of input states.
(Ref. ANSI/IEEE Std 91.)

JESD99C, 12/12

NOTE The words “combinative” and “combinatorial” have also been used in place of combinational.

common cause: A source of natural variation that affects all the individual values of the process output being studied. In control chart analysis it appears as part of the random process variation.

EIA-557-B, 2/06
JEP132, 7/98
JESD659B, 2/07

common-mode input voltage (V_{IC}): The average of the voltages at two input terminals of a circuit.

JESD99C, 12/12

common-mode input voltage range (V_{ICR}): The range of common-mode input voltage that, if exceeded, will cause the total harmonic distortion of the output signal resulting from the common-mode input to exceed a specified maximum value.

JESD99C, 12/12

common-mode output voltage (V_{OC}): (1) The average of the voltages at two output terminals of a circuit.

JESD99C, 12/12

(2) The ac voltage between two output terminals (or the output terminals and ground for circuits with one output) when ac signals of identical phase and amplitude are applied to the input terminals.

common-mode rejection ratio (k_{CMR} or CMRR): The ratio of the differential voltage amplification to the common-mode voltage amplification.

JESD99C, 12/12

common-mode voltage: The average voltage level of the two signals on a differential line.

JESD96, 4/04

common-source small-signal (forward transfer, input, output, reverse transfer) conductance (g_{fs} , g_{is} , g_{os} , g_{rs}): The real part of the corresponding common-source small-signal admittance y_{fs} , y_{is} , y_{os} , or y_{rs} .

JESD24, 7/85
JESD77D, 8/12

NOTE Symbols in the forms of g_{xx} and $y_{xx(\text{real})}$ are equivalent.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

common-source small-signal short-circuit forward transfer admittance (y_{fs}): The ac rms drain current divided by the ac rms gate-source voltage with the drain-source voltage held constant.

JESD24, 7/85
JESD77D, 8/12

NOTE The fact that the drain-source voltage is held constant implies that the drain terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit input admittance (y_{is}): The ac rms gate current divided by the ac rms gate-source voltage with the drain-source voltage held constant.

JESD24, 7/85
JESD77D, 8/12

NOTE The fact that the drain-source voltage is held constant implies that the drain terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit output admittance (y_{os}): The ac rms drain current divided by the ac rms drain-source voltage with the gate-source voltage held constant.

JESD24, 7/85
JESD77D, 8/12#

NOTE The fact that the gate-source voltage is held constant implies that the gate terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit reverse transfer admittance (y_{rs}): The ac rms gate current divided by the ac rms drain-source voltage with the gate-source voltage held constant.

JESD24, 7/85
JESD77D, 8/12

NOTE The fact that the gate-source voltage is held constant implies that the gate terminal is ac short-circuited to the source terminal.

commutation: The transfer of unidirectional current between rectifier circuit elements that conduct in succession.

JESD282-B, 4/00

companding DAC: A digital-to-analog converter whose transfer function complies with a compression or expansion law.

JESD99C, 12/12

NOTE 1 The corresponding analog-to-digital converter normally consists of such a companding DAC and additional external circuitry.

NOTE 2 The compression or expansion law is usually a logarithmic function, e.g., A-law or μ -law.

comparator, differential voltage: A device that compares an input voltage with a reference voltage and indicates which is greater by means of a digital output.

JESD99C, 12/12

comparison unit (CU): (1) The change in a temperature-sensitive parameter divided by the change in a dependent heating-condition parameter.

JESD51-1, 12/95

(2) For an integrated circuit, the change in temperature-sensing diode forward junction voltage under measurement conditions divided by the change in heating current, $\Delta V_F / \Delta I_H$. This allows for thermal comparison of one device to another when the heating voltage remains constant.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

complementary integrated circuit technology: The technology, as applied to integrated circuits, whereby active elements of both polarities are fabricated as single-chip elements on or within the same substrate.

JESD99C, 12/12

NOTE For example, a complementary bipolar semiconductor integrated circuit is one that employs both npn and pnp bipolar transistors in the same semiconductor substrate, and a complementary MOS integrated circuit is one that employs both n-channel and p-channel field-effect transistors in the same semiconductor substrate.

complementary metal-oxide semiconductor (CMOS) technology: A technology for combining p-channel and n-channel metal-oxide-semiconductor field-effect transistors in a single-chip integrated circuit.

JESD99C, 12/12

complete data: All available data from all units in the stress test, including those in the failure set.

JESD37, 10/92

complex-instruction-set computer (CISC): A microcomputer or microprocessor that performs multiple tasks per complex instruction, usually requiring multiple clock cycles.

JESD100-B, 12/99

compliance: (1) **(general):** Conformity in fulfilling official requirements.

Merriam-Webster's
Collegiate Dict.

(2) **(of test equipment):** The maximum current- or voltage-forcing capability of the test equipment.

JESD35-A, 4/01

compliance, current (of a digital-to-analog converter) ($\Delta I_{O(op)}$): The permissible range of output current within which the specifications are valid.

JESD99C, 12/12

compliance, voltage (of a digital-to-analog converter) ($\Delta V_{O(op)}$): The permissible range of output voltage within which the specifications are valid.

JESD99C, 12/12

component: (1) A constituent part.

JESD77D, 8/12

JESD99C, 12/12

NOTE 1 Examples include source and drain regions as components of transistors, lead frames and dice as components of packaged integrated circuits, resistors and integrated circuits as components of printed circuit boards, motherboards as components of computers, LCD screens as components of monitors, ac and dc components of complex waveforms, and loops and algorithms as components of software programs.

NOTE 2 Unless the context identifies the thing of which a component is a part, a descriptive prepositional phrase identifying the thing should follow the word "component".

NOTE 3 The classification of an item as a device or as a component depends upon the intention of the owner at the time of classification.

J-STD-609.01, 2/11

(2) An individual part such as a connector, capacitor, integrated circuit, socket, multichip module, hybrid circuit, etc.

component (of a hybrid integrated circuit): A part that is mounted within the package and that contributes to the composition of the circuit.

JESD99C, 12/12

NOTE For electronic components, a distinction is made between integrated components and discrete components.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

component, active (of a hybrid integrated circuit): A component in which at least one circuit element is an active circuit element.	JESD99C, 12/12
component, discrete (of a hybrid integrated circuit): A discrete device that serves as a component of a hybrid integrated circuit.	JESD99C, 12/12
component, integrated (of a hybrid integrated circuit): An integrated circuit, completed or partially completed, that serves as a component of a hybrid integrated circuit.	JESD99C, 12/12
component, passive (of a hybrid integrated circuit): A component in which all circuit elements are passive.	JESD99C, 12/12
component problem: Any problem related to the supplier's component that causes failure during, or interruption to, the customer's production flow or failures of their products in the final application, e.g., a) administrative problems (wrong product, wrong quantity, packing/materials, orientation, date code, paperwork, shipping damage, shipping error, labeling, etc.), b) electrical problems (functional, parametric, timing, continuity, programming, etc.), and c) visual/mechanical problems (marking, leads, package body, solderability, contamination, etc.).	JESD671B, 6/12
component, (semiconductor): A packaged semiconductor device.	IPC/JEDEC-9702, 6/04 JEP140, 6/02 JESD22-B104C, 11/04 JESD22-B110A, 11/04 JESD22-B111, 7/03 JESD89A, 10/06
concave warpage: Negative (-) warpage resulting in the package corners being farther from the contact plane than the center of the bottom surface of the package substrate.	JESD22-B112A, 10/09
concentric: Having a common center point.	JESD9B, 5/11
conducting [conduction] period (of a rectifier circuit element): The part of an alternating-voltage cycle during which the current flows in the forward direction. NOTE The forward period is not necessarily the same as the conducting period because of circuit parameters and semiconductor rectifier diode characteristics.	JESD282-B, 4/00
conductive material: A material that has a surface or volume resistance less than 1×10^4 ohms. NOTE A conductive material is not necessarily antistatic.	JESD625B, 1/12
conductivity-connected charge-coupled device (C⁴D): A charge-coupled device that uses doped regions between the potential wells and hence becomes a hybrid between the charge-coupled device and a bucket-brigade device.	JESD99C, 12/12
configure: Synonym for “program”.	JESD32, 6/96

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

connection, electrical (within a semiconductor device): An electrically conducting element that functions as a pathway between other elements, including terminals, and whose primary purpose is to conduct electric current in a confined manner.

JESD99C, 12/12

NOTE The connection may either consist of a separate conductive entity such as a wire or metallic film or be an integral part of the body.

connect (state): A state in a switch device characterized by a minimal series impedance of the designated electrical path.

JESD73, 6/99
JESD73-1, 8/01
JESD73-2, 8/01
JESD73-3, 8/01
JESD73-4, 11/01

constant-current threshold voltage ($V_{T(ci)}$): The gate-source voltage at which the drain current is equal to a constant current, appropriate for a given technology, times the ratio of gate width (W) to gate length (L). $V_{T(ci)}$ can be calculated using

JESD28-A, 12/01#
JESD60A, 9/04
JESD90, 11/04

$$V_{T(ci)} = V_{GS} \text{ (at } I_D = I_{D0} W/L \text{)}$$

where W and L are the gate width and gate length as printed on the wafer.

NOTE I_{D0} is selected for a given technology such that $V_{T(ci)}$ is in the subthreshold region of the device. For N-MOSFET devices, JESD28-A suggests 0.1 μA ; for P-MOSFET devices, JESD60 suggests $-0.025 \mu\text{A}$.

contact, bump; ball contact; raised pad; pedestal: (1) A contacting pad that rises substantially above the surface level of the chip.

JESD99C, 12/12

(2) A raised pad on the substrate that contacts a flat land area of the chip.

contact plane: A plane parallel to the reference plane passing through the lowest contact point on the package substrate.

JESD22-B112A, 10/09

containment: Interim action(s) taken to minimize the effects of component problems on customers until corrective actions are implemented.

JESD671B, 6/12

content-addressable memory (CAM): A memory that responds with all the data in a storage zone if a portion of that data matches the data used for addressing the memory. (Ref. IEC 748-2.)

JESD100-B, 12/99

continuous improvement: The methodology whereby quality improvement tools (e.g., statistical process control (SPC), Ishikawa diagram, design of experiments (DOE), etc.) are applied to a process to improve measurable attributes (e.g., repeatability, efficiency, predictability, etc.).

JEP132, 7/98

contrast (of a mark on a device): The difference in luminance (“brightness”) between the mark and the surrounding device surface.

JESD22-B114A, 5/11

NOTE Contrast is typically quantified by comparison of minimum and maximum reflectance values

control: A corrective action process based on feedback.

JEP131B, 4/12

control bus: A bus carrying the signals that regulate system operations. (Ref. ANSI X3.172.)

JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions**References**

control-charge region (within a semiconductor device): A functional region that contains the controlling charge and that may or may not be the path for the principal current.

JESD77D, 8/12

control chart: A graphic representation of a process characteristic showing plotted values of some statistic gathered from that characteristic, a central line, and one or two statistically derived control limits. Two basic uses are to determine whether a process has been operating in statistical control and to aid in maintaining statistical control.

EIA-557-B, 2/06
JEP132, 7/98

control current: Current at the control terminals.

JESD14, 11/86

controllability: The ability of a node to be established at specific logic state(s) by applying stimuli to the circuit's externally accessible node(s).

JESD12-5, 8/88

controlled edge: The output signal edge that is locked to the phase-locked loop (PLL) trigger reference.

JESD65B, 9/03

controlled SPCM: A semiconductor power-control module (thyristor SPCM, transistor SPCM, thyristor-diode SPCM, or transistor-diode SPCM) with internal control-signal processing circuitry that may have provisions for external adjustment.

JESD14, 11/86

control limits: The maximum allowable variation of a process characteristic due to common causes alone. Variation beyond a control limit may be evidence that special causes are affecting the process. Control limits are calculated from process data and are usually represented as a line (or lines) on a control chart. They are not to be confused with engineering specification limits.

EIA-557-B, 2/06
JEP132, 7/98
JESD659B, 2/07

control loop: A corrective action system based on a feedback procedure.

EIA-557-B, 2/06

control region (within a semiconductor device): A functional region through which the principal-current charge carriers flow and are controlled in the manner for which the device is intended.

JESD77D, 8/12

control terminals: The terminals to which the external control signal is applied.

JESD14, 11/86

control voltage: The voltage at the control terminals.

JESD14, 11/86

convection oven: A controlled-temperature chamber in which the heat is transferred by air flow, rather than by conduction or radiation.

JEP153, 1/08

NOTE The chamber must be capable of maintaining specified temperatures over the entire working area.

conversion code (1) (of an analog-to-digital converter): The set of correlations between each of the fractional parts of the total analog input range and the corresponding digital output codes.

JESD99C, 12/12

NOTE Examples of analog-to-digital converter output code formats are straight binary, 2s complement, and binary-coded decimal.

(2) (of a digital-to-analog converter): The set of correlations between each of the digital input codes and the corresponding analog output values.

JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.