

JEDEC STANDARD

Test Method for Beam Accelerated Soft Error Rate

JESD89-3B

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Test Method for Beam Accelerated Soft Error Rate

(From JEDEC Board Ballot JCB-20-63, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This test method is offered as a standardized procedure to determine the terrestrial cosmic ray (i.e., high energy and thermal neutron) Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g., flip-flops) by measuring the error rate while the device is irradiated in a neutron or proton beam of known flux.

JESD89 describes considerations for executing such an estimate from data collected with this method. Refer to JESD89 for other background on the motivation for requirements in this test method and guidance for those elements left to the discretion of the tester. The results of this accelerated test can be used to estimate the terrestrial cosmic ray induced SER for a given terrestrial cosmic ray radiation environment.

NOTE 1 This test cannot be used to project alpha-particle-induced SER.

NOTE 2 Special considerations apply to devices that are more than memory arrays and/or bistable logic elements. These can preclude the application of this test procedure. Refer to JESD89 for further discussion on some examples.

2 Applicable documents

JESD89	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-1	Test Method for Real-Time Soft Error Rate
JESD89-2	Test Method for Alpha Source Accelerated Soft Error Rate

3 Apparatus

The performance of this test requires equipment that is capable of providing the particular test conditions to which the test samples will be subjected.

3.1 Vehicle design and operation

The biasing and operating schemes shall consider the limitations of the devices and shall not overstress the devices or contribute to thermal runaway.

3.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under test (e.g., improper heat dissipation).

3 Apparatus (cont'd)

3.3 Power supplies and signal sources

Instruments (e.g., oscilloscopes) used to set up and monitor power supplies and signal sources shall be calibrated and have long-term stability. Electrical noise shielding shall be in place to allow for accurate test results.

3.4 Scattered/stray radiation

- Special attention should be taken with respect to the effects of scattered radiation from the beam on the test setup. Technical personnel operating the facility should be consulted in terms of the relative flux of the forward and backward scattering distribution of the beam. They should also be consulted on effectiveness of shielding materials for the main beam and scattered beam attenuation.
- Spectral purity (e.g., energy and species) is also important. Scattering of the primary beam with material upstream from the DUT can generate additional radiation. Technical personnel operating the facility should be able to provide an estimate of the relative intensity of this stray radiation and effective means to shield it from the experiment. For example, thermal neutrons will be present in any high energy neutron beam, but use of material rich in B-10 can act as an effective attenuator (refer to JESD89 for details). This enables distinction of device effects due to high energy neutrons from those due to thermal neutrons.
- The results of the testing should be due to radiation effects on the DUT and not from interaction of radiation with other components in the test. In particular, power supplies can be vulnerable to radiation-induced avalanche breakdown. Sensitive electronic circuits in the tester and any device on the DUT board (e.g., buffers or registers) can also be affected. Any of these components should be moved as far from the primary and scattered beam as possible or appropriate shielding should be used.
- Assure that the tester and power supply are not affected by scattered radiation from the beam before conducting tests in a new facility or before conducting tests with a new tester setup (including modified shielding of the tester). To assure this, position and shield the tester exactly as during actual tests except for the DUT that shall be positioned outside the beam or shall be shielded from the beam. With the beam on and the DUT shielded or otherwise not exposed to the beam, test the DUT. Tester setup verification is successful if no failures are observed. Unless otherwise specified, this tester setup verification test shall last as long as a typical test.
- Care shall be taken to prevent upsets from stray signals or noise in the cables to the DUT. A tester readiness check shall be performed as part of the test sequence to assure electrical noise immunity, see section 4.3.1.

4 Terms and definitions

absolute maximum rated temperature: The maximum junction or ambient temperature of an operating device as listed in its data sheet and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated voltage: The maximum voltage that may be applied to a device and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

critical charge (Q_c): The minimum amount of collected charge that will cause a device node to change state and result in a single event upset (SEU).

DUT: Device under test.

ECC: Error correction code, sometimes called error detection and correction (EDAC).

failure cross section: The numbers of failures detected per fluence .

fluence (of particle radiation incident on a surface): The total amount of particles incident on a surface in a given period of time, divided by the area of the surface and represented by the upper-case symbol Φ in this standard.

NOTE This fluence is usually expressed in particles per unit area (e.g., n/cm²). Fluence is the product of flux multiplied by exposure time.

flux: The time rate of flow of particles incident on a surface, divided by the area of that surface, and represented by the symbol $\dot{\Phi}$ in this standard. It is the time rate of change of the fluence Φ : $\dot{\Phi} = d\Phi/dt$.

NOTE 1 Flux is usually expressed in particles per unit area, per unit time (e.g., n/cm²h).

NOTE 2 The term “flux” is used in this standard whereas other standards might use the term “flux density” for the same meaning.

golden part: A sample used to monitor the consistency of the beam and tester setup.

maximum operating voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

minimum operating voltage: The minimum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

multiple-bit upset (MBU): A single event that induces upset of multiple-cells where two or more of the upsets occur in the same logical word (or frame/column/sector, etc. for FPGAs).

NOTE An MBU is a logical manifestation of a single event.

4 Terms and definitions (cont'd)

multiple-cell upset (MCU): A single event that induces several cells (e.g. memory cells or flip-flops) in an IC to flip their state at one time.

NOTE 1 The induced errors are usually, but not always, physically adjacent. This does not imply logical adjacency, since this will depend on how cells are placed and routed (interleaved).

power cycle soft error (PCSE): a single event effect that is not corrected by repeated reading or writing but can be corrected by removal and reapplication of power.

single-event burnout (SEB): An event in which a single energetic-particle strike induces a localized high-current state in a device that results in catastrophic failure.

single-event effect (SEE): An event initiated by a particle strike that causes a transient voltage or current pulse. Various types of SEE are shown in Figure 1 of JESD89.

single-event functional interrupt (SEFI): A single event effect (SEE) that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not result in permanent damage (i.e., hard error).

NOTE A SEFI is often associated with an SBU/MBU in a control bit or register, whereas an SEL is caused by the turn-on of a parasitic thyristor. Many SEFI events can be cleared with a component reset operation (see RSE). In cases where resetting some configuration registers requires a complete power cycle of the device, it can be difficult to distinguish between a SEFI and an SEL. A SEFI event does not necessarily result in an extended increase in operational current like a high current SEL.

single-event gate rupture (SEGR): An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

single-event hard error (SEHE): A hard error caused by a single event radiation strike.

single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle inducing a parasitic thyristor to turn on and remain in a fixed state regardless of inputs, until the device is power cycled.

NOTE 1 Some SEL events result in a measureable current increase (e.g. latch-up of an IO circuit). Some SEL events may result in a difficult to detect increase in current (micro-SEL) compared to the quiescent current of the entire component (e.g. latch-up of memory cells within a common well).

NOTE 2 A high current SEL may cause permanent damage to the component and result in a hard error. Micro-SEL events are typically non-destructive due to the low current draw and can be cleared by power cycling.

single-event transient (SET): A time dependent radiation induced spurious current or voltage signal on a circuit node. A digital SET (DSET) occurs when an SET in a combinational logic gate (along data or control paths) propagates and is latched to create an error (SEU) in the output of a sequential element. An analog SET (ASET) is a spurious signal in an analog circuit (e.g. a spurious signal on an IO pin, etc.) that causes an erroneous output.

4 Terms and definitions (cont'd)

single-event upset (SEU): An error in a circuit that is not permanent (i.e., not a hard error) caused by a state change of a latch, flop, memory cell or other bistable element from a single energetic particle strike. The energetic strike can occur directly on the circuit element or propagate to that circuit (see SET).

NOTE In many documents and publications, SEU is used to include other soft errors, such as SEFI and SEL.

soft error: An erroneous output signal from a circuit that can be corrected by performing one or more normal functions of the device (e.g., retrying operation, rewriting data, power cycling, etc.) In many documents and publications, soft error is synonymous with SEU.

NOTE 1 The term refers to an error caused by radiation or electromagnetic noise (e.g. electromagnetic pulse from a nuclear event) and not to an error associated with a physical defect introduced during the manufacturing process. For the purposes of this standard, soft errors are considered to be single particle radiation induced events and not due to other sources, such as signal integrity or noise.

NOTE 2 The terms soft error and soft error rate (SER) have been adopted by the commercial IC industry while other terms, such as SEU, SEFI, etc.. are typically used by the avionics, space, automotive, functional safety and military electronics communities.

NOTE 3 The term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).