

JEDEC STANDARD

Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices

JESD89A

(Revision of JESD89, August 2001)

OCTOBER 2006

(Reaffirmed: JANUARY 2012)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2012
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

CONTENTS

	Page
Foreword	iii
Introduction.....	iii
1 Scope	1
2 Terms and definitions	1
3 Test equipment and software requirements	5
3.1 Test equipment.....	5
3.2 Test plan.....	6
3.3 Test conditions	8
3.4 Setup procedure	10
3.5 General testing specifications	11
3.6 Data collection	11
3.7 Considerations for testing non-memory components	11
4 Real-time (unaccelerated and high-altitude) test procedures	15
4.1 Background.....	15
4.2 Test facilities and equipment	16
4.3 Testing procedures	18
4.4 Differences in real-time ser tests and actual end-user observed fail rates.....	20
4.5 Final report.....	20
5 Accelerated alpha particle test procedure	22
5.1 Background.....	22
5.2 Alpha particle environment.....	23
5.3 Packaging for alpha particle testing.....	23
5.4 Alpha particle sources.....	24
5.5 Basic test methodology	26
5.6 Test procedure and results	27
5.7 Interferences.....	30
5.8 Final report.....	32
6 Accelerated terrestrial cosmic ray test procedures	33
6.1 Background.....	33
6.2 Test facilities.....	34
6.3 Basic test methodology	34
6.4 Basic test procedure	34
6.5 Beam parameters.....	35
6.6 Fundamental quantities: seu cross-section and seu rate	36
6.7 Interferences.....	42
6.8 Final report.....	43

**MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC
RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES**

CONTENTS (cont'd)

	Page
7 Accelerated thermal neutron test procedures	44
7.1 Background	44
7.2 The terrestrial thermal neutron environment.....	46
7.3 Packaging for thermal neutron testing	46
7.4 Thermal neutron sources.....	47
7.5 Basic test methodology	49
7.6 Test procedure and results	49
7.7 Interferences.....	52
7.8 Final report.....	53

Annexes

A (normative) Determination of terrestrial neutron flux.....	55
B (normative) Counting statistics	70
C (normative) Real-time testing statistics	71
D (informative) The alpha particle environment	75
E (informative) Neutron and proton test facilities	79
F Bibliographic References.....	82
G Differences Between JESD89A and JESD89	84

Foreword

This specification defines the standard requirements and procedures for terrestrial soft error rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation, dominated by high- and low-energy neutron-induced reactions, and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device's SER is complete, **only** when an unaccelerated test is done under actual use conditions, **or** accelerated SER data for the alpha-particle component, the high-energy cosmic-radiation component, and if necessary, the thermal neutron component (see 7 for details) has been obtained and extrapolated to the use conditions.

Annexes D and E are informative; Annexes A, B, and C are normative.

Introduction

Soft errors are nondestructive functional errors induced by energetic ion strikes. Soft errors are a subset of single event effects (SEE), and include single-event upsets (SEU), multiple-bit upsets (MBU), single-event functional interrupts (SEFI), single-event transients (SET) that, if latched, become SEU, and single-event latchup (SEL) where the formation of parasitic bipolar action in CMOS wells induce a low-impedance path between power and ground, producing a high current condition (SEL can also cause latent and hard errors).

In general, soft errors may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by highly ionizing secondary particles produced from the reaction of both thermal and high-energy neutrons with component materials.

There are two fundamental methods to determine a product's SER. One is to test a large number of actual production devices for a long enough period of time (weeks or months) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. This is generally referred to as a real-time or unaccelerated SER testing. Real-time testing has the advantage of being a direct measurement of the actual product SER requiring no intense radiation sources, extrapolations to use conditions, etc. (provided the test is performed in a building location similar to the actual use environment - see A.5). However, real-time testing does require an expensive system capable of monitoring hundreds or thousands of devices in parallel, for long periods of time.

The other method commonly employed to allow more rapid SER estimations and to clarify the source of errors is accelerated-SER (ASER) testing. In ASER testing, devices are exposed to a specific radiation source whose intensity is much higher than the ambient levels of radiation the device would normally encounter. ASER allows useful data to be obtained in a fraction of the time required by unaccelerated real-time testing. Only a few units are needed and complete evaluations can often be done in a few hours or days instead of weeks or months. The disadvantages of ASER are that the results must be extrapolated to use conditions and that several different radiation sources **must** be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray-neutron events.

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

(From JEDEC Board ballot JCB-06-63, formulated under the cognizance of the JC-13.4 Subcommittee on Radiation Hardness: Assurance and Characterization.)

1 Scope

This standard specification covers soft errors due to alpha particles and low and high-energy atmospheric neutrons. 3 covers test methods and issues common to all test types, 4 covers real-time or unaccelerated measurements, 5 covers accelerated soft error rate test procedures related to alpha particles, 6 covers accelerated soft error rate test procedures related to high-energy neutron reactions (>1 MeV), and 7 covers test procedures for thermal neutron reactions with ^{10}B .

This specification defines the standard requirements and procedures for terrestrial soft error rate (including real-time and accelerated) testing of integrated circuits and a standardized methodology for reporting the results of the tests.

The procedures apply to components including memory and logic.

Warning: These tests may involve hazardous materials, operations, and equipment. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and to determine the applicability of regulatory limitations prior to use.

2 Terms and definitions

ATE: Automatic test equipment

component: A packaged die or integrated circuit.

NOTE This may be either a test vehicle or an actual product.

collected charge: The charge collected by a particular device node during the passage of a particle.

NOTE The collected charge is dependent on the geometry and doping of the node, the particle mass, energy, and trajectory, and the density and type of material in the volume being penetrated by the incident radiation.

critical charge: The minimum amount of collected charge that will cause a device node to change state.

device, electronic: synonymous with component or microcircuit

2 Terms and definitions (cont'd)

differential flux: The time rate of fluence per unit energy, the rate of the quantity of radiation, particle fluence, per unit area incident on a surface per unit energy.

NOTE 1 Differential flux is usually expressed in particles per unit area per unit energy per unit time, e.g., $n/(cm^2 \text{ MeV hr})$.

NOTE 2 The term differential flux in this standard is synonymous with spectral flux density used in other publications.

DUT: Device under test.

ECC: Error correction code, sometimes called error detection and correction (EDAC).

FITs: Failures in time; the number of failures per 10^9 device-hours.

fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface. NOTE This fluence is usually expressed in particles per unit area (e.g., N/cm^2).

flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.

NOTE 1 Flux is usually expressed in particles per unit area, per unit time (e.g., N/cm^2h).

NOTE 2 The term “flux” is used in this standard whereas other standards might use the term “flux density” for the same meaning.

hard error: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events).NOTE The error is “hard” because the data is lost and the component or device no longer functions properly, even after power reset and re-initialization.

multiple-bit upset (MBU): A multiple-cell upset in which two or more error bits occur in the same word.

NOTE An MBU cannot be corrected by a simple single-bit ECC.

multiple-cell upset (MCU): A single event that induces several bits in an IC to fail at one time.

NOTE The error bits are usually, but not always, adjacent.

process: A combination of people, procedures, methods, machines, materials, measurement equipment, and/or environment for specific work activities to produce a given product or service.

NOTE For the purposes of this standard the process is specifically the manufacturing steps and methodologies used to fabricate an IC.

2 Terms and definitions (cont'd)

product: A component or service sold to satisfy a particular customer application.

NOTE For the purposes of this standard a product is a complete integrated circuit sold to satisfy a particular customer application.

radiation: Energy emitted in the form of electromagnetic waves or moving nuclear particles.

NOTE For purposes of this standard the primary radiation of concern is ionizing and includes protons, electrons, alpha particles, and nuclear reaction products.

real-time soft error rate (RTSER): Soft error rate measurement technique under a naturally occurring alpha particle and neutron environment using a large number of devices to obtain a statistically significant error count. This is in contrast to an accelerated SER test where an intense radiation source is used on a single, or small number of devices. RTSER error counts can be increased by using a higher neutron flux at higher altitudes, but for the purposes of this specification, the term accelerated is reserved for intense radiation sources that do not occur in natural terrestrial environments. System SER (SSER) is another term that is often used and is considered synonymous with RTSER.

sensitive volume: A region, or multiple regions, containing nodes whose states can be changed by incident radiation.

NOTE The sensitive volume is determined by the angle of the incident radiation, the mass and energy of the incident particles, and the density and type of material in the volume being penetrated by the incident radiation.

single-event effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.

NOTE Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE) and single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).

single-event functional interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).

NOTE A SEFI is often associated with an upset in a control bit or register.

2 Terms and definitions (cont'd)

single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.

NOTE 1 SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

NOTE 2 An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

single event transient (SET): A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by a single energetic particle strike.

single-event upset (SEU): A soft error caused by the transient signal induced by a single energetic particle strike.

single-event upset (SEU) cross-section: the number of events per unit fluence. For device SEU cross-section, the dimensions are area per device. For bit SEU cross-section, the dimensions are area per bit.

single-event upset (SEU) rate: the rate at which single event upsets occur.

soft error, device: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell.

NOTE 1 As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.

NOTE 2 Soft errors can be generated from SEU, SEFI, MBU, MCU, and or SET. The term SER has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc.. are typically used by the avionics, space and military electronics communities.

NOTE 3 The term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).

soft error rate (SER): The rate at which soft errors occur.

storage element: A circuit or device that can be programmed to hold (or store) different states. For example, a DRAM cell, that can store charge (or not) on a capacitor. An SRAM cell or a flip-flop is another example.

test vehicle: A circuit or IC designed for the purpose of evaluating one or many device characteristics. For the purposes of this document, the characterization would be the soft error sensitivity of a particular process technology. But the test vehicle can incorporate other structures used to characterize different parameters, such as yield, speed, voltage margin, etc.

NOTE This test vehicle is not typically a product but is a dedicated component or section of an IC chip designed to be used to extrapolate to the SER of a product.

3 Test equipment and software requirements

3.1 Test equipment

3.1.1 ATE hardware

The automatic test equipment (ATE) hardware used for testing may be conventional electronic test gear or custom-built equipment. The ATE must be able to tolerate stray radiation and potentially poor quality power. So the use of uninterruptible battery-backed power supplies is recommended.

The ATE hardware must be capable of exercising the DUT over the range of operating conditions such as power supply voltage, access cycle speed and temperature that are specified in the test plan. Proper operation of the ATE under all of these operating conditions must be rigorously confirmed prior to the beginning of testing with a radiation source. The use of cabling to connect the DUT and test equipment, power supply accuracy at the DUT, and the exposure of the ATE to scattered radiation during testing should all be considered.

For accelerated testing with a high-intensity radiation source, the ATE is generally designed to hold a small number of DUTs at a time while they are irradiated. The ATE for field-testing, also known as real-time testing, is designed to hold a large number of DUTs while they are being irradiated, typically by the unaccelerated environmental exposure.

The ATE for use at a neutron or proton beam facility must be capable of remote operation since the operators will be shielded in the control room during an exposure. Cabling between the control room and beam station may be provided by the beam facility or be the responsibility of the experimenter. If the ATE is constructed as a holder and a separate electronics package to exercise the DUT, the cabling between them must be carefully designed and constructed to minimize the potential for errors during operation. Test cables should be short enough to allow sufficient test speeds without electrical noise problems.

Careful coordination with the beam facility prior to arrival can save a great deal of setup time. In general, the physical dimensions, accessibility and power availability at the test facility should be carefully checked before making a trip. The ATE must be rugged enough to withstand shipping to the test site and to be reassembled in a reasonable time.

In addition to the above, the following features are desirable,

- 1) The ability to adjust and monitor the temperature of the DUT.
- 2) Monitoring power supply current compliance to check for latchup.
- 3) Operation at, or near, the rated DUT clock speed if test performed in dynamic mode.
- 4) The ability to record particle fluence for each test if electronic data access from a detection system is provided by the test facility (this enables each test run to store the fluence with the data file).

3.1 Test equipment (cont'd)

3.1.2 ATE software

The ATE software creates the proper conditions for the test, and identifies, records and corrects errors as they are detected. Operation of the device with good fault coverage is required. When designing the test system, the experimenter should understand the portions of the die, signal path, and latching circuits of the device being tested in order to arrive at a quantitative result. The fraction of time the device is in an SEE susceptible mode and what fractions of the DUT's susceptible elements are not tested should be known. Complex devices do not always permit easy testing access.

The ATE software should be capable of

- 1) Controlling device initialization and rudimentary functional checks.
- 2) Device operation in dynamic or static operation, as required by the test plan.
- 3) Resetting the DUT during irradiation or real-time testing.
- 4) Error detection and logging, including the time that the error was detected. It is important during error detection that new errors are not omitted or that corrections are made for system dead time.

In addition to the characteristics listed above, the following features are also desirable

- 1) Bit error mapping and data processing, storage and retrieval for display.
- 2) Applicability to a variety of device types.
- 3) High-speed operation and a high duty factor.
- 4) Real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing.
- 5) The ability to do preliminary data analysis while the test is in progress. This feature is desirable for modification / optimization of test procedures in light of the data being collected.
- 6) Reliable audit path for data collection to allow correlation of experimental notes and collected data from the ATE.
- 7) Recording the particle fluence, either automatically acquired from the test facility or manually entered.

3.2 Test plan

A test plan shall be developed to support each test. This test plan will serve as a guide for the procedures and decisions to be made during the irradiation period. In most cases the test plan cannot be followed exclusively, as adjustments must be made during the course of testing based on equipment performance, observations and other factors.

3.2 Test plan (cont'd)

For all soft error testing it is necessary to accurately measure the following:

- 1) Particle fluence at the DUT, either by estimation using Annex A in the case of real time SER (RTSER) testing or measurement in the case accelerated SER testing.
- 2) Number of storage elements that are subject to upset,
- 3) Number of upsets that occur in each storage element.

Measurement of the particle fluence depends on the test setup and is a matter of good laboratory practice and metrology. The number of storage elements, and the number of upsets in them caused by irradiation is easy to assess for a memory component, but may be much harder to determine for other types of components such as microprocessors or FPGAs. Whereas each storage element is generally visible in a memory, other types of components may have large numbers of inaccessible elements, particularly when they are being tested without knowledge of the proprietary internal structure. For this reason, the comparison of soft error rates for non-memory devices following even slightly different testing procedures is generally not meaningful.

A minimal test plan includes:

- 1) Description of the radiation flux to be used for testing, including calibration in the case of accelerated SER, or geographic description of the test location in the case of RTSER (see A for details).
- 2) For each DUT, the number of samples, supply voltages and required error counts.
- 3) Specification of the data to be collected for each exposure.
- 4) Test procedures for each phase of testing.

Minimum accelerated beam or alpha particle source test procedure:

- 1) Setup and checkout the ATE operation
- 2) Dosimetry calibration for beam testing or alpha particle source calibration information (see 5.4.2).
- 3) Check against reference DUT from previous testing for beam testing.
- 4) Initial test run for DUT to confirm exposure rate.
- 5) Data collection for each DUT, at planned supply voltages.
- 6) Final test using the same conditions as step 4 to verify consistency of results.
- 7) Final dosimetry and setup checks using the reference DUT for beam testing.

Steps 4 through 6 are repeated for each DUT type to be tested.

Minimum real-time test procedure:

- 1) Setup and check ATE operation
- 2) Data acquisition phase, typically lasting several weeks or months, depending on the sample size and DUT sensitivity.
- 3) Final setup checks.

After testing is completed a final report is written describing the DUT error rate for each of the test conditions. The requirements for what data and parameters to include in the final report are described at the end of 4, 5, 6, and 7.

3.3 Test conditions

Test conditions for soft error testing are often limited by the capabilities of the portable ATE used to cycle the DUT.

3.3.1 Test pattern

The basic data pattern for all memory circuits is a logical checkerboard, alternating by address and bit. If detailed layout information for the DUT is available, a physical checkerboard is also useful. A determination of the best test pattern is left to the discretion of the experimenter, but must be documented in the final report.

The use of physical data patterns, i.e., patterns that are related to the actual layout of the DUT, rather than logical addressing is recommended where possible. These patterns may provide insight into the ionizing radiation sensitivity of the DUT. Because layout information is generally proprietary only DUT manufacturers would generally be expected to be able to meet this recommendation.

Some devices, particularly dynamic RAMs (DRAMs) and logic elements often have a “preferred” soft error failure, either $0 \rightarrow 1$ or $1 \rightarrow 0$. The selected test pattern must consider this possibility in its design. For testing when there is no *a priori* knowledge of the device the test pattern should balance the number of 0's and 1's. If the relative failure rates are known, perhaps from previous test experience, the test pattern may be adjusted to improve statistics of the less likely transition. The use of an unbalanced test pattern must be described fully in the final report and data analysis.

3.3.2 Supply voltage

The test plan defines the required supply voltage for the test. Since the soft error rate may be very sensitive to the supply voltage it is critically important that this parameter be accurately measured and controlled. Note that characterization of SER dependency on applied supply voltage is required by many customers. Some parts have internally regulated supply voltages that may interact with the measurement. These internally regulated supplies may automatically change their settings depending on operating mode, making the SER measurement dependent on the specific test method.

The DUT supply voltage needs to be carefully adjusted to match the values called for in the test plan. The soft error performance of many devices is very sensitive to the supply voltage so careful adjustment is required to assure consistent results. Some DUTs have internal voltage regulators and will be insensitive to supply voltage variations.

3.3.3 Static vs. dynamic testing

Depending on the objectives of the test program, static or dynamic operation of the DUT may be specified. For static tests the DUT is initialized to a known state, and then the DUT is irradiated. Following the irradiation, the state of the DUT is read out and compared with the initialized value to determine the number of upset events.

3.3.3 Static vs. dynamic testing (cont'd)

In dynamic testing the DUT is also initialized prior to irradiation to a known state. Once irradiation begins, the DUT is continuously accessed, at a rate specified in the test plan, counting upset events as they are detected. Once the irradiation stops, sufficient time to read all of the DUT is allowed to assure that all upsets induced by the radiation have been tabulated. Generally, the DUT state is rewritten with a new pattern as it is being accessed, to correct upset events and to exercise more internal data states.

The pattern of accesses for dynamic testing has to be planned to eliminate “dead-time” between a read of a location and a subsequent write to that location. Any upset that occurs between a read from a location and the next write will not be detected since it is overwritten. Failure to account for this dead time will result in an erroneously low estimate of SER. The final report must include details of the dead-time calculation.

Use of a “write array” followed by “read array” update is not recommended. Soft errors that occur between the last read of a location and its next write cannot be detected and result in excessive dead time. For the case where continuous updating of the array is used, this method would result in 50% of the test time being unused and the SER value being too low by a factor of 2.

Dynamic testing of memory is often carried out through the device’s normal access method. Non-memory components may use test access modes, such as JTAG boundary scan, for access to internal logic.

One example of a dynamic test cycle uses 2 cycles per address. The first cycle reads the value stored at the address, comparing it with the expected value and noting any errors. The second cycle writes a value to the same address to correct any errors. The second access writes the complement of the expected value so that every bit in the DUT changes state with each complete pass through the memory. This cycle has a very short dead time of approximately 1 memory cycle for each complete scan through the DUT.

Both types of testing are illustrated in the flow diagram in Figure 3.1. For these flows, a logical “checkerboard” pattern of alternating 0 and 1 value is assumed, along with a complementary rewrite operation for the dynamic test.

When testing non-memory components, such as microprocessors, the choice of static or dynamic testing may have a very large effect on the measured results, particularly at clock rates over 200 MHz. The

3.3.3 Static vs. dynamic testing (cont'd)

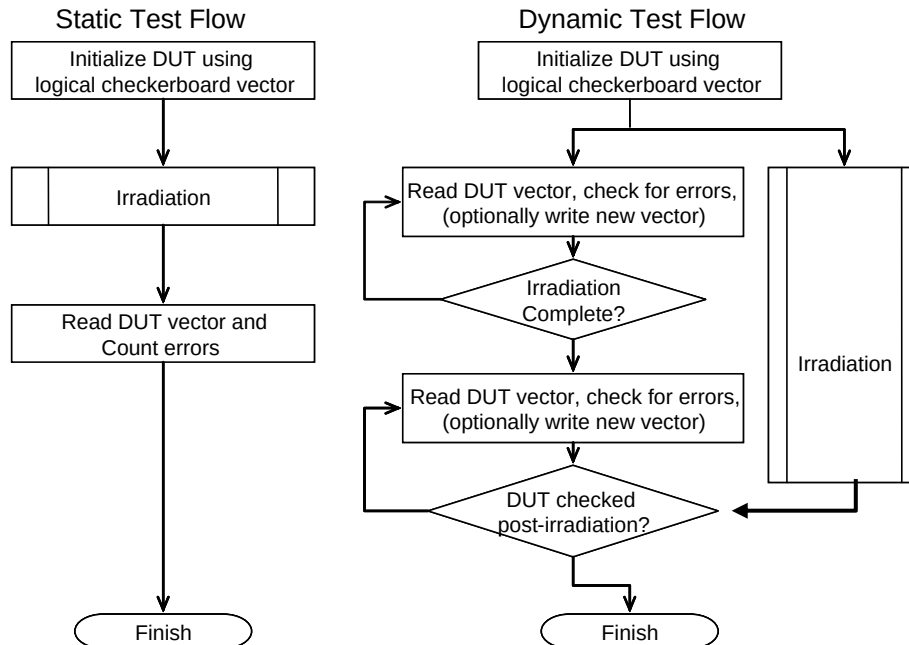


Figure 3.1 — Flow diagram comparing static and dynamic testing.

dynamic case will have a higher soft error rate due to the effects of errors in combinational logic being clocked into sequential logic elements and from race conditions created by particle strikes on the clock network.

3.4 Setup procedure

3.4.1 DUT packaging and handling

Special care must be taken in handling the DUTs used for real-time SER tests. All parts must be handled with the precautions for parts susceptible to damage from electrostatic discharge. The use of ground planes and straps is highly recommended whenever possible. In order for real-time SER results to be valid, standard production packaging (or a close replication) should be used whenever possible. While this might not be as important for neutron SER, the package can act as a source as well as shield for alpha SER. At the very least, the same molding compound and bump material (where appropriate) should be used.

3.4.2 Test equipment location

The test equipment should be set up close to the DUT holder to avoid noise issues related to long cabling. In the case of beam testing, this consideration must be balanced against test equipment upset from being too close to the scattered beam. Also ensure that cables are not physically blocking any areas accessed during the replacement of DUTs.

3.4.3 Test setup checkout

An ATE checkout should be performed with the equipment that will be used to perform the test, including all cables connected, as they will be during the irradiation. After any major changes such as replacing the DUT, or modifying the cabling arrangement, a short dry-run test should be run to verify proper operation of the devices and the test system. It is important to test the entire system, with all the DUTs in place for some time in order to ensure ATE integrity.

For accelerated testing, particularly neutron and proton beam testing, the ATE setup should be checked without irradiation to confirm that the error rate is less than 1% of the expected value. A very low error rate may be seen at some facilities due to residual radiation even when the beam is nominally “off.” If these errors are suspected of being due to electrical noise issues rather than residual radiation, the test must be halted and the source of noise eliminated.

3.5 General testing specifications

Keep testing the DUTs until the desired number of errors has been observed or until the appropriate test duration is reached (determined by the required confidence intervals in B.1).

A minimal test will include the following operations:

- 1) Load DUTs.
- 2) Verify correct test program execution and that all DUTs are nominal.
- 3) Monitor error location and time of detection.

3.6 Data collection

For each run, record all data required for the final report (see last section of 4, 5, 6, or 7). For tests using a radiation beam, the distance from a reference point must be noted to account for solid angle effects if appropriate. Record any problems or unusual behavior.

If possible, record failure signatures. The impact of upsets on different circuits will result in observable differences at an IC's output. For example, a hit on an address decode circuit may cause data to be written to the wrong address, causing two addresses to show up as fails – the address where the data was supposed to be written and the incorrect address where the data was actually written. Verify that the part is being properly operated, e.g., the appropriate address space is being covered for memory DUTs.

3.7 Considerations for testing non-memory components

Testing for non-memory components is a complex topic that cannot be completely described herein. This section addresses some specific issues to be considered for testing of various non-memory components such as random logic, microprocessors, and FPGAs.

A carefully written test plan and report are essential for meaningful non-memory testing. It is particularly important to consider the number of storage elements that are exposed during irradiation and the observability of errors in those elements. Errors in sequential logic, control structures and even FPGA configuration logic is often not observed during operation because it is masked by the operational state of the device or choice of test vectors. A minor change in the test conditions may have a large effect on the rate of observed errors.

3.7.1 Random logic circuits

Testing procedures of the following types of logic circuits and devices are specified:

- 1) Sequential Logic (includes dynamic combinatorial logic)
- 2) Register Files
- 3) Static Combinatorial Logic

The SER testing procedure critically depends on the type of logic device under investigation. Testing of types 1 and 2 are somewhat similar to SRAM testing, since both types of cells are memory/storage cells with feedback devices at the state nodes. SER testing of type 3 is much more involved due to the transient nature of the propagating glitches and the dependency on the circuit's logic configuration and state at the time a transient reaches a sequential cell or output.

Sequential Logic: In this section, the procedure to measure the *nominal* SER of sequential logic is described. (Note: The *nominal* SER refers to conditions where logic sequentials hold data statically, without clocks being exercised.) Clock upsets of nodes located in the sequential logic are not covered in this specification. Note that the actual SER of sequential logic in a product can be vastly different from nominal values and depends critically on the circuit context in which the sequential has been placed. The actual SER of sequential logic in a data path depends on the logic depth of the stage and on the clock frequency. The nominal SER of sequential logic can be tested using a shift register or array type architecture.

A sequential logic testing procedure typically involves the following steps:

- 1) The clock signal (or clock signals, if a race proof scheme is implemented) is running at a low speed (typically kHz to a few MHz range) and the data are shifted in.
- 2) The clock(s) is (are) stopped and the devices are irradiated.
- 3) Irradiation is stopped.
- 4) Clocks are turned on and data are shifted out and logged.

Due to the asymmetric nature of sequential nodes, critical charges and therefore failure rates of different sequential nodes are state dependent. At a minimum, data patterns must include a logical checkerboard pattern and its complement or both solid ones and solid zeros to cover all potential transitions and states. Patterns are written into the shift register before exposure and then irradiated for a given exposure time. After exposure data are shifted out and checked for any upsets. This procedure allows identification of the sequential logic cells that were upset during exposure.

For tests where the clock is running during irradiation, use of a test structure with a non-overlapping clocking scheme, where the master and slave stages of a flip-flop are clocked separately, is recommended to avoid minimum-delay problems. If master/slave flip-flops are used in a shift register topology together with a non-overlapping clock scheme, the state information of one stage (master or slave) is lost because the shifting process overwrites the state of one of the stages after both clocks have been stopped. Testing is recommended at slow clock speeds, i.e., at clock speeds where the cycle time is orders of magnitude longer than the internal device delays.[1, 2]

3.7.1 Random logic circuits (cont'd)

The DUT can be designed to have significant SEU contributions from one node only by increasing the critical charge Q_{crit} of other nodes sufficiently. This allows for a separation of $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions. Furthermore, by implementing various sequential flavors with different diffusion area sizes of the most critical node, the diffusion area scaling can be characterized [3].

The functionality of the sequential logic circuit must be tested prior to the radiation exposure for all patterns over the planned voltage range.

The nominal SER of sequential logic can also be assessed by exploiting scan chains implemented in products for testing purposes. The testing procedure in this case is very similar to the one above since scan chains are usually implemented in the form of shift registers.

Multiport Register Files: The SER of register files may be assessed using a memory array structure where all register file cells can be individually written and read. Testing guidelines are the same as for memory components. One important difference is, however, that for multiport devices the write and read logic also needs to be tested for its susceptibility to upsets.

Static Combinatorial Logic: The soft error rate of static combinatorial logic is defined here as the rate of latched glitches induced by upsets of combinatorial nodes. A glitch by itself is not considered a soft error and a static combinatorial gate by itself does not have a well-defined soft error rate. Its SER contribution depends on the circuitry it feeds into. The glitch induced by radiation can be attenuated or even blocked by consecutive stages. The arrival time at the latching element determines if the glitch is latched and therefore whether the event is relevant.

Static combinational SER has to be tested in its natural circuit environment. Static combinational SER can be tested using a shift register architecture as described in [4]. This architecture comprises shift registers of various lengths and with different logic depths to quantify the impact of clock speed and electrical masking on the failure rate. Because attenuation (electrical masking) depends on the gate delay relative to the pulse width, it is highly recommended that the static combinational test structures comprise paths with different logic depths and different logic-cell sizes (i.e., gate speeds).

To maximize the signal due to upsets occurring in combinatorial nodes in a test circuit, the SER contribution of sequential elements needs to be minimized. This can be achieved by using a minimum number of hardened sequential elements.

Because the content of the receiving latch impacts the sensitivity to the minimum magnitude and width of the glitch to be latched, data patterns must include a logical checkerboard pattern and its complement as well as solid 1 and solid 0 patterns [5].

Recommended variable evaluations include:

- 1) Voltage: nominal +/- tolerance; Expanded range of test voltages is highly recommended.
- 2) Different cycle times; please note that the SER of static combinational logic increases linearly with clock speed.

3.7.2 Field programmable gate arrays

When testing FPGAs for soft error effects, one should design the test strategy to detect:

- 1) SEU in the configuration memory
- 2) SEFI in the logic blocks
- 3) SEFI in the IO blocks
- 4) SEFI in the configuration circuitry
- 5) SEU in flip-flops embedded in logic blocks
- 6) SEU in RAM blocks

The final report should clearly show results for all failure mechanisms separately.

One approach for measuring SEFI and SEU in configuration memory uses a test strategy based on the continuous monitoring of the outputs of a combinatorial circuit implemented in the FPGA under test. As soon as a permanent mismatch of the output values is observed, the test is stopped and the configuration memory read back and stored in a file. Additionally, the FPGA configuration memory is periodically read back, even if the output values are correct. The test strategy enables identification of the non-critical and the critical SEU in the configuration memory, that is, those SEU in the configuration memory that do not create an error in the output, and those that create an error in the output.

For SEU in embedded logic blocks and RAM blocks, a similar approach to other stand-alone components may be used.

3.7.3 Microprocessors

The SER of microprocessors comprises failure contributions from the components described above. The microprocessor SER can be assessed either by properly adding up the contributions of those components tested individually, or by directly measuring the SER on the microprocessor itself [3.6]. In the latter case the microprocessor needs to be tested in either a real system or on a high speed ATE. In both cases the failure rate of a microprocessor is application dependent.

Testing in a real system involves running diagnostic software on the system that logs detected upsets. Note that this constitutes only one potential contribution of the overall microprocessor SER. Changes in unobserved states, also known as silent data corruption, can be observed for only by transforming silent errors into detected errors. Another complication arises from the fact that a system might crash and no data might be available on what caused the crash. Great care needs to be taken to ensure that the system is stable and that other intermittent errors are not mistaken as radiation-induced soft errors. In the case of accelerated testing of microprocessors in systems, it is important that only the DUT be irradiated and other peripheral chips are not accidentally irradiated.

Running the microprocessor on a high speed ATE while exposing it to radiation has the advantage that more of the relevant errors can be detected and less ambiguity exists. In this case the SER is typically assessed for specific patterns that might yield SER values very different from actual systems deployed in the field.

4 Real-time (unaccelerated and high-altitude) SER procedures

4.1 Background

4.1.1 Introduction

The most direct way to measure SER in a device is simply to observe it under standard operating conditions under normal ambient background radiation. The inherent problem with this approach is that the effective failure rate is so low that a single device would take decades to generate a statistically significant number of soft errors. In order to circumvent this limitation, real-time (unaccelerated) SER (RTSER) testing utilizes a very large number of devices in parallel to reduce the required test time. Testing can also be done at elevated altitudes where the higher neutron flux will generate a higher error rate. The system can either be a set of custom designed boards populated with a large number of the devices to be tested or a large server or other complex system (or array of servers/systems) containing a high part count.

Since RTSER testing typically involves a large number of devices and relatively long test times (weeks or months), a good test plan is crucial. It is extremely helpful to have some accelerated SER data (alpha particle and neutron) to get an estimate of the average failure rate. This estimate can then be used with the chi-squared statistics in C.2 to optimize the sample size and test duration so that the measured real-time SER will be valid to the desired confidence interval.

The procedures for non-accelerated RTSER and accelerated testing are similar. For real-time testing, the neutron flux is generally assumed to be a nominal value, based on the location of the ATE (see annex A). Alternatively, a measurement of the actual flux during the test may be made. This is a difficult measurement and beyond the scope of this specification. The alpha particle flux from the DUT packaging materials is assumed to be representative of the actual packaging. Separating the alpha and neutron contributions is complicated, requiring accelerated beam testing or system tests conducted at multiple locations. If RTSER results are to be used for SER estimates at other locations, this separation of effects is required. The minimum test procedures are listed separately below.

4.1.2 Guideline

The test method described below defines the requirements and procedures for RTSER testing without an ionizing source, i.e., only the natural ambient background radiation due to terrestrial cosmic rays and alpha particles from packaging and chip materials. Accelerated or ASER testing with alpha particles, high-energy neutrons/protons, and thermal neutrons are discussed in 5, 6 and 7, respectively.

4.1.3 Limits of test method

This test method can be used to test large arrays of SRAM or DRAM memory, and can be adapted for use with other types of components, such as microprocessors. The RTSER test algorithm and hardware must have allowances for separating actual radiation induced soft errors from errors induced by system noise. Since the RTSER test method does not discriminate between alpha particle and neutron induced soft errors, doing real-time tests on the same components in different environments, such as in a cave for shielding the terrestrial neutron flux, at high altitudes for enhancing terrestrial neutron flux, and thermal neutron shielding for shielding thermal neutrons (see 7) allow the alpha particle SER contribution (which will be constant) to be separated from the terrestrial high-energy and thermal neutron-induced SER.

4.1.4 Goal of test method

The primary goal of RTSER testing is to obtain a well-defined estimate of the total soft failure rate for products/components using a uniform test methodology.

4.2 Test facilities and equipment

4.2.1 Basic test requirement

The basic RTSER test requirement is to monitor each DUT's output vector and continually verify that the measured output matches the expected output vector. A vector could simply be a pattern of data stored within the memory array of a DUT, or a stream of data generated as an operation or sequence of operations performed by the DUT on an input vector. The latter would be relevant for logic devices such as microprocessors. If the vector from the DUT does not match the expected vector, then a soft error may have occurred. The system consists of the input stimulus generator and response recorder that is designed to accommodate the specified device. Testing requires some sequence of writing data to the DUT, reading the data back, comparing the output data to the written data, and tabulating the number of detected errors.

4.2.2 DUT board hardware

RTSER testing requires a DUT board capable of supporting a large number of DUTs. Several DUT boards may be used in a single system. The boards are controlled by a computer driven system that monitors and communicates with the DUTs during the test interval.

4.2.3 Test hardware

The test cables should be short enough and designed with the proper shielding to allow sufficient test speeds without electrical noise problems. If this is not possible, then on-board controllers should be used to allow high-speed operation of the DUTs and low speed communication off-board. The ATE should be capable of being configured to do both static and dynamic testing.

The following features are also desirable:

- 1) the ability to adjust and monitor the temperature of the DUTs or at least the ambient in which the DUT boards are located;
- 2) the ability to monitor power supply current of individual DUTs to check for latchup (preferably the ability to individually remove power from latched-up DUTs should also be provided);
- 3) if BPSG is used in the device process, the ability to shield the DUT enclosure from background thermal neutrons to determine their contribution to the SER (see 7);
- 4) operation at the rated core cycle for the DUT. If this is not possible due to power consumption issues, the deviation should be noted in the final report.

4.2.4 Test software

The basic requirements for a RTSER DUT test system are as follows:

- 1) Create test conditions for the DUT. A suite of test patterns should be selected that represents the intended operation of the DUT. In general, the test program for memories or arrays of latches should include patterns of ones, zeros and more complex variations, such as internal checkerboards, alternating rows and alternating columns to determine if the component has any preferred data states that are more robust or can be affected by nearest neighbors.
- 2) Identify and record any errors based on the selected test conditions. If an error does not go away when the component is rewritten or power cycled (powered down and then powered up), then it is a hard or intermittent fail. Hard fail events should be noted in the final report with an explanation of the source (e.g., a latent defect in the DUT, an early life fail, a power supply malfunction, etc.).
- 3) Provide adequate fault coverage and failure bit mapping. This is effective in distinguishing multiple independent failures from a cluster of nearest neighbor upsets from a single multi-cell upset caused by a single energetic particle (MCU). If a redundancy latch is hit and brings a defective row or column back into a repaired memory array, the signature of the error pattern should be distinguishable from a normal SEU or MCU. Likewise, if latchup occurs in a memory array, the signature of that event (typically inducing a large number of contiguous failing bits) should be uniquely distinguishable.
- 4) Initialization of control devices and rudimentary functional checks. Any upset of the control devices or power supplies should be distinguished from upsets of the DUT.
- 5) Select operation mode (dynamic or static operation) and provide resetting capability. For example, static testing of memory would be to write a test pattern once and store it for an extended period before reading the pattern back out. Dynamic testing of memory would involve writing once and then reading continuously or interleaving write and read operations at a specified operating frequency.
- 6) Provide error detection and logging. Typical error correction codes can correct a single bit and detect double bit errors but are ineffective at detecting multi-bit errors with a bit count greater than 2. Bit-by-bit comparison of the read pattern with the original write pattern is required to determine the details of particle hits.
- 7) Data analysis and logging while the test is in process. This is required to help separate independent events due to multiple particle hits from single events that upset multiple cells. (Note: This is less of a concern for real-time SER than accelerated SER due to the lower flux levels, but should not be ignored.)
- 8) Ability to distinguish and report different soft error types (e.g., single memory cell upset, multiple cell upsets, latchup, functional interrupts from hits on the address or control registers, etc.). See 2 for definition of types of soft errors.

4.3 Testing procedures

4.3.1 Pretest preparations

4.3.1.1 Sample selection

Component variability for RTSER is generally small for components produced with the same masks and fabrication steps. The system user must be sure that components tested are equivalent to actual baseline production components, because manufacturers may make process/design changes affecting SER without changing the component's designation.

In general a minimum requirement to establish a product's RTSER is to run the test with roughly equal numbers of nominal devices from at least three different baseline lots. If a product is tested that has on-board error-correction codes/circuits (ECC), tests should to be run under two conditions, both with ECC enabled and with ECC disabled if possible. The presence of ECC and its on/off status during each data collection run must be included in the final report. (Note: In general, ECC is effective at masking single-bit cell upsets. But it will be ineffective with non-cell related events such as neutron-induced latchup or other single-event functional interrupts).

4.3.1.2 DUT preparation and orientation

The DUT package used for the RTSER test must be identical to the package used for production components. This is critical for the alpha component of RTSER. If a finned heat sink is required, this can have an impact on the neutron flux reaching the DUT. Since there is some angular dependence for high-energy neutrons (more neutrons have normal incidence to the Earth's surface), the DUTs should be mounted in an orientation similar to the end use where the tester does not dictate otherwise. If this is not known, then the DUTs should be mounted horizontally to expose them to the maximum flux where the tester does not dictate otherwise. Care must be taken in considering the path of atmospheric neutrons in the real-time SER setup and the effects of building shielding. For example, vertical stacking of DRAM DIMMs that are each oriented in a horizontal position would cause a neutron to traverse many DRAMs before reaching the final device. The possibility of generating secondary particles as well as the attenuation of flux could lead to anomalous results. Therefore, the layout of the DUTs in real-time SER testing should avoid this. If this is not possible, an attempt should be made to note any differences in SER FIT between the top and bottom devices. Ideally, where other constraints do not exist, the testing location should also be done on the top floor or roof to avoid building shielding effects. Finally, the use of heatsinks, the orientation of the DUTs and stacking of DUTs should be noted in the final report.

4.3.1.3 Load DUT

Place the desired population of DUTs in their sockets on each DUT board and run the test program to verify proper operation of all the DUTs. Make necessary adjustments to system and DUTs to insure that the test program executes flawlessly on all DUTs in the test system.

4.3.1.4 Effective neutron flux at the test location

When performing real-time SER testing, it is necessary to either measure the neutron flux directly or make estimates based on the amount of building shielding and the terrestrial neutron flux (see annex A). Measurement of the actual neutron flux is rather involved because several detection schemes are required to obtain counts over a large neutron energy range and there are many interferences. The results should be normalized to NYC flux in the final report for purposes of standardization. A qualitative estimate of sensitivity to thermal neutrons should also be made (see 7).

If the testing is to be done at high altitude, several factors should be taken into consideration when designing the experiment.

- 1) The cosmic ray dosimetry method and how it is monitored.
- 2) The electrical power features and stability of the facility. The test setup often requires an independently stabilized uninterruptible power supply to run the test. Note that the overall power consumption for a large sample size can be significant. Make sure that the facility can provide the required power with good stability.
- 3) The lab should be protected against electrostatic discharge from lightning (i.e., presence of a Faraday cage, a lightning rod, etc.)
- 4) The environmental conditions that influence cosmic ray flux and how they are monitored (i.e., temperature, hygrometry, average pressure, average accumulation of snow, etc). An assessment of the impact of the variation of these environmental conditions (either important or insignificant) should be noted in the final report. If variation is determined to be insignificant, an average condition can be used in the final report. General guidance on the threshold for significant variation is a 50% impact on measured SER. Annex A details the impact of altitude and barometric pressure. As a quick rule of thumb:
Example 1 — a 40mmHg drop in atmospheric pressure (which is a significant change in weather conditions), will lead to a 50% increase in neutron flux.
Example 2 — based on typical values of snow density ($\sim 0.4\text{--}0.5 \text{ gm/cm}^3$), the reduction in neutron flux due to attenuation by snow on a roof is approximately 50% for 5 feet of snow.
- 5) It is convenient to have real-time monitoring of the experiment remotely through Ethernet access, as well as a remote reset function so that full-time staffing is not required.

4.3.1.5 DRAM and SRAM testing

At the minimum, data patterns must include a logical (external) checkerboard pattern and its complement, alternating by address and by bit. This will average out any asymmetry in SER behavior and represent actual application of the device. Read and write cycles should be selected so that all the elements of the DRAM or SRAM circuit (sense amps, storage capacitor or latches, decoders, multiplexers, etc.) are vulnerable to upset.

If the design supports a broad frequency range and different circuit elements will show different soft error rates as a function of frequency, care must be taken in selecting the core clock. A recommended solution is to run the RTSER test at a nominal frequency defined either by the tester capability or the product specification sheet to get a calibrated overall upset rate. Since the RTSER results can be frequency dependent, the nominal frequency used and how it was selected should be noted on the final RTSER report. Accelerated SER testing can then be used to determine the frequency dependent upset rate of the various circuit elements.

4.3.1.5 DRAM and SRAM testing

For those DRAM and SRAM designs that support a standby or reduced power mode (i.e., read and write operations are not allowed, but the device is expected to maintain its memory), a fraction of the real-time SER testing time should be dedicated to this mode of operation. The final report should include the estimate of SER from this mode vs. normal operating mode.

4.3.1.6 Other device testing

It might not be appropriate to use real-time SER testing procedures on all device types. Memory devices are good candidates because these devices are dominated by the core array and it is possible to capture and log all cell related upsets. Likewise, any FPGA or ASIC technologies using a high SRAM or DRAM content would be good candidates. On the other hand, not all upsets in logic devices will propagate to the output. This will depend on the static and dynamic design elements used. Therefore, an estimate of the expected fail rates should be made initially and the counting statistics discussed in annex B should be used to determine if a real-time SER test is appropriate for a device.

4.4 Differences in real-time SER tests and actual end-user observed fail rates

While the error rates determined from real-time SER testing are representative of device performance under real-life radiation conditions (both alpha particle and atmospheric neutrons), the results are not necessarily directly applicable to end user system applications. In addition to the customer environmental conditions that can be accounted for using Annex A (i.e. geomagnetic location, altitude, building construction, etc.), other factors that need to be taken into consideration in translating real-time SER FITs to actual end user error rates include (but are not limited to):

- 1) Geometry of end user system (e.g., Are components stacked? Are they above or below the system board? Are the system boards stacked? Are the system boards oriented parallel or perpendicular to the background radiation? etc.)
- 2) What types of errors are masked by software ECC code of the application (not to be confused with built in hardware ECC in some device designs)?
- 3) What fraction of errors will be over-written before they are read? (Highly sensitive to application software.)
- 4) Is the end-system using standard packaging or heat sinks?

4.5 Final report

The following items must be included in the final report for real-time SER tests:

DUT description:

- 1) Sample size (number of devices tested)
- 2) Vendor, Part # and Die rev (for commercial components)
- 3) Process technology (feature size, # and type of metal levels, presence or absence of polyimide or other layers, etc.)
- 4) Circuit (e.g., SRAM, DRAM, Microprocessor, FF chain, etc.)
- 5) On-chip error correction (type and coverage of ECC)
- 6) Dimension of the active device area tested.
- 7) Package (type, connection to chip, materials and geometries) with description of any modifications made for SER testing (e.g., etch back of encapsulant, etc.).

4.5 Final report (cont'd)

Test Description:

- 8) Test duration
- 9) Voltage (external supply, internal regulated, back bias voltages if applicable)
- 10) Junction & ambient temperature during test
- 11) Static or Dynamic test (core cycle time or frequency if dynamic) – special note must be made if the DUTs are run at a cycle time different than the intended end use
- 12) Refresh rate (where applicable)
- 13) Test patterns and data patterns, including dead-time calculation (see 3.3.3)
- 14) ATE (commercial model and/or physical description)
- 15) Description of test board
- 16) Special shielding from radiation sources (if used)
- 17) Record any problems or unusual behavior

Fail Information:

- 18) Time of each failure
- 19) Failing electrical address or addresses
- 20) Failing physical location or locations

Electrical signature of each soft error including a description of the occurrence of SEU, MBU, SEL, and SEFI events. Estimating a failure rate without determining the types of errors occurring (SEU, MBU, MCU, SEL, SEFI, etc.) can lead to erroneously high average failure rates. The effective failure rate of each unique failure signature must be calculated accordingly:

$$\text{FIT}(\text{total}) = [\text{total \# of events (SEU, MCU, SEL, etc.)} / \text{device hours}] \times 10^9$$

$$\text{FIT}(\text{single-cell}) = [\text{number of single cell events} / \text{device hours}] \times 10^9$$

$$\text{FIT}(\text{multiple-cell}) = [\text{number of multi-cell events} / \text{device hours}] \times 10^9$$

$$\text{FIT}(\text{SEL}) = [\text{number of SEL events} / \text{device hours}] \times 10^9$$

- 21) Voltage, ECC on/off status, chip power mode and test/data pattern at the time of failure
- 22) Identification of failures that are multiple-cell errors
- 23) Electrical signature and source of hard errors (if observed)

Real-time SER specific items

Location of devices under test:

- 24) Latitude and Longitude
- 25) Altitude
- 26) Average of atmospheric conditions
- 27) General building description (e.g., number of floors, building material, windows, etc.) and location of DUTs within building
- 28) Either a measurement of the neutron flux at the ATE or an estimation showing clear details of the calculation (e.g., direct measurement over a particular energy range, calculations from annex A, etc.)
- 29) Orientation of DUT to horizon and geometry of boards (i.e., planar or stacked)