

JEDEC STANDARD

Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices

JESD89B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

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Foreword

This standard defines the requirements and procedures for terrestrial soft error rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation, dominated by high- and low-energy neutron-induced reactions, and alpha-particle radiation from radioisotopic impurities in the package and chip materials. Other high energy particles, such as muons, are generated by cosmic rays and reach terrestrial altitudes. They are not considered in this standard at this point in time since there have been no significant soft error muon induced cross sections reported. An overall assessment of a device's SER is complete, **only** when an unaccelerated test is done under actual use conditions, **or** accelerated SER data for the alpha-particle component, the high-energy cosmic-radiation component, and if necessary, the thermal neutron component (see 7 for details) has been obtained and extrapolated to the use conditions.

Annexes D, E, F, G, H and J are informative; annexes A, B and C are normative.

Introduction

Soft errors are nondestructive functional errors induced by energetic particle strikes. Soft errors are a subset of single event effects (SEE), and include single-event upsets (SEU), single-bit upsets (SBU), multiple-bit upsets (MBU), single-event functional interrupts (SEFI), single-event transients (SET) that, if latched, become SEU, and single-event latchup (SEL) where the formation of parasitic bipolar action in CMOS wells induce a low-impedance path between power and ground, producing a localized high current condition (SEL can also cause latent and hard errors) if a thermal runaway condition is created). While there is variation on the exact use of these terms in the literature, Figure 1 shows how they are defined in this document (see 2 – Terms and definitions. For the components tested, all applicable SEE rates due to the different radiation types should be characterized.

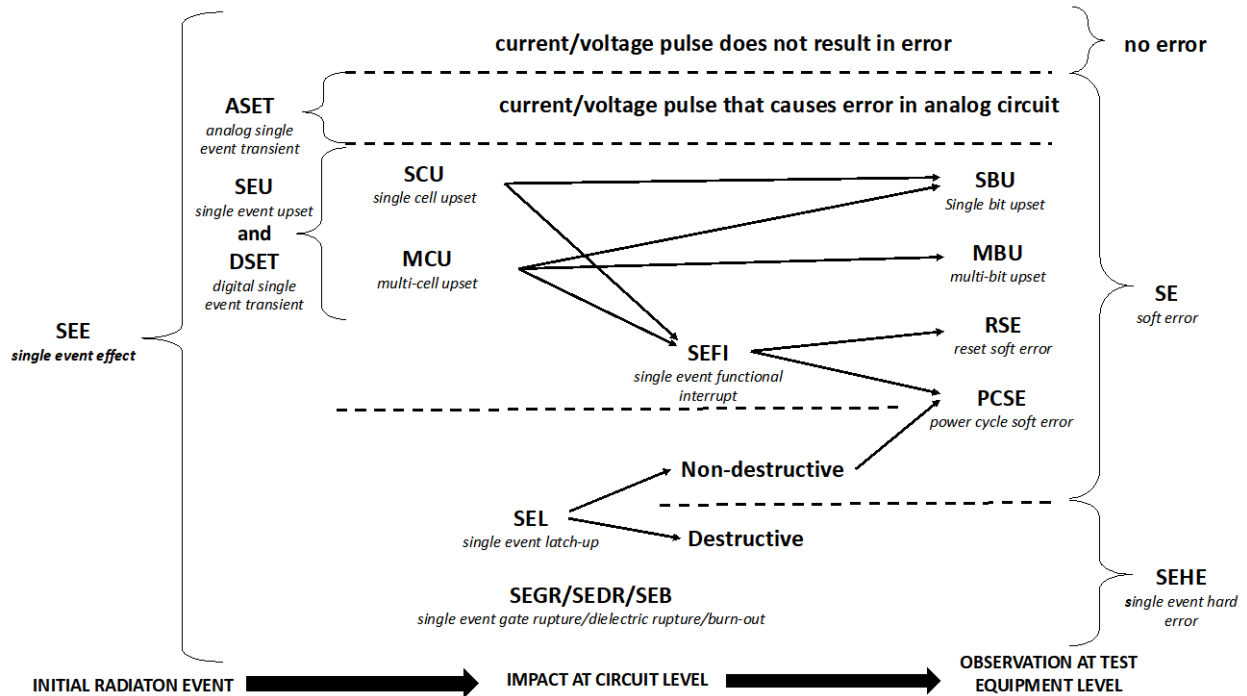


Figure 1 — Diagram of terms used to describe single event effects (SEE). More detailed definitions can be found in 2 Terms and definitions.

In general, soft errors may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by highly ionizing secondary particles produced from the reaction of both thermal and high-energy neutrons with component materials.

There are two fundamental methods to determine a product's SER. One is to test a large number of actual production devices for a long enough period of time (weeks or months) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. This is generally referred to as a real-time or unaccelerated SER testing. Real-time testing has the advantage of being a direct measurement of the actual product SER requiring no intense radiation sources, extrapolations to use conditions, etc. (provided the test is performed in a building location similar to the actual use environment – see A.5). However, real-time testing does require a system capable of monitoring hundreds or thousands of devices in parallel, for long periods of time.

The other method commonly employed to allow more rapid SER estimations and to clarify the source of errors is accelerated SER testing. In accelerated SER testing, devices are exposed to a specific radiation source whose intensity is much higher than the ambient levels of radiation the device would normally encounter. Accelerated SER allows useful data to be obtained in a fraction of the time required by unaccelerated real-time testing. Only a few units are needed and complete evaluations can often be done in a few hours or days instead of weeks or months. The disadvantages of accelerated SER are that the results must be extrapolated to use conditions and that several different radiation sources *must* be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray generated neutron events.

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

(From JEDEC Board ballot JCB-20-11, formulated under the cognizance of the JC-13.4 Subcommittee on Radiation Hardness: Assurance and Characterization.)

1 Scope

This standard specification covers soft errors due to alpha particles and terrestrial neutrons generated by cosmic rays. 2 covers terms and definitions. 3 covers test methods and issues common to all test types. 4 covers real-time or unaccelerated measurements, 5 covers accelerated soft error rate test procedures related to alpha particles, 6 covers accelerated soft error rate test procedures related to high-energy neutron reactions (>1 MeV), and 7 covers test procedures for thermal neutron reactions with ^{10}B .

This standard defines the requirements and procedures for terrestrial soft error rate (including real-time and accelerated) testing of integrated circuits and a standardized methodology for reporting the results of the tests.

The procedures apply to components including memory and logic. System behavior, including effects like Silent Data Corruption (SDC) and Detectable but Uncorrectable Errors (DUE), is beyond the scope of this standard.

NOTE This standard applies to electronic devices in a terrestrial environments (i.e., ~ 0 to 4,000 meters). Other environments (such as avionics or medical-radiation therapy) are outside the scope of this standard.

1.1 Related Documents

Testing with accelerated radiation sources can introduce damage mechanisms that interfere with the soft error measurements covered in this standard. The user should familiarize themselves with the following documents and eliminate or minimize these sources of interference:

- **JESD57** Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation
- **JESD234** Test Standard for the Measurement of Proton Radiation Single Event Effects in Electronic Devices

In addition, the following document provides more information on destructive effects from terrestrial radiation and accelerator environments:

- **JEP151** Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices
- **MIL-HDBK-814** Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices, 1994

And measurement of alpha flux is covered in the following:

- **JESD221** Alpha Radiation Measurement in Electronic Materials

1.1 Related Documents (cont'd)

The following sources are additional information on device irradiation:

- **ASTM F1192** Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices
- **ASTM E262-03** Standard Method for Determining Thermal Neutron Reaction and Fluence Rates by Radioactivation Techniques
- **MIL-STD-883J** Method 1017.3 Neutron Irradiation

Warning: These tests may involve hazardous materials, operations, and equipment. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and to determine the applicability of regulatory limitations prior to use.

2 Terms and definitions

ATE: Automated test equipment.

bit: Logical representation of a binary digit (i.e., zero or one)

cell: Either a combinatorial cell or a storage cell. Combinatorial cell is a circuit element that performs a combinatorial function within logic (e.g., XOR, NOR, NAND, etc.) Storage cell is a circuit element that stores one or more bits (e.g., DRAM, SRAM, multi-level FLASH, register, latch, flip flop, etc.)

component: A packaged die or integrated circuit (IC). A component is comprised of transistors, circuit nodes, interconnects, packaging, etc.

NOTE This may be either a test vehicle (i.e., test chip) or an actual IC product.

collected charge: The charge collected by a particular circuit node during the passage of a particle.

NOTE The collected charge is dependent on multiple design and manufacturing parameters: device geometry and design, circuit layout, particle mass, energy and trajectory, the density and type of material in the sensitive volume and the substrate material.

critical charge: The minimum amount of collected charge that will cause a device node to change state and result in a single event upset (SEU).

device, electronic: synonymous with component or microcircuit

differential flux: Flux per unit of energy, denoted as $d\Phi/dE$.

NOTE 1 Differential flux is usually expressed in particles per unit area per unit energy per unit time, e.g., $n/(\text{cm}^2 \text{ MeV hr})$.

NOTE 2 Spectral flux density is used in other publications and is synonymous with differential flux in this standard.

DUT: Device under test. In this instance, device is defined as a product IC or test chip.

ECC: Error correction code, sometimes called error detection and correction (EDAC).

fault coverage: The percentage of possible faults detected by a set of test vectors.

FIT: Failure in time; the number of failures per 10^9 device-hours.

fluence (of particle radiation incident on a surface): The total amount of particles incident on a surface in a given period of time, divided by the area of the surface and represented by the upper-case symbol Φ in this standard.

NOTE This fluence is usually expressed in particles per unit area (e.g., n/cm^2). Fluence is the product of flux multiplied by exposure time.

2 Terms and definitions (cont'd)

flux: The time rate of flow of particles incident on a surface, divided by the area of that surface, and represented by the symbol $\dot{\Phi}$ in this standard. It is the time rate of change of the fluence Φ : $\dot{\Phi} = d\Phi/dt$.

NOTE 1 Flux is usually expressed in particles per unit area, per unit time (e.g., n/cm^2h).

NOTE 2 The term “flux” is used in this standard whereas other standards might use the term “flux density” for the same meaning.

glitch: Any spurious voltage or current pulse in a circuit that occurs from a radiation event or electrical noise.

hard error: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit gate oxide rupture, single event burn-out and destructive latch-up.

NOTE The error is “hard” because the data is lost and the component or device is non-functional, even after power reset and re-initialization.

multiple-bit upset (MBU): A single event that induces upset of multiple-cells where two or more of the upsets occur in the same logical word (or frame/column/sector, etc. for FPGAs).

NOTE An MBU is a logical manifestation of a single event.

multiple-cell upset (MCU): A single event that induces several cells (e.g., memory cells or flip-flops) in an IC to flip their state at one time.

NOTE 1 The induced errors are usually, but not always, physically adjacent. This does not imply logical adjacency, since this will depend on how cells are placed and routed (interleaved).

NOTE 2 MCUs can manifest themselves logically as MBUs, multiple SBUs or a combination of the two.

power cycle soft error (PCSE): a single event effect that is not corrected by repeated reading or writing but can be corrected by removal and reapplication of power.

NOTE Non-destructive single event latch-up and SEFIs are power cycle soft errors.

process: A combination of people, procedures, methods, machines, materials, measurement equipment, and/or environment for specific work activities to produce a given product or service.

NOTE For the purposes of this standard the process is specifically the manufacturing steps and methodologies used to fabricate a component.

product: A component or service sold to satisfy a particular customer application.

NOTE For the purposes of this standard a product is a complete integrated circuit sold to satisfy a particular customer application.

2 Terms and definitions (cont'd)

radiation: Energy emitted in the form of electromagnetic waves or moving nuclear particles capable of causing direct or indirect ionization. Examples include protons, electrons, alpha particles and neutrons.

NOTE For purposes of this standard the primary radiation of concern is ionizing and includes protons, electrons, alpha particles, and nuclear reaction products.

real-time soft error rate (RTSER): Soft error rate measurement technique in a naturally occurring alpha particle and neutron environment using a large number of devices to obtain a statistically significant error count. This is in contrast to an accelerated SER test in which an intense radiation source is used on a single, or small number of devices. RTSER error counts can be increased by using a higher neutron flux at higher altitudes, but for the purposes of this specification, the term “accelerated test” is reserved for intense radiation sources that do not occur in natural terrestrial environments. System SER (SSER) is another term that is often used and is considered synonymous with RTSER.

reset soft error (RSE): an SEU that requires re-writing to the device configuration registers in order to return to normal operation without a power cycle operation. This reset can also be considered a reconfiguration (e.g., FPGA) or reprogramming.

sensitive volume: A region, or multiple regions, that will cause an SEE.

NOTE The sensitive volume is determined by the angle of the incident radiation, the mass and energy of the incident particles, and the density and type of material in the volume being penetrated by the incident radiation.

single bit upset (SBU): an SEU in which the observed error is a single logical or data bit.

NOTE The actual SEU can be an MCU, but if the cells are multiplex into different words, then the MCU will appear as multiple SBUs.

single cell upset (SCU): an SEU where only one cell or logic element (latch, flip flop, etc.) is upset (compare to MCU).

single-event burnout (SEB): An event in which a single energetic particle strike induces a localized high-current state in a device, resulting in catastrophic failure.

single-event dielectric rupture (SEDR): An event in which conducting path is created in a dielectric material from a single energetic particle strike.

single-event effect (SEE): An event initiated by a particle strike that causes a transient voltage or current pulse. Various types of SEE are shown in Figure 1.

2 Terms and definitions (cont'd)

single-event functional interrupt (SEFI): A single event effect (SEE) that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not result in permanent damage (i.e. hard error).

NOTE A SEFI is often associated with an SBU/MBU in a control bit or register, whereas an SEL is caused by the turn-on of a parasitic thyristor. Many SEFI events can be cleared with a component reset operation (see RSE). In cases where resetting some configuration registers requires a complete power cycle of the device, it can be difficult to distinguish between a SEFI and an SEL. A SEFI event does not necessarily result in an extended increase in operational current like a high current SEL.

single-event gate rupture (SEGR): An event in which a single energetic particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

single event hard error (SEHE): A hard error caused by a single event radiation strike.

single-event latch-up (SEL): An abnormal current state in a circuit caused by the passage of a single energetic particle inducing a parasitic thyristor to turn on and remain in a fixed state regardless of inputs, until the device is power cycled.

NOTE 1 Some SEL events result in a measureable current increase (e.g., latch-up of an IO circuit). Some SEL events may result in a difficult to detect increase in current (micro-SEL) compared to the quiescent current of the entire component (e.g., latch-up of memory cells within a common well).

NOTE 2 A high current SEL may cause permanent damage to the component and result in a hard error. Micro-SEL events are typically non-destructive due to the low current draw and can be cleared by power cycling.

single event transient (SET): A time dependent radiation induced spurious current or voltage signal on a circuit node. A digital SET (DSET) occurs when an SET in a combinational logic gate (along data or control paths) propagates and is latched to create an error (SEU) in the output of a sequential element. An analog SET (ASET) is a spurious signal in an analog circuit (e.g., a spurious signal on an IO pin, etc.) that causes an erroneous output.

NOTE Not all SETs will result in an upset or soft error. SETs propagating along data and control paths can be masked and never become a latched SEU (logic masking, electrical and temporal masking).

single-event upset (SEU): An error in a circuit that is not permanent (i.e. not a hard error) caused by a state change of a latch, flop, memory cell or other bistable element from a single energetic particle strike. The energetic strike can occur directly on the circuit element or propagate to that circuit (see SET).

NOTE In many documents and publications, SEU is used to include other soft errors, such as SEFI and SEL.

single-event upset (SEU) cross-section: the number of events per unit fluence. For device SEU cross-section, the dimensions are area per device. For bit SEU cross-section, the dimensions are area per bit.

single-event upset (SEU) rate: the rate at which single event upsets occur.

2 Terms and definitions (cont'd)

soft error: An erroneous output signal from a circuit that can be corrected by performing one or more normal functions of the device (e.g., retrying operation, rewriting data, power cycling, etc.) In many documents and publications, soft error is synonymous with SEU.

NOTE 1 The term refers to an error caused by radiation or electromagnetic noise (e.g., electromagnetic pulse from a nuclear event) and not to an error associated with a physical defect introduced during the manufacturing process. For the purposes of this standard, soft errors are considered to be single particle radiation induced events and not due to other sources, such as signal integrity or noise.

NOTE 2 The terms soft error and soft error rate (SER) have been adopted by the commercial IC industry while other terms, such as SEU, SEFI, etc., are typically used by the avionics, space, automotive, functional safety and military electronics communities.

NOTE 3 The term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).

soft error rate (SER): The rate at which soft errors occur.

storage element: A circuit or device that can be programmed to hold (or store) different states. For example, a DRAM cell, that can store charge (or not) on a capacitor. An SRAM cell or a flip-flop is another example.

test chip: A circuit or IC designed for the purpose of evaluating one or many device characteristics. For the purposes of this document, the characterization would be the soft error sensitivity of a particular process technology. But the test chip can incorporate other structures used to characterize different parameters, such as yield, speed, voltage margin, etc.

NOTE This test chip is not typically a product but is a dedicated component or section of an IC chip designed to be used to extrapolate to the SER of a product.

user: The individual using this standard to measure the soft error characteristics of a component or technology

3 Test equipment and software requirements

3.1 Test plan

A test plan shall be developed to support testing of each DUT type (if multiple types of devices are to be tested) and each type of test condition (i.e., temperature, voltage, frequency and test pattern). This test plan will serve as a guide for the procedures and decisions to be made during the irradiation period. In most cases, if the test plan cannot be followed exactly, adjustments must be made during the course of testing based on equipment performance, user observations and other factors that might not have been accounted for in the original plan.

In developing a test plan, the user should consider the following questions:

- 1) What are the single event effects that are of interest? And how can they be detected and classified?
- 2) What are the operating conditions of interest? What voltage, temperature, and frequency range is of interest (i.e., the entire datasheet specification, just nominal conditions or maximum stress conditions for soft errors)? What test patterns or program applications will be run? What device modes will be used (i.e., active vs standby as well as any special automated selective power saving programs)?
- 3) What sources of radiation will be used (e.g., the natural terrestrial spectrum? or special high intensity sources?) And what is the test duration – hours, days, weeks? Note: For accelerated alpha and neutron testing covered in Sec 5, 6 and 7), it is possible that the devices will receive particle doses greater than that under normal lifetime conditions which could impact various electrical parameters (i.e., dose effects). These dose effects are beyond the scope of this standard and the user should refer to other standards listed in Sec 1.1. As a precaution to determine dose effects are not an issue, the user can do device characterization (e.g., threshold voltage, leakage current, maximum frequency, etc) before and after accelerated testing.
- 4) What is the minimum detectable soft error limit of interest in case no errors are seen (e.g., How much testing is required to determine that a DUT displays an SEL < 10 FIT @90% confidence level if no SEL events are observed?) or what level of statistical variation around a measured mean soft error rate is desired (e.g., Is a +/- 50% variation about the mean at a 60% confidence level acceptable)? The answer to these questions will help to determine the test time required.

The following examples show how these questions can be handled.

Example 1 – An SRAM for which the user wants to determine the average cell upset rate within an 80% confidence level (CL) upper bound and 20% CL lower bound. annex C.2 gives an example of a device with an average soft error rate of ~1257 FIT. Table C.3 shows that if device testing is only carried out for 450 hours on 3500 parts, the upper and lower limits are 2717 FIT and 975 FIT, or 1270 FIT (see Table C.1) +114%/-23%. If testing were extended to 2045 hours, then the results would be 1257 FIT +39%/-19%. If the user desired and even smaller variation, longer test times and/or more devices would be required.

Example 2 – A power controller where the user wants to confirm the SEL is <10FIT at a 90% CL using a neutron beam with an acceleration factor of 10^6 . This usually implies that no SEL events will be observed at this low a FIT. Table C.2 shows the chi-squared values for error count and CL. For 0 errors and a 90% upper limit, $X^2 = 0.211$. Using the left side of Eq C.3 for a single device, the unaccelerated test time (T_r) would have to be $>10^7$ hr without any SEL events to satisfy <10 FIT, meaning >10 hr beam testing.

3.1 Test plan (cont'd)

Once these questions are addressed and the user has familiarized themselves with the appropriate radiation test sections (4 through 7), a test plan can be developed. If the soft error test campaign involves a remote site from the user's home location (e.g., particle beam facility or high altitude site for RTSER), it is highly recommended to make a site survey visit prior to creating a test plan in order to determine the details of the facility's support team, procedures, physical layout and infrastructure.

For beam and reactor facilities, the following questions should be addressed during the site survey visit:

- Is there special registration and training required by the facility prior to testing?
- If the facility runs 24hr a day, how does the user plan around the clock coverage?
- What are shielding materials to protect the test equipment and are they available at the facility or does the user need to bring them (especially thermal neutrons)?
- If other devices are on the DUT board and exposed to the beam, what precautions are taken (i.e., can these devices be put in a special position with respect to the beam or be shielded)? Where will equipment be placed and how will it be powered and accessed?
- How will communication between the various pieces of hardware be handled?
- Are there enough cables and are they long enough to connect all the equipment?
- What technique will be used to align the DUTs with the beam?
- Will one DUT be tested at a time? If multiple DUTs are exposed side by side, what is the beam uniformity across the exposure area? Or if the DUTs are mounted front to back, how will beam flux attenuation, energy dispersion and spallation effects be accounted for? (e.g., can the facility experts provide guidance or advice?)
- How will recording of results (both error logs and particle fluence) be managed?
- Is there a capability to analyze results while testing is taking place? Often times, test data will not be what is expected by the user. This requires "on the spot" decisions of whether or not to continue testing or change to an alternate plan. If consultation with software or applications engineers not present at the test site is needed for this decision, a method for sharing the test results in "real time" is required.
- Does the facility require quarantine of DUTs and equipment that has been in the beam due to radioactivity? If so, for how long? What are the security measures and process to retrieve the DUTs and equipment?
- Is a user agreement with the facility required?
- What happens if equipment damaged in shipment? Does the facility have equipment to effect repairs (e.g., solder irons, etc) or should the user bring repair equipment?

For RTSER testing at remote (i.e., high altitude) locations, the following questions should be addressed during the site survey visit:

- What is the nature of power sources provided by the facility (i.e., Are there routine interruptions in supply? How well controlled and noise free is it? What is the total power capacity? etc.)?
- What are the environmental controls of the facility (i.e., HVAC system capacity and controls)?
- How will data be collected over the duration of the test, which is bound to take several months (i.e., Will there be personnel on site during the total duration of testing? Or will the user have access test controls and data collection remotely after initial setup?)
- In the event of unanticipated events (e.g., power supplies blowing up or HVAC system failure), what are the plans for human intervention (i.e., Are there personnel on site or close by? Or will the user have to schedule an emergency trip?)
- Is a user agreement with the facility required?

3.1 Test plan (cont'd)

- What happens if equipment damaged in shipment? Does the facility have equipment to effect repairs (e.g., solder irons, etc) or should the user bring repair equipment?
- Does the facility provide real time logging of high energy and thermal neutron flux/fluence? Or will the user need to make a calculation based on annex A?

Prior to the actual test campaign, exhaustive dry-run testing should be done with all the equipment at the user home facility. Considerations should also be made for provisioning spare equipment and DUTs wherever possible. This will minimize the impact of any hardware failures that might occur during shipment or at the remote test location (e.g., cables, power supplies, ESD damage of DUTs, etc). In addition, the ability to electronically link with the user's home location is critical to allow for patches in any software and test bugs that might be uncovered during testing. Having application/test engineers as part of the test team (either on site or available via telecom/internet connection) is highly recommended. Check with the facility about remote login requirements. Due to firewall restrictions, this might require running two separate networks during testing – one local for the DUT/ATE hardware and one remote for technical support at the user's home facility. Before travelling to the test site, it is strongly recommended that several dry runs be made with the hardware, software and DUTs to confirm trouble-free operation. The user should also consider the use of a "golden part" (i.e., one or more DUTs that has been previously tested and characterized to serve as a check for repeatability at the same site or from site to site). If this is the first test campaign, the user should consider creating a "golden part" and setting it aside for calibration of future campaigns. Since these "golden parts" can be exposed to high radiation doses from multiple campaigns, radiation damage might occur. The user should perform electrical characterization on these parts and replace them with new "golden parts" when this occurs.

For all soft error testing it is important to understand the following:

- 1) Particle fluence at the DUT, either by estimation using annex A in the case of real time SER (RTSER) testing or measurement in the case accelerated SER testing using a particle beam, reactor or alpha particle source.
- 2) Number of circuit elements that are accessible to the user and subject to upset. The user should determine the basic schematic structure of the device (e.g., 4 kbit internal SRAM) to understand the internal elements at risk of soft errors. The user should understand how each applicable soft error type will be tested. In some cases, such as user visible bits, the SBU and MBU rates can be measured on a per bit bases. On the other hand, characterization of SEFIs may only be possible on a per device (or IC chip) basis if the source of the SEFI is unknown (i.e., details of which registers or sub-circuits caused the SEFI).
- 3) Number of upsets that occur in each circuit element or function. The user should think about how many of each type of upset event (e.g., memory SBU, SEFI, SEL, etc) should be measured.
- 4) The user should develop an initial estimate of the number of upsets to be measured in the allotted test interval. Prior published data on soft error rates can be used as a guide if the user has no prior experience. If no data are available, the user should decide on the lowest soft error limit of interest such that the observation of zero errors confirms this limit (See annex B – Real Time Counting Statistics).

3.2 Test equipment

3.2.1 ATE hardware

The automatic test equipment (ATE) hardware used for testing may be conventional electronic test gear or custom-built equipment. The ATE must be able to tolerate stray radiation (or be shielded or mounted remotely in a shielded area) and able to operate in potentially poor quality power conditions. The use of uninterruptible battery-backed power supplies is recommended in facilities that cannot provide highly reliable power.

The ATE hardware must be capable of exercising the DUT over the range of operating conditions such as power supply voltage, access cycle speed and temperature that are specified in the test plan. Proper operation of the ATE under all of these operating conditions must be rigorously confirmed prior to the beginning of testing with a radiation source. The use of cabling to connect the DUT and test equipment, power supply accuracy at the DUT, and the exposure of the ATE to scattered radiation during testing should all be considered. (Note – In general, power supplies are sensitive to radiation. Therefore, measures should be taken to minimize their exposure.)

3.2.2 ATE software

The ATE software creates the proper conditions for the test. It identifies and records errors as they are detected. Depending on the test, software can also be used to correct the errors before continuing. The user should make a determination of the fault coverage required. When designing the test system, the user should understand the portions of the die, signal path, and latching circuits of the device being tested in order to arrive at a quantitative result. The fraction of time the device is in an SEE susceptible mode and what fractions of the DUT's susceptible elements are not tested should be known. Complex devices do not always permit easy testing access.

The ATE software should be capable of:

- 1) Controlling device initialization and rudimentary functional checks.
- 2) Device operation in dynamic or static operation, as required by the test plan.
- 3) Resetting the DUT during beam irradiation or environmental real-time testing.
- 4) Error detection and logging, including the time that the error was detected. It is important during error detection that new errors are not omitted (i.e., the process of reading out errors does not interfere with the collection of new errors).

In addition to the characteristics listed above, the following features are also desirable:

- 1) Bit error mapping and data processing, storage and retrieval for display.
- 2) High-speed operation and a high duty factor (i.e., datasheet frequency and operating load specifications).
- 3) Real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing.
- 4) The ability to do preliminary data analysis while the test is in progress. This feature is desirable for modification / optimization of test procedures in light of the data being collected.
- 5) Reliable audit path for data collection to allow correlation of experimental notes and collected data from the ATE.
- 6) Recording the particle fluence, either automatically acquired from the test facility or manually entered.

3.3 Test conditions

Test conditions include the source of radiation, environmental conditions (voltage, temperature, frequency, etc), test patterns or applications and mode of operation (dynamic vs static). Considerations should be given to the actual application of the device in real operating environments. If the SER test cannot duplicate all of these conditions (e.g., if the component cannot be run at datasheet speeds during radiation testing), any techniques to extrapolate tested ~~SEU~~ soft error rates to application ~~SEU~~ soft error rates should be clearly explained in the final report.

3.3.1 Test pattern/applications

Based upon the product being tested, careful consideration should be given to test patterns/applications that cover the maximum functionality space of the device. For example, the basic data patterns for all memory circuits is a combination of logical checkerboard (alternating by address and bit) as well as solid 1 and 0s. If detailed layout information for the DUT is available, a physical checkerboard is also useful. A determination of the best test pattern s appropriate for the DUT and its use is left to the discretion of the user, but must be documented in the final report.

The use of physical data patterns, i.e., patterns that are related to the actual layout of the DUT, rather than logical addressing is recommended where possible. These patterns may provide additional insight into the ionizing radiation sensitivity of the DUT. Because layout information is generally proprietary only DUT manufacturers would generally be expected to be able to meet this recommendation.

Some devices, particularly dynamic RAMs (DRAMs) and logic elements often have a “preferred” soft error failure, either $0 \rightarrow 1$ or $1 \rightarrow 0$. The selected test pattern must consider this possibility in its design. For testing when there is no *a priori* knowledge of the device, a minimum of four test patterns should be used: all 0s, all 1s and checkerboard (and its inverse). (Note: If knowledge of the layout is available, these patterns should be physical.) If the relative failure rates are known, perhaps from previous test experience, the test pattern may be adjusted to improve statistics of the less likely transition. The use of an unbalanced test pattern (i.e., deviation from checkerboard, all 1s or all 0s) must be described fully in the final report and data analysis.

3.3.2 Environmental Conditions

The test plan defines the required supply voltage, temperature and operating frequency for the test. Since the soft error rate may be very sensitive to the supply voltage, temperature and frequency, it is critically important that these parameters be accurately measured and controlled. Some parts have internally regulated supply voltages that may interact with the measurement. These internally regulated supplies may automatically change their settings depending on operating mode, making the SER measurement dependent on the specific test method. If the test plan requires SER measurement from minimum to maximum voltage, the user should consider if internal voltage regulators are used and if they can be disabled without leaving the DUT unoperable or should be left in operation per the test plan. Considerations should be given to the junction temperature of the device vs monitoring temperature (eg thermocouple on or near the device package).

3.3.3 Static vs. dynamic testing

It is important to consider the interaction of the soft error test with the operating modes of the device. The following definitions help to clarify the use of the terms static and dynamic in the context of soft error test methods and device operating modes.

Static Device Operation – Many devices have a static (aka standby or idle) mode to reduce power consumption. This mode can be implemented in many different ways (e.g., reduced clock frequency, clock gating, lower V_{dd} or completely turning off parts of the device) depending on the IC design. These modes should be documented in the device datasheet. The soft error performance of a device can depend on the operating mode and the user should define what modes are of interest in the Test Plan (3.1).

Static Soft Error Testing – For static soft error testing, a device is first loaded with a test pattern or vectors and then put into a static or idle mode, or powered down completely in the case of non-volatile memory. The device is then radiated for a specified time. After radiation, the device is returned to normal operation so that upsets can be determined. Static soft error testing will expose errors in state elements (e.g., flops, latches, memory cells, etc.). If these elements are at reduced voltage or frequency during idle mode, then the soft error rates measured are for the reduced voltage or frequency used. These rates can be different than the rates measured when full power and frequency are applied. Self-heating effects (i.e., change in junction temperature due to voltage and frequency effects) can also have an impact. The limitation of static soft error testing is that the temporal information is not captured which prevents the user from separating temporal and physically adjacent single-event multiple-bit upsets.

Continuously-Read Soft Error Testing – For continuously-read soft error testing, the memory arrays are first loaded with a test pattern and then the arrays will be read in a loop for a specific loop count (e.g., 1 loop is a pass through the entire memory space), error count, or duration of time. For memory array, typically the read operation will be executed on a per address basis. Once the error is found, the address information should be reported along with the time stamp (i.e., time or loop count). To prevent the same error from being reported in the next iteration of the read loop, the correct data should be written back to the word with the error. The timing information of the errors can be used to help distinguished between temporal and physically adjacent single-event multiple-cell upsets. Errors that are found physically adjacent to each other but separated by more than 1 loop count cannot be from the single-event upset. The second error has to come from a different event, otherwise it would have been detected in the same loop as the first error (with the exception that the event happens right after one address is read and before the other address is read). However, care must be taken to ensure that the flux used in the test is not too high because if there are too many errors that need to be written back, a significantly delay in the completion of the read loop cycle could result in loss of the temporal data.

Dynamic Soft Error Testing – For dynamic soft error testing, the device is run in normal operating mode running user applications (or tests to simulate user applications) while it is being radiated. Typically, this involves running the device under typical datasheet conditions (i.e., nominal voltage, temperature and frequency). In addition, extended voltage, temperature and frequency conditions can be used to determine the soft error rates over a range of environmental IC operation window. This test mode exposes all of the elements of the device that are used in normal operation to soft error. It should be noted that many modern IC designs at advanced technology nodes use automated internal power saving features by shutting down various circuit blocks that are not in use for a particular test or operation. If these features are running during dynamic soft error testing, radiation strikes to the control circuits can cause these features to malfunction leading to possible SEFI events.

3.3.3 Static vs. dynamic testing (cont'd)

NOTE In order to characterize soft error events related to the device IO and power pins, the user should ensure that the DUT board design uses impedances consistent with the datasheet specification.

Depending on the objectives of the test program, static or dynamic operation of the DUT may be specified. For static tests the DUT is initialized to a known state (e.g., data pattern written into memory, and then the DUT is irradiated. Following the irradiation, the state of the DUT is read out and compared with the initialized value to determine the number of upset events.

In dynamic testing the DUT is also initialized prior to irradiation to a known state. Once irradiation begins, the DUT is continuously operated (e.g., continuous write-read operations) at a rate specified in the test plan, counting upset events as they are detected. Once the irradiation stops, sufficient time to read all of the DUT is allowed to assure that all upsets induced by the radiation have been tabulated. Generally, the DUT state is rewritten with a new complement pattern as it is being accessed, to correct upset events and to exercise more internal data states.

The pattern of accesses for dynamic testing has to be planned to minimize “dead-time” between a read of a location and a subsequent write to that location. Any upset that occurs between a read from a location and the next write will not be detected since it is overwritten. Failure to account for this dead time will result in an erroneously low estimate of SER. The final report must include details of the dead-time calculation.

Use of a “write array” followed by “read array” update is not recommended. Soft errors that occur between the last read of a location and its next write cannot be detected and result in excessive dead time. For the case where continuous updating of the array is used, this method would result in 50% of the test time being unused and the SER value being too low by a factor of 2. A better strategy would be to perform a write – soak – read followed by immediate write of new data (where soak is the delay time between write and read, the time the memory cell is susceptible to an upset that will be detected and not overwritten.) This minimizes the dead time to small period between read and re-write.

Dynamic testing of memory is often carried out through the device’s normal access (i.e., row and column address circuits). Non-memory components may use test access modes, such as JTAG boundary scan, for access to internal logic.

One example of a dynamic test cycle uses 2 cycles per address. The first cycle reads the value stored at the address, comparing it with the expected value and noting any errors. The second cycle writes a value to the same address to correct any errors. The second access writes the complement of the expected value so that every bit in the DUT changes state with each complete pass through the memory. This cycle has a very short dead time of approximately 1 memory cycle for each complete scan through the DUT.

Both types of testing are illustrated in the flow diagram in Figure 3.1. For these flows, a logical “checkerboard” pattern of alternating 0 and 1 value is assumed, along with a complementary rewrite operation for the dynamic test.

When testing non-memory components, such as microprocessors, the choice of static or dynamic testing may have a very large effect on the measured results, particularly at clock rates over 200 MHz. The

3.3.3 Static vs. dynamic testing (cont'd)

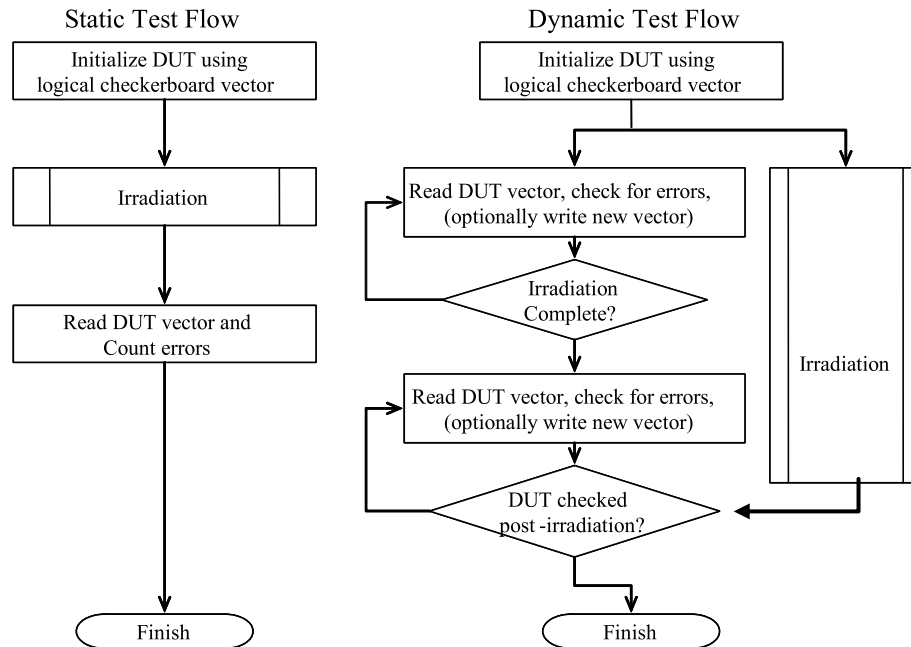


Figure 3.1 — Flow diagram comparing static and dynamic testing.

dynamic case will have a higher soft error rate due to the effects of errors in combinational logic being clocked into sequential logic elements and from race conditions created by particle strikes on the clock network.

3.4 Considerations for Soft Error Testing of Individual Circuit Elements

Modern IC components typically consist of several different types of circuit elements – latches, flops, memory cells, clock circuits, etc. How each of these building blocks respond to radiation can be very different. For example, higher voltages on a flip-flop or memory cell might decrease its SER (due to a higher stored charge) but increase the probability of SEL in a parasitic pnpn element. The purpose of this section is to outline the known soft error effects in these various circuit elements. The user should be familiar with the various circuits in the DUT of interest in order to formulate a valid Test Plan. If detailed circuit schematics of the DUT are not possible, familiarity with the various DUT functions from the datasheet should be used.

This section addresses soft error testing of the individual building block circuits used to design a modern IC product (FPGA, CPU, SoC, etc). Test chips can be designed with these elements in order to test SEU effects. Alternatively, the can user isolate and test these circuit elements individually on a complex IC product. 3.5 addresses soft error testing of the entire IC as a whole.

3.4 Considerations for Soft Error Testing of Individual Circuit Elements (cont'd)

3.4.1 Memory

Memory devices store digital data in memory cells, which can be addressed and read out. The logical address is the electronic representation and the physical address is the actual x-y coordinates of the cell. Typical memory cells store a 0 or 1 (e.g., DRAM, SRAM and single level NVM) but multi-level data storage is also possible (e.g., Multi-level cell NVM). Typically, memory cells are packed in close physical alignment and a single soft error event can lead to the upset of a single cell or multiple cells in close physical proximity. Upset rates can also depend on whether the bit flip is from a logical 0 --> 1 or 1-->0. The user should also be aware that there can be a difference between logical 0s and 1s vs voltage stored on a node or not. A memory cell is susceptible to a soft error event between the time data is written and when it is read back. If new data is overwritten before a read, then any soft errors will be erased and undetected.

3.4.2 Combinational Logic

In combinational logic, the output is a pure function of the present input only. An SET event can occur at any time on an input (or internal) node that changes the output state.

3.4.3 Sequential Logic

In sequential logic, the output depends not only on the present value of its input signals but on the sequence of past inputs. For synchronous sequential logic, the state of the circuit changes only at specific times in response to a clock signal. Therefore, soft errors will depend on a) any upsets in the input logic or signal lines, b) timing of the radiation strike and c) the clock frequency. For asynchronous sequential circuits, the state of the device can change at any time in response to changing inputs. In this case, the soft error event in the registers can occur at any point in time.

3.5 Considerations for Testing IC Products

Testing for non-memory components is a complex topic that cannot be completely described herein due to the wide variety of different ICs. This section addresses some specific issues to be considered for the fundamental soft error testing of various memory and non-memory components (e.g., random logic, microprocessors, and FPGAs, analog devices and power devices). In today's IC technology, many products have combined memory and logic functions. This section addresses considerations for testing the IC as a whole (e.g., normal operating functions). 3.4 addresses soft error testing of the individual elements (or building blocks) of the IC.

A carefully written test plan and report are essential for meaningful non-memory testing. It is particularly important to consider the number of storage elements that are exposed during irradiation and the observability of errors in those elements. Errors in sequential logic, control structures and even FPGA configuration logic is often not observed during operation because it is masked by the operational state of the device or choice of test vectors. A minor change in the test conditions may have a large effect on the rate of observed errors.

3.5 Considerations for Testing IC Products (cont'd)

3.5.1 Memory components

There are three basic functions of a memory component: write data, store data and read data. Any of these operations can be susceptible to soft errors. The memory cells (i.e., memory core) are common to each of these modes. Different periphery/logic circuits can be used for each of these operations. Therefore, for complete soft error testing of memory, each of these three functions should be exercised and a determination made of the soft error rate during each of these operations.

Example 1 - Determine the susceptibility in the storage mode

Data can be written into memory prior to irradiation (so soft errors won't occur in the write mode), the memory is then irradiated to induce soft errors and then data read out after radiation is turned off (so soft errors won't occur in the read mode). The soft error rate can be measured in normal operation (i.e., normal voltage supplied to the memory core) or in standby mode (i.e., core power is reduced but still maintains data). Care should be taken to insure that the only errors occurring in standby mode are due to radiation (i.e., the memory should be cycled through write-standby-read without radiation and display no errors).

Example 2 - Determine the susceptibility of read mode

Data can be written into memory prior to irradiation (so soft errors won't occur in the write mode), memory is then irradiated and read continuously. Soft errors in this mode can be due to cell upsets as well as read circuit upsets. Comparison of soft error data with Example 1 can give insight into how much and what types of errors are due to the memory cells vs the read circuits.

Example 3 - Determine the susceptibility of write mode

Data can be written and read continuously during irradiation. In this case, both read and write circuits are susceptible to soft errors as well as the memory cells. Comparison of data acquired in this mode with Examples 1 and 2 can give insight into the soft errors from the write circuits.

If the user is knowledgeable about cell asymmetries (i.e., if a 1 or 0 represents stored charge in a DRAM, or an SRAM cell is more sensitive to read or write disturb when transitioning from $1 \rightarrow 0$ or $0 \rightarrow 1$), this information can be helpful in explain if there are pattern dependent differences in error rates.

3.5.2 Random logic circuits

Testing procedures of the following types of logic circuits and devices are specified:

- 1) Sequential Logic (includes dynamic combinatorial logic)
- 2) Register Files
- 3) Static Combinatorial Logic

The SER testing procedure critically depends on the type of logic device under investigation. Testing of types 1 and 2 are somewhat similar to SRAM testing, since both types of cells are memory/storage cells with feedback devices at the state nodes. SER testing of type 3 is much more involved due to the transient nature of the propagating glitches and the dependency on the circuit's logic configuration and state at the time a transient reaches a sequential cell or output.

3.5.2 Random logic circuits (cont'd)

Sequential Logic: In this section, the procedure to measure the *nominal* SER of sequential logic (i.e., logic whose output depends not only on the present value of its input signals but on the sequence of past inputs) is described. (Note: The *nominal* SER refers to conditions where logic sequentials hold data statically, without clocks being exercised.) Clock upsets of nodes located in the sequential logic are not covered in this specification. Note that the actual SER of sequential logic in a product can be vastly different from nominal values and depends critically on the circuit context in which the sequential has been placed. The actual SER of sequential logic in a data path depends on the logic depth of the stage and on the clock frequency. The nominal SER of sequential logic can be tested using a shift register or array type architecture.

A sequential logic testing procedure typically involves the following steps:

- 1) The clock signal (or clock signals, if a race proof scheme is implemented) is running at a low speed (typically kHz to a few MHz range) and the data are shifted in.
- 2) The clock(s) is (are) stopped and the devices are irradiated.
- 3) Irradiation is stopped.
- 4) Clocks are turned on and data are shifted out and logged.

Due to the asymmetric nature of sequential nodes, critical charges and therefore failure rates of different sequential nodes are state dependent. At a minimum, data patterns must include a logical checkerboard pattern and its complement or both solid ones and solid zeros to cover all potential transitions and states. Patterns are written into the shift register before exposure and then irradiated for a given exposure time. After exposure data are shifted out and checked for any upsets. This procedure allows identification of the sequential logic cells that were upset during exposure.

For tests where the clock is running during irradiation, use of a test structure with a non-overlapping clocking scheme, where the main and secondary stages of a flip-flop are clocked separately, is recommended to avoid minimum-delay problems. If main/secondary flip-flops are used in a shift register topology together with a non-overlapping clock scheme, the state information of one stage (main or secondary) is lost because the shifting process overwrites the state of one of the stages after both clocks have been stopped. Testing is recommended at slow clock speeds, i.e., at clock speeds where the cycle time is orders of magnitude longer than the internal device delays.[1], [2]

The DUT can be designed to have significant soft error contributions from one node only by increasing the critical charge Q_{crit} of other nodes sufficiently. This allows for a separation of $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions. Furthermore, by implementing various sequential flavors with different diffusion area sizes of the most critical node, the diffusion area scaling can be characterized [3].

The functionality of the sequential logic circuit must be tested prior to the radiation exposure for all patterns over the planned voltage range.

The nominal SER of sequential logic can also be assessed by exploiting scan chains implemented in products for testing purposes. The testing procedure in this case is very similar to the one above since scan chains are usually implemented in the form of shift registers.

3.5.2 Random logic circuits (cont'd)

Multiport Register Files: The SER of register files may be assessed using a memory array structure where all register file cells can be individually written and read. Testing guidelines are the same as for memory components. One important difference is, however, that for multiport devices the write and read logic also needs to be tested for its susceptibility to upsets.

Static Combinational Logic: The soft error rate of static combinatorial logic is defined here as the rate of latched glitches induced by upsets of combinatorial nodes. A glitch by itself is not considered a soft error and a static combinatorial gate by itself does not have a well-defined soft error rate in digital logic. Its SER contribution depends on the circuitry it feeds into. The glitch induced by radiation can be attenuated or even blocked by consecutive stages. The arrival time at the latching element determines if the glitch is latched and therefore whether the event is relevant and results in a SEU.

Static combinational SER has to be tested in its application environment. Static combinational SER can be tested and quantified using a shift register architecture as described in [4], [5] and [6]. This architecture comprises shift registers of various lengths and with different logic (i.e., shift register) depths to quantify the impact of clock speed and electrical masking on the failure rate. Because attenuation (electrical masking) depends on the gate delay relative to the pulse width, it is highly recommended that the static combinational test structures comprise paths with different logic depths and different logic-cell sizes (i.e., gate speeds). This technique quantifies the SET induced SEU rate that can be quantified per path or per gate and extrapolated to the circuit block or product level.

Another approach to estimate the contribution of ionizing particle strikes in combinational logic that relies on test-chips is circuitry that enables characterization of SET amplitude and width distributions for different static logic cells along circuit paths [7]. The pre-characterized distributions are then applied in a full product risk assessment which involves estimating the fraction of SETs that are latched in clocked receivers.

To maximize the signal due to upsets occurring in combinatorial nodes in a test circuit, the SER contribution of sequential elements needs to be minimized. This can be achieved by using a minimum number of hardened sequential elements.

Because the content of the receiving latch impacts the sensitivity to the minimum magnitude and width of the glitch to be latched, data patterns must include a logical checkerboard pattern and its complement as well as solid 1 and solid 0 patterns [8].

Recommended variable evaluations include:

- 1) Voltage: nominal +/- tolerance; Expanded range of test voltages is highly recommended.
- 2) Different cycle times; please note that the SER of static combinational logic increases linearly with clock speed.

3.5.3 Field programmable gate arrays

When testing FPGAs for single event effects, one should design the test strategy to detect:

- 1) SEU in the configuration memory
- 2) SEFI in the logic blocks
- 3) SEU and SEFI in the IO blocks
- 4) SEFI in the configuration circuitry
- 5) SET and SEU in flip-flops embedded in logic blocks
- 6) SEU in RAM blocks (or user memory)
- 7) SEL – either non-destructive (i.e., increased leakage) or destructive

FPGA supplier view vs user view of soft error testing – An FPGA supplier should characterize the soft error cross-section at the basic building block level. A user can use this information to do their own estimate of the total soft error cross-section of their design (not covered in this standard) or use the suppliers software tools (if available). The user might also choose to do actual soft error testing on an FPGA configured to their own application (or user configured circuit). The user derived soft error cross-section is design/application (or user configured circuit) dependent and does not apply to different design/applications on the same FPGA base die.

The final report should clearly show results for all failure mechanisms separately. On-line scrubbing (periodic reading and correction of configuration memory) detects soft errors within seconds to minutes of their occurrence (depending on scan time). Functional monitoring is capable of detecting errors in the application. With the combination of on-line scrubbing and functional monitoring it is possible to directly tie the FPGA's SEUs to the functional failure. Furthermore, on-line scrubbing will keep SEUs from accumulating, making it easier to do fault attribution.

For SEU in embedded logic blocks and RAM blocks, a similar approach to other stand-alone components may be used.

3.5.4 Microprocessors

The SER of microprocessors comprises failure contributions from the components described above. The microprocessor SER can be assessed either by properly adding up the contributions of those components tested individually, or by directly measuring the SER on the microprocessor itself [3],[9]. In the latter case the microprocessor needs to be tested in either a real system or on a high speed ATE. In both cases the failure rate of a microprocessor is application dependent.

Testing in a real system involves running diagnostic software on the system that logs detected upsets. Note that this constitutes only one potential contribution of the overall microprocessor SER. Changes in unobserved states, also known as silent data corruption, can be observed for only by transforming silent errors into detected errors. Another complication arises from the fact that a system might crash and no data might be available on what caused the crash. Great care needs to be taken to ensure that the system is stable and that other intermittent errors are not mistaken as radiation-induced soft errors. In the case of accelerated testing of microprocessors in systems, it is important that only the DUT be irradiated and other peripheral chips are not accidentally irradiated.

Running the microprocessor on a high speed ATE while exposing it to radiation has the advantage that more of the relevant errors can be detected and less ambiguity exists. In this case the SER is typically assessed for specific patterns that might yield SER values very different from actual systems deployed in the field.

4 Real-time (unaccelerated and high-altitude) soft error test procedures

4.1 Background

4.1.1 Introduction

The most direct way to measure SER in a device is simply to observe it under standard operating conditions under normal ambient background radiation. The inherent problem with this approach is that the effective failure rate is so low that a single device would take decades to generate a statistically significant number of soft errors. In order to circumvent this limitation, real-time (unaccelerated) SER (RTSER) testing utilizes a very large number of devices in parallel to reduce the required test time. The number of soft errors observed is linearly proportional to the number of DUTs multiplied by test time (ie device hours). Testing can also be done at elevated altitudes where the higher neutron flux will generate a higher error rate. The system can either be a set of custom designed boards populated with a large number of the devices to be tested or a large server or other complex system (or array of servers/systems) containing a high part count.

Since RTSER testing typically involves a large number of devices and relatively long test times (weeks or months), a good test plan is crucial. It is extremely helpful to have some accelerated SER data (alpha particle and neutron) to get an estimate of the average failure rate. This estimate can then be used with the chi-squared statistics in annex C.2 to optimize the sample size and test duration so that the measured real-time SER will be valid to the desired confidence interval.

The procedures for non-accelerated RTSER and accelerated testing are similar. For real-time testing, the neutron flux is generally assumed to be a nominal value, based on the location of the ATE (see annex A). Alternatively, a measurement of the actual flux during the test may be made. This is a difficult measurement and beyond the scope of this specification. The alpha particle flux from the DUT packaging materials is assumed to be representative of the actual packaging. Separating the alpha and neutron contributions is complicated, requiring accelerated beam testing or system tests conducted at multiple locations. If RTSER results are to be used for SER estimates at other locations, this separation of effects is required. The minimum test procedures are listed separately below.

4.1.2 Guideline

The test method described below defines the requirements and procedures for RTSER testing without a radiation source, i.e., only the natural ambient background radiation due to terrestrial cosmic rays and alpha particles from packaging and chip materials. Accelerated SER testing with alpha particles, high-energy neutrons/protons, and thermal neutrons are discussed in **5**, **6** and **7**, respectively.

4.1.3 Scope of test method

This test method can be used to test large arrays of SRAM or DRAM memory, and can be adapted for use with other types of components, such as microprocessors. The RTSER test algorithm and hardware must have allowances for separating actual radiation induced soft errors from errors induced by system noise. Since the RTSER test method does not discriminate between alpha particle and neutron induced soft errors, doing real-time tests on the same components in different environments, such as in a cave for shielding the terrestrial neutron flux, at high altitudes for enhancing terrestrial neutron flux, and thermal neutron shielding for shielding thermal neutrons (see **6.6**) allow the alpha particle SER contribution (which will be constant when in secular equilibrium) to be separated from the terrestrial high-energy and thermal neutron-induced SER [10].

4.1.4 Goal of test method

The primary goal of RTSER testing is to obtain a well-defined estimate of the total soft failure rate for products/components using a uniform test methodology.

4.2 Test facilities and equipment

4.2.1 Basic electrical test requirements

The basic RTSER test requirement is to monitor each DUT's output vector and continually verify that the measured output matches the expected output vector or by using built-in self-test (BIST) features. A vector could simply be a pattern of data stored within the memory array of a DUT, or a stream of data generated as an operation or sequence of operations performed by the DUT on an input vector. The latter would be relevant for logic devices such as microprocessors. If the vector from the DUT does not match the expected vector, then a soft error may have occurred. The system consists of the input stimulus generator and response recorder that is designed to accommodate the specified device. Testing requires some sequence of writing data to the DUT, reading the data back, comparing the output data to the written data, and tabulating the number of detected errors.

4.2.2 DUT board hardware

RTSER testing requires a DUT board capable of supporting a large number of DUTs. Several DUT boards may be used in a single system. The boards can be controlled by a computer driven system or on a board controller that monitors and communicates with the DUTs during the test interval.

4.2.3 Test hardware

The test cables should be short enough and designed with the proper shielding to allow sufficient test speeds without electrical noise problems. If this is not possible, then on-board controllers should be used to allow high-speed operation of the DUTs and low speed communication off-board. The ATE should be capable of being configured to do both static and dynamic testing.

The following features are also desirable:

- 1) the ability to adjust and monitor the temperature of the DUTs or at least the ambient in which the DUT boards are located;
- 2) the ability to monitor power supply current of individual DUTs to check for latchup (preferably the ability to individually remove power from latched-up DUTs should also be provided);
- 3) if knowledge of the thermal neutron contribution is of interest, the ability to shield the DUT enclosure from background thermal neutrons to determine their contribution to the SER (see 7);
- 4) operation at the rated core cycle for the DUT. If this is not possible due to power consumption issues, the deviation should be noted in the final report.

4.2.4 Test software

The basic requirements for a RTSER DUT test system software are as follows:

- 1) Create test conditions for the DUT. A suite of test patterns (or benchmarks) should be selected that represents the intended operation of the DUT. In general, the test program for memories or arrays of latches should include patterns of ones, zeros and more complex variations, such as internal checkerboards, alternating rows and alternating columns to determine if the component has any preferred data states that are more robust or can be affected by nearest neighbors.
- 2) Identify and record any errors based on the selected test conditions. If an error does not go away when the component is rewritten or power cycled (powered down and then powered up), then it is a hard or intermittent fail. Hard fail events should be noted in the final report with an explanation of the source (e.g., a latent defect in the DUT, an early life fail, a power supply malfunction, etc.).
- 3) Provide adequate fault coverage and failure bit mapping (or analysis of output results). This is effective in distinguishing multiple independent failures from a cluster of nearest neighbor upsets from a single multi-cell upset caused by a single energetic particle (MCU). If a redundancy latch is hit and brings a defective row or column back into a repaired memory array, the signature of the error pattern should be distinguishable from a normal SCU or MCU. Likewise, if latchup occurs in a memory array, the signature of that event (typically inducing a large number of contiguous failing bits) should be uniquely distinguishable.
- 4) Initialization of control devices and rudimentary functional checks. Any upset of the control devices or power supplies should be distinguished from upsets of the DUT.
- 5) Select operation mode (dynamic or static operation) and provide resetting capability. For example, static testing of memory would be to write a test pattern once and store it for an extended period before reading the pattern back out. Dynamic testing of memory would involve writing once and then reading continuously or interleaving write and read operations at a specified operating frequency.
- 6) Provide error detection and logging. If the embedded ECC capabilities of the DUT are being enabled, the user must understand the details of the ECC operation (e.g., code, error registers, bit interleaving, etc.)
- 7) Data analysis and logging while the test is in process. This is required to help separate independent events due to multiple particle hits from single events that upset multiple cells. (Note: This is less of a concern for real-time SER than accelerated SER due to the lower flux levels, but should not be ignored.)
- 8) Ability to distinguish and report different soft error types (e.g., single memory cell upset, multiple cell upsets, latchup, functional interrupts from hits on the address or control registers, etc.). See 2 for definition of types of soft errors.

4.3 Testing procedures

4.3.1 Pretest preparations

4.3.1.1 Sample selection

Component variability for RTSER is generally small for components produced with the same masks and fabrication steps. The system user must be sure that components tested are equivalent to actual baseline production components, because manufacturers may make process/design changes affecting SER without changing the component's designation or advising users of the changes.

In general a minimum requirement to establish a product's RTSER is to run the test with roughly equal numbers of nominal devices from at least three different baseline lots. If a product is tested that has on-board error-correction codes/circuits (ECC), tests should to be run under two conditions, both with ECC enabled and with ECC disabled if possible. The presence of ECC and its on/off status during each data collection run must be included in the final report. (Note: In general, ECC is effective at masking single-bit cell upsets. But it will be ineffective with non-cell related events such as neutron-induced latchup or other single-event functional interrupts).

4.3.1.2 DUT preparation and orientation

The DUT package used for the RTSER test must be identical to the package used for production components. This is critical for the alpha component of RTSER. If a finned heat sink is required, this can have an impact on the neutron flux reaching the DUT. Since there is some angular dependence for high-energy neutrons (more high energy neutrons have normal incidence to the Earth's surface - see **A.5**), the DUTs should be mounted horizontally to expose them to the maximum flux where the tester does not dictate otherwise. Care must be taken in considering the path of atmospheric neutrons in the real-time SER setup and the effects of building shielding. For example, vertical stacking of DRAM DIMMs that are each oriented in a horizontal position would cause a neutron to traverse many DRAMs before reaching the final device (see [11] for discussion of neutron attenuation through DUT cards). The possibility of generating secondary particles as well as the attenuation of flux could lead to anomalous results. Therefore, the orientation of the DUTs in real-time SER testing should avoid this. If this is not possible, an attempt should be made to note any differences in SER FIT between the top and bottom devices. Ideally, where other constraints do not exist, the testing location should also be done on the top floor or roof to avoid building shielding effects. Finally, the orientation of the DUTs and stacking of DUTs should be noted in the final report. If heatsinks are used, then their geometry (e.g., thickness, fin height and number, etc.) and material should be described in the final report. If the user also intends to do accelerated beam testing (Sec 6), the orientation of the beam should be similar to the RTSER testing.

4.3.1.3 Load DUT

Place the desired population of DUTs on each DUT board and run the test program to verify proper operation of all the DUTs. Make necessary adjustments to system and DUTs to insure that the test program executes flawlessly on all DUTs in the test system.

4.3.1.4 Effective neutron flux at the test location

When performing real-time SER testing, it is necessary to make estimates based on the amount of building shielding and the terrestrial neutron flux (see annex A). Measurement of the actual neutron flux is beyond the scope of most experimental programs. The results should be normalized to the reference high energy neutron flux (see annex A) in the final report for purposes of standardization. An estimate of sensitivity to thermal neutrons should also be made using thermal neutron shielding for part of the experiment (see 7.6).

If the testing is to be done at high altitude, several factors should be taken into consideration when designing the experiment.

- 1) The cosmic ray dosimetry method and how it is monitored. If the facility has a dosimeter, it should be used but is not mandatory. (See annex A for the expected neutron flux at the test location).
- 2) The electrical power features and stability of the facility. The test setup often requires an independently stabilized uninterruptible power supply to run the test. Note that the overall power consumption for a large sample size can be significant. Make sure that the facility can provide the required power with good stability.
- 3) The lab should be protected against electrostatic discharge from lightning (i.e., presence of a Faraday cage, a lightning rod, etc.)
- 4) The environmental conditions that influence cosmic ray flux and how they are monitored (i.e., temperature, hygrometry, average pressure, average accumulation of snow, etc). An assessment of the impact of the variation of these environmental conditions (either important or insignificant) should be noted in the final report. If variation is determined to be insignificant, an average condition can be used in the final report. General guidance on the threshold for significant variation is a 50% impact on measured SER. Annex A details the impact of altitude and barometric pressure. As a quick rule of thumb:
Example 1 — a 40mmHg drop in atmospheric pressure (which is a significant change in weather conditions), will lead to a 50% increase in neutron flux.
Example 2 — based on typical values of snow density ($\sim 0.4\text{--}0.5 \text{ gm/cm}^3$), the reduction in neutron flux due to attenuation by snow on a roof is approximately 50% for 5 feet of snow.
- 5) It is convenient to have real-time monitoring of the experiment remotely through Ethernet access, as well as a remote reset function so that full-time staffing is not required.

4.3.1.5 DRAM and SRAM testing

At the minimum, data patterns must include a logical (external) checkerboard pattern and its complement, alternating by address and by bit. This will average out any asymmetry in SER behavior and represent actual application of the device. Read and write cycles should be selected so that all the elements of the DRAM or SRAM circuit (sense amps, storage capacitor or latches, decoders, multiplexers, etc.) are vulnerable to upset.

If the design supports a broad frequency range and different circuit elements will show different soft error rates as a function of frequency, care must be taken in selecting the core clock. A recommended solution is to run the RTSER test at a nominal frequency defined either by the tester capability or the product specification sheet to get a calibrated overall upset rate. Since the RTSER results can be frequency dependent, the nominal frequency used and how it was selected should be noted on the final RTSER report. Accelerated SER testing (see 5, 6 and 7) can then be used to determine the frequency dependent upset rate of the various circuit elements.

4.3.1.5 DRAM and SRAM testing (cont'd)

For those DRAM and SRAM designs that support a standby or reduced power mode (i.e., read and write operations are not allowed, but the device is expected to maintain its memory), a fraction of the real-time SER testing time should be dedicated to this mode of operation. The final report should include the estimate of SER from this mode vs. normal operating mode.

4.3.1.6 Other device testing

It might not be appropriate to use real-time SER testing procedures on all device types. Memory devices are good candidates because these devices are dominated by the core array and it is possible to capture and log all cell related upsets. Likewise, any FPGA or ASIC technologies using a high SRAM or DRAM content would be good candidates. On the other hand, not all upsets in logic devices will propagate to the output. This will depend on the static and dynamic design elements used. Therefore, an estimate of the expected fail rates should be made initially and the counting statistics discussed in annex B should be used to determine if a real-time SER test is appropriate for a device. Likewise, use of systems with large memory installations (like super-computers or server data-centers) might be appropriate for RTSER measurements. However, the user should be aware of confounding effects that happen at the system level (see 4.4).

4.4 Differences in real-time soft error tests and actual end-user observed fail rates

While the error rates determined from real-time SER testing are representative of device performance under real-life radiation conditions (both alpha particle and atmospheric neutrons), the results are not necessarily directly applicable to end user system applications. In addition to the customer environmental conditions that can be accounted for using annex A (i.e., geomagnetic location, altitude, building construction, etc.), other factors that need to be taken into consideration in translating real-time SER FITs to actual end user error rates include (but are not limited to):

- 1) Geometry of end user system (e.g., Are components stacked? Are they above or below the system board? Are the system boards stacked? Are the system boards oriented parallel or perpendicular to the background radiation? etc.)
- 2) How are errors detected (e.g., by ECC or by comparing read data to write data)? Are all errors reported? For example, are hardware ECC errors reported to error registers? If multiple errors occur within a short period of time, will error registers be overwritten, losing information about earlier errors?
- 3) How is determination made between a soft error event and signal integrity/noise, weak cells, hard fails?
- 4) What measures are taken to prevent multiple counting of a single event? For example, if hardware ECC corrects the error for the user but leaves the write-correct to a slower software operation, will the same event be counted multiple times (i.e., many hardware reads to same address before software corrects the data in memory)?
- 5) Can multiple errors from a single event be distinguished from single errors from multiple events?
- 6) What types of errors are masked by software error handling codes of the application?
- 7) What fraction of errors will be over-written before they are read? (Highly sensitive to application software.)
- 8) What fraction of errors will not be reported because they are not utilized by the application? This includes both unutilized memory as well as memory written to but never read.
- 9) Is the end-system using standard packaging or heat sinks (i.e., is the device packaging used in the system the same as the packaging used in the test configuration)?

5 Accelerated alpha-particle test procedures

5.1 Background

5.1.1 Introduction

Uranium and thorium impurities and their daughter products found in trace amounts in the various production and packaging materials as well as ^{210}Po contamination of lead and tin emit alpha particles. Alpha particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This charge disruption can be collected at pn junctions (much like charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. This section deals with the method of determining a component's sensitivity to alpha particle radiation from accelerated experiments.

5.1.2 Scope

This section deals strictly with SER induced by alpha particles and the techniques of using intense alpha particle sources to accelerate the alpha SER and use the ratio of this source emissivity to the package emissivity in order to determine the device alpha SER. The alpha flux is independent of altitude, and is only a function of the type, location, and amount radioactive impurities present in the component or its package.

Alpha particle SER data cannot be used to predict high- or low-energy neutron cosmic-ray-induced failure rates. Conversely, neither can high-energy neutron nor low-energy neutron SER data be used to predict alpha-induced failure rates. An overall assessment of a device's soft error sensitivity is complete ONLY when the alpha AND high- and low-energy neutron induced failure rates have been accounted for.

5.1.3 Safety issues

All of the accelerated test procedures involve the use of ionizing radiation sources that are potentially hazardous. Proper safety and monitoring procedures are essential for tests utilizing these sources.

Test hardware and parts may become contaminated with radioactive material when recoil fragments or larger fragments of the radioisotope escape the alpha source encapsulation. Good ventilation should be provided as some unsealed alpha sources may emit radon as a decay product. When not in use, alpha sources should be stored away from personnel as most alpha sources also produce low-level gamma radiation. Alpha sources should be handled with care even though external alpha emission is not hazardous (alpha particles have insufficient energy to penetrate the dead layers of the skin). Alpha emitting contaminants are extremely hazardous if inhaled or swallowed as alpha particles damage living tissues inside the body. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and the applicability of and compliance with local, state and Federal/National regulatory limitations. Gloves should also be used in handling the source to prevent accidental contamination of other locations. The user should check if a license is required to operate a source used in this study and will need to go through a compliance process that is beyond the scope of this spec. (Each country or state will have its own regulations.)