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Procedure for Characterizing Time- Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics

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PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

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PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

Foreword

This document is intended for use MOS integrated circuit manufacturing. It describes a test procedure for estimating the acceleration parameters of “wear-out” or Time-Dependent-Dielectric Breakdown (TDDB) of ultra-thin ($t_{ox} < 5$ nm) gate oxides. This document also describes robust techniques to detect breakdown and analysis methods for ultra-thin dielectric films that exhibit large tunneling currents and soft breakdown. It includes one informative annex on supplemental data analysis.

The purpose of this document is to describe test procedures for characterizing the reliability of ultra-thin gate oxides. It does not specify acceptance or rejection criteria for any of the described procedures.

The material contained within this standard is formulated under the cognizance of JEDEC 14.2 Committee and approved by the JEDEC Board of Directors.

PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

(From the JEDEC Board ballot JCB-03-16, formulated under the cognizance of the JC-14.2 Committee on Wafer Level Reliability)

1 Scope

This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or “wear-out” of thin gate dielectrics. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. Unlike highly accelerated ramp tests that are designed to be extremely fast and performed at the wafer-level, the constant voltage test procedure may be conducted over long periods of time. It may be applied at the wafer-level or with packaged devices.

For ultra-thin films breakdown can be difficult to detect. Ultra-thin films exhibit large tunneling currents and soft or noisy breakdown characteristics; special techniques must be used to detect breakdown under these circumstances.

This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

2 Overview

This document describes a constant voltage stress (CVS) test used to obtain acceleration parameters required to predict Time-Dependent Dielectric Breakdown (TDDB) of ultra-thin gate dielectrics used in advanced CMOS microelectronics.

It has been observed that breakdown in ultra-thin SiO₂ films ($t_{ox} < 5$ nm) becomes “soft” or noisy. At the breakdown event abrupt changes in current may not occur and device breakdown is difficult to detect. This document describes special methods for soft breakdown detection.

The complete CVS test procedure includes four sub-tests. First, a pre-characterization test is performed to determine operating points required by the CVS test. Second, a pre-CVS test is performed to remove damaged capacitors prior to starting the CVS test. Third, the CVS test is conducted, and finally, a post-CVS test is performed to confirm that a valid failure has occurred during the CVS test.

Several parameters are recorded as a result of the test including time-to-breakdown (t_{bd}), charge-to-breakdown (Q_{bd}) and the accumulation of stress-induced leakage current (SILC).

3 Terms and definitions

The following symbols are used in this document. They have been listed alphabetically for the convenience of the reader.

A_{oxide} (cm²) Oxide gate area.

E_{ox} (V/cm) E_{ox} is the oxide electric field. The general formula for E is:

$$E_{ox} = V_{ox} / t_{ox}, \quad (1)$$

where V_{ox} is the oxide voltage and t_{ox} is the oxide thickness. t_{ox} must be determined by a consistent, documented method. It is important to point out that the applied voltage is not necessarily the voltage across the oxide. Ultra-thin oxides exhibit quantum confinement effects and gate electrode depletion effects effectively reducing the voltage across the oxide. The method of determining t_{ox} or a reference to the documented standard must be included in the data report.

E_{bd} (V/cm) The estimated oxide electric field just before oxide breakdown. (see Annex).

I_{bd} (A) Oxide current measured just before oxide breakdown.

I_{comp} (A) The maximum current of the voltage-forcing equipment. Often the user can specify a compliance limit for a particular test.

I_{leak} (A) An optional pre-test leakage current at which the device is considered a yield failure.

I_{meas} (A) The measured oxide current.

I_{SILC} (A) The stress-induced leakage current measured at V_{SILC}. This value is measured and compared during the constant voltage test if the stress interruption method is used to detect breakdown.

I_{use} (A) The typical measured current through the oxide at the normal use voltage.

I_{stress} (A) The oxide current measured during the CVS test.

I_{previous} (A) The previously measured oxide current.

3 Terms and definitions (cont'd)

J (A/cm²) The oxide current density calculated by dividing the oxide current by the oxide area (A_{oxide}).

Q_{bd} (coulombs) The accumulated charge in coulombs that passed through the oxide prior to breakdown. Q_{bd} is defined as:

$$Q_{bd} = \int_{t=0}^{t=t_{bd}} I(t) dt \quad (2)$$

where t is time. The Q_{bd} is calculated as the integral from t = 0 to t = t_{bd} where t_{bd} is the time of the last measurement just prior to breakdown.

q_{bd} (C/cm²) The accumulated charge density is calculated as:

$$q_{bd} = \frac{Q_{bd}}{A_{oxide}} \quad (3)$$

t_{bd} (s) The recorded time at oxide failure.

t_{int} (s) The time that stress is applied before the stress is interrupted and I_{SILC} is measured during the stress interruption technique for detecting breakdown.

t_{meas} (s) The time interval for measuring the stress current (I_{stress}) during the constant voltage test.

t_{ox} (nm) Physical thickness of gate oxide.

t_{record} (s) The time interval for recording current measurements (I_{meas}) during the constant voltage test.

t_{wait} (s) The wait time after stress is interrupted before I_{SILC} is measured during the stress interruption technique for detecting breakdown.

V_{SILC} (V) The voltage at which the stress-induced leakage current (I_{SILC}) is measured.

V_{stress} (V) The oxide stress voltage.

V_{use} (V) The test voltage that is applied during pre- and post-test to determine device validity. This voltage is usually the power supply voltage or use voltage of the technology.

4 Constant voltage test procedure

4.1 Test configuration

The CVS test may be performed either in inversion or in accumulation. The capacitor test structure must be carefully selected depending on your product requirements.

For ultra-thin oxides (with $t_{ox} < 5$ nm), there is evidence that the driving force for dielectric breakdown is the gate voltage (voltage difference between the Fermi level positions in the anode and cathode) and not the oxide voltage (voltage difference between the top of the conduction bands in the anode and cathode). It is therefore important to minimize any voltage drops in the substrate and gate wiring due to series resistance that may lead to errors in the actual applied gate voltage.

For inversion testing the test capacitor must be bounded by a diffusion layer that provides the necessary minority carriers. The resistive path from any point in the inverted layer to the diffusion layer should be kept to a minimum to minimize voltage drops and hence errors in the actual voltage applied across the dielectric. For PMOS/P-poly capacitors tested in inversion, there is also a voltage drop due to the depletion region in the p^+ gate electrode that must be considered.

The test capacitor should not have contacts or probe pads over the thin oxide region. Compressive stress caused by probing pads over oxides can result in device damage and inaccurate defect density measurements.

In order to determine the voltage acceleration parameter γ and the thermal activation energy required to extrapolate product lifetime from accelerated stress conditions, the CVS test is performed at several voltages and temperatures. Although log-normal statistics can be used to fit the failure distribution, Weibull statistics are recommended. The parameter γ is the slope of the $\ln(t_{63})$ vs. V_{stress} plot. t_{63} is the modal value of the Weibull distribution. To determine the thermal activation energy, it is necessary to perform the test at several temperatures. Stress voltages are selected to provide reasonable test times.

Note that the extrapolated product lifetime must also take into consideration the difference in area between the test devices and the product. It is recommended that at least three different test structure areas be used in characterizing the area dependence of time-dependent dielectric breakdown. One of the properties of Weibull statistics is a shift of the distribution with device area. Area scaling of time-to-breakdown, T_{BD} , can be defined as follows [1]:

$$\frac{T_{BD1}}{T_{BD2}} = \left[\frac{A_2}{A_1} \right]^{1/\beta}$$