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Application Specific Qualification Using Knowledge Based Test Methodology

JESD94B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Introduction

The solid state device industry manufactures devices that are used in a wide range of applications. Consequently, the accelerated stress portion of the qualification regime used to assess the reliability performance of these devices should be customized to reconcile their design and functionality to the range of end use applications, based upon knowledge of the customer's end use application conditions, expected use environment, life time requirements, potential failure mechanisms, and associated failure models. The practice of using prescribed reliability stress test conditions, durations, sample sizes, and acceptance criteria may be inappropriate, especially with the ever-evolving applications and material sets found in the solid state device industry. The historically prescribed stress tests may either produce false failures or not accelerate valid failure mechanisms because the stress conditions do not correlate appropriately to the actual use environment.

APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY

(From JEDEC Board Ballot JCB-15-34, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The method described in this document applies to all application specific reliability testing for solid state device with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go/no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments.

The purpose of this document is to provide a method for developing an application specific reliability evaluation methodology based on the use conditions the solid state device is expected to experience in the field. It assumes that the failure mechanisms and models, relevant to the product being tested, are a known entity.

2 Terms and definitions

acceleration factor (A, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvin, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used instead of the symbol A.

2 Terms and definitions (cont'd)

environmental relative humidity: The relative humidity in the area immediately surrounding a specified component in an application.

environmental temperature cycle: A temperature cycle in an application resulting from environmental temperature changes.

environmental temperature range: The temperature range found in the area or enclosure surrounding an application.

field lifetime: (1) The anticipated time a product will last in the field determined solely by its ability to function.

(2) The anticipated time a product will be in use in the field determined by need rather than by its ability to function.

minicycle: A temperature cycle in an application resulting from a small degree of change in the operational temperatures (e.g., due to PC program variations, a typical minicycle may have up to 5 °C change).

nonoperating lifetime: The length of time that a component is not operating in an application.

NOTE The nonoperating lifetime may be calculated by subtracting the power-on-hours (POH) from the field lifetime.

operating lifetime: The length of time that a component is expected to function in an application at or below the predicted failure rate, stated in power-on-hours (POH).

operating temperature cycle range: The temperature range of a component caused by power cycling.

power cycle: A temperature cycle in an application resulting from cycling power on and off.

NOTE For applications with transient states such as mini-cycle, hibernation, standby, or systems with redundant or cyclic states, power on and off phases may require additional delineation for requirements computation.

shipping environment: The effects to which a component may be exposed while being shipped. Potential effects include temperature, relative humidity, and radiation.

shock and vibration condition: The shock and vibration experienced by an application in manufacturing, shipment, operation, and user handling (user transportation and/or regular operation).

2 Terms and definitions (cont'd)

storage environment: The effects to which a component may be exposed while being stored in a nonoperating state. Potential effects include temperature, relative humidity, and radiation.

storage lifetime: The length of time that a component is in storage prior to usage in an application.

use conditions: The various stages to which a component may be exposed starting from manufacturing and processing through shipping, storage, and useful life.

NOTE 1 The useful life normally consists of the operating, nonoperating, and storage lifetimes.

NOTE 2 Depending on the application and product usage, some of these stages may be more dominant and require additional consideration for requirements estimation.



Figure 1 — Illustration of typical use conditions

3 References

JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*

JESD85, *Calculation of Failure Rate in Units of FITs.*

JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*

JESD22-A110, *Highly Accelerated Temperature and Humidity Stress Test (HAST).*

JESD22-A118, *Accelerated Moisture Resistance-Unbiased HAST.*

JESD22-A102, *Accelerated Moisture Resistance-Unbiased Autoclave.*

JESD22-A101, *Steady-State Temperature Humidity Bias Life Test.*

JESD22-A103, *High Temperature Storage Life.*

JESD22-B110, *Mechanical Shock – Component and Subassembly*

JEP131, *Process Failure Modes and Effect Analysis (FMEA).*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits.*

JEP143, *Solid State Reliability Assessment and Qualification Methodologies.*

JEP148, *Reliability Qualification of Semiconductor Devices based on Physics of Failure and Risk and Opportunity Assessment.*

IPC/JEDEC9701, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*

IPC/JEDEC9703, *IPC/JEDEC Mechanical Shot Test Guidelines for Solder Joint Reliability*

IPC/JEDEC9704, *Printed Circuit Assembly Board Strain Gage Test Guidelines*

SEMATECH White Paper #99083810A-XFR, *Use Condition Based Reliability Evaluation of New Semiconductor Technologies.*

SEMATECH White Paper #99083813A-XFR, *Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages.*

4 Knowledge based test method flow

A typical flow of a knowledge based test method is shown in Figure 2. For a given device, a supplier will determine its potential use conditions from manufacturing to shipping it to the end-user as well as its exposure to environmental settings in its useful life (indoor and outdoor). Some of the requirements may be extracted from market expectations or provided by customers for some specific applications. Aspects of system design may also be introduced in the use condition definition. Once that exercise is completed, failure mechanisms and corresponding failure modes shall be determined (JEP131 or similar sources); appropriate reliability models and acceleration factors (JEP122 and JESD91 respectively or similar documents) shall be implemented or new ones may need to be developed; and lastly a qualification strategy shall be established. Finally, device performance from the application of stress tests (JESD22-Axxx and JESD22-Bxxx) would be reported. These steps are outlined in clause 5 thru clause 11.

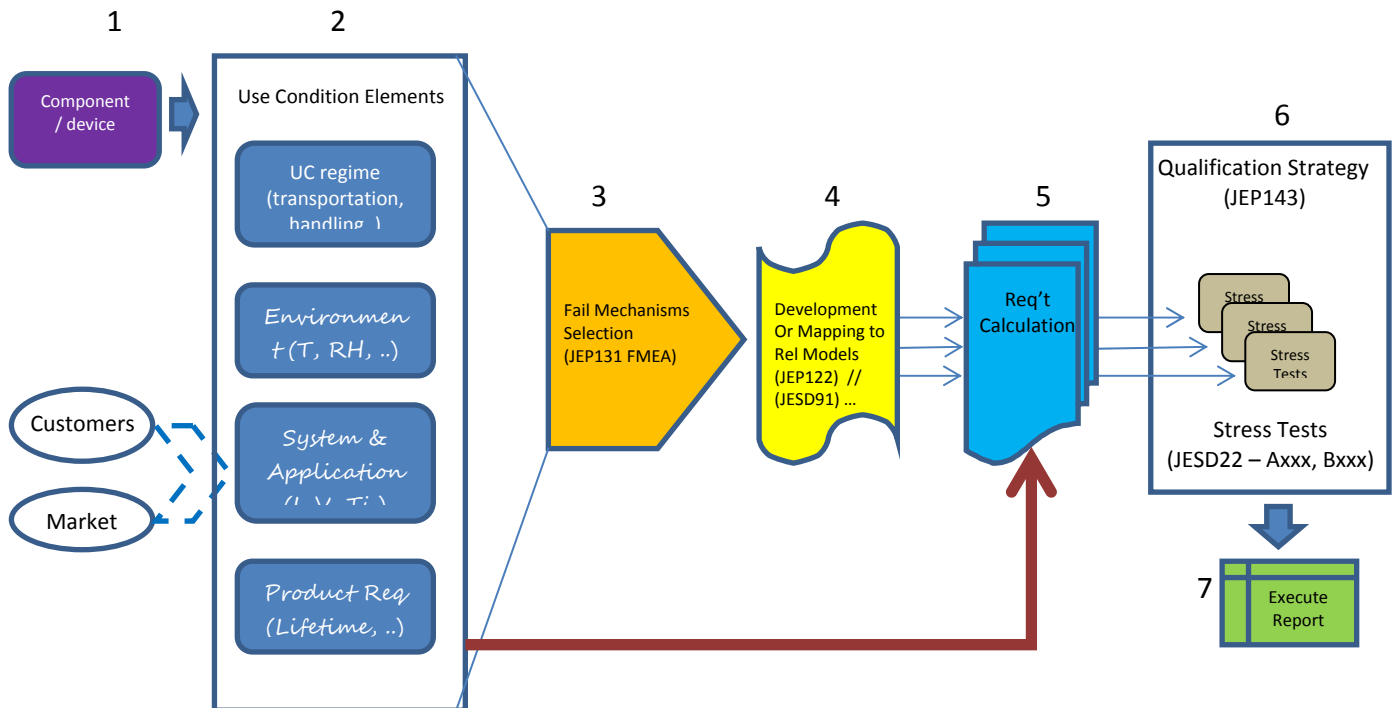


Figure 2 — Basic step by step flow of the knowledge based test method

5 Determining application specific test requirements

It is necessary to determine the range of use conditions the solid state device will experience in the application space(s). This information may be obtained from customer requirements or based on general knowledge of the typical use, operation and reliability requirements for the product's market segment.

Additionally, an application's lifetime may be determined by financial, regulatory, safety, and market driven requirements. Some examples of financial requirements include product warranty and the costs associated with developing, sustaining, and depreciation of the equipment and tools necessary to enable a device. Product lifetime may also be determined by its end use application (for instance, consumer, industrial, business, etc.)

5.1 Identification of environmental, lifetime and manufacturing conditions

Key information required to develop an application specific qualification test sequence is the identification of use condition regimes that comprise of the environmental, lifetime and manufacturing conditions to which the solid state device will be exposed. Since there are various types of attributes with differing levels of availability and complexity, it is recommended to organize these attributes in different levels in order to prioritize data acquisition, clarify supplier and customer understanding, and facilitate use of knowledge based test method.

For illustration, one approach would be to establish Category 1 as data that is fairly static, common to many applications, and readily available in publications. Category 2 would be attributes that are traceable to specific market or product groups. Finally, Category 3 would be the attributes that may be design or product specific with significant variability. A potential list of these attributes, with respective categories (1, 2, 3) suggesting their level of availability and complexity, is:

Category 1: (mostly environmental)

- ambient relative humidity and temperature range, pollution, use or exposure to hazard materials/chemicals, radiation of the environment where the device operates
- storage conditions (temperature and humidity)
- shipping conditions (temperature, humidity and shock / vibration, radiation)

5.1 Identification of environmental, lifetime and manufacturing conditions (cont'd)

Category 2: (design and operating elements)

- expected operating lifetime of the device in power-on hours
- actual number of weekly operating hours
- device operating voltage and electric field
- number of environmental and power cycles experienced per day
- number of minicycles and sleep cycles per day, if applicable
- expected assembly layout and assembly conditions (board cross section, heat sink attachment, surrounding devices, reflow profile)

Category 3: (application specific elements inclusive of mitigation options)

- number and duration of transient states (hibernation, standby) that governs the behavior of the application
- cumulative end of life failure rate
- early life failure rate
- mitigation options – customized design (e.g., via location/stack), geometry and configuration features (e.g., assembly, enabling solutions) and material selection

Dependent on the application and the failure mechanism of interest, only some of these attributes may play a critical role in the customization of the test sequence, so it is important to understand their relative impact to the reliability model and qualification requirements.

6 Identification of potential failure mechanisms and corresponding failure modes

Key failure mechanisms and corresponding failure modes can be identified in several ways, but one of the most effective is to perform a failure mode and effect analysis (FMEA) on the product of interest, see JEP131. Another method that can be used in conjunction with performing an FMEA is the modeling of the product. Based on its design and material attributes, the model can predict any thermal or mechanical interactions in the application environment, which could initiate stresses and associated product failure.

If unknown failure mechanisms are found during test, it is important to characterize it properly as defect-driven or intrinsic. On the former, mitigation steps to ensure process stability may be required to address them. For the latter, appropriate acceleration model experiments may be designed and performed in order to establish models, activation energy and test duration. JESD91, Method of Developing Acceleration Models for Electronic Component Failure Mechanisms, describes how to accomplish this task.

7 Selection and application of reliability models

Once the potential known failure modes and mechanisms are identified, the appropriate failure models should be selected. Appropriate models and activation energies for the range of known failure mechanisms are discussed in JEP122, Failure Mechanisms and Models for Silicon Semiconductor Devices.

For a given reliability, model, acceleration factor (AF) can be computed by the ratio of time necessary for a given device population to fail under its expected useful life over the corresponding time to fail when the devices are subjected to the application of stress tests. Following sections provide examples of stress test use. Annex A offers illustration for AF computation.

8 Qualification strategy - Selection of stress tests and test hardware

Stress tests shall be selected based on targeted failure mechanism and the expected failure modes. JESD47 relates many process attributes and the accelerated tests used for stress testing. JEP122 and JEP143 have extensive information on various reliability stress testing models, concepts and methods.

Test hardware shall be representative of the expected application design with respect to key attributes, yet capable of discerning stress test failures. Considerations for interactive effects with the assembly may include: expected component layout, circuit board cross-section, and heat sink requirements. For the most representative test results, the test hardware build should simulate the anticipated manufacturing assembly, test, burn-in and shipping conditions. The test hardware may be either actual product or test vehicles designed to simulate product attributes. Dependent on the failure modes and mechanisms of concern, a test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms. A valid test hardware strategy should take this into account.

9 Application of stress test conditions and durations

Stress test conditions shall be selected that accelerate the failure mode of interest, but do not produce false failure modes that are artifacts of the test conditions and not representative of the product's use environment. Selection must be based on solid state device material properties versus use conditions and test acceleration factors.

The reliability stress conditions should be bounded so that they are not beyond the physical capability of the product materials. These physical limits may dictate upper and/or lower limits on the stress conditions selected. If the actual use condition requirements are beyond the physical limits of the product materials, testing should be performed at those limits to demonstrate product incompatibility for the specific application. Material properties of interest include, but are not limited to, coefficient of thermal expansion, modulus and elongation as a function of temperature and creep properties.

The test duration shall be based on the failure model selected, the acceleration factor for that mechanism, the failure rates that need to be verified for the product, including early life and end of life. It should reflect the performance goals that might be specified under functional/safety, customer demand, or projected lifetime. Depending on these goals, there may be instances where acceleration factor is small causing test time to be long. If the test duration is unreasonable, alternative stress test conditions or methods should be explored.

The sample size used needs to be sufficient to support the failure rate requirements. Potential ways to reduce sample size such as lifetime characterization for failure rate approaches may be preferable for cost saving purposes. JESD74, Early Life Failure Rate Calculation Procedure for Electronic Components, and JESD85, Calculation of Failure Rate in Units of FITs are the applicable documents for failure rate and distribution determination, based on stress test results.

If the failure rate requirement is low, the quantity of parts tested could be large. The test sequence should simulate the handling, shipping and use conditions for the application, and as such, combination of tests may be warranted.

Finally, considering the variability of use condition attributes, a stochastic approach to understand the overall sensitivity of the parameters and their effect on qualification requirements for reliability is recommended. This type of strategy could also provide robust assessments on product lifetime that reconciles probability of use conditions with the range of reliability performance. For instance, consideration of environmental and operational conditions should capture all appropriate sources, from location (indoor/outdoor) to product features (internal/external, ventilation, etc.). Product lifetime could be constructed from a distribution that captures all recorded temperatures and their variability. Annex B provides an actual illustration of this approach. Examples of potential stress tests are given in 9.1, 9.2, 9.3, 9.4, and 9.5.