

JEDEC STANDARD

Radio Front End-Baseband (RF-BB) Interface

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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RADIO FRONT END-BASEBAND (RF-BB) INTERFACE

Foreword

This standard establishes the requirements for an interface between Radio Front End (RF) and Baseband (BB) integrated circuits (IC). These requirements are intended to ensure that multiple RF and baseband IC vendors can collaborate and design a common IC interface allowing each of the devices to work with each other. Included are requirements for electrical signaling, link layer state machines and register map definitions.

Introduction

This interface is a high-speed, low latency digital interface that has been defined primarily for wireless local area networking applications but can be used for other RF to BB links such as used in metro area networking and wide area networking applications. This interface allows the radio front end of a wireless network controller to be separated from the base-band and MAC device(s) by up to 50 cm. A typical example is to connect a radio front end in the upper (screen) portion of a laptop computer to a base-band device on the motherboard. Lower power options are also defined for shorter distances.

The basic interface consists of three differential signals totaling to six pins. A clock signal must be provided by the FED on one pair of pins along with two pairs of pins for data transfers from the FED to BED and in the reverse direction. A separate pair is dedicated for either direction. Figure 1 illustrates the pin connections for the RF-BB interface. An optional pair of pins can be assigned for a return clock from the BED to the FED.

The interface provides three, concurrent, logical channels for communication: a streaming data channel, a control channel and a register access channel. Each of these channels can be programmed by the BED, subject to the constraints indicated by the FED in its capability registers. The FED determines the clock frequency, while the BED can select the data frame formats subject to the constraints indicated by the FED in its capability registers. Registers defined in clause 7 control the streaming rate, data and control word sizes, and optional configurations.

I.1 Features

- 1) Flexible interface usable for multiple standards
- 2) Low power duty cycle data and clock sub-modes
- 3) Low analog complexity
- 4) Low latency data transfer configurable down to 20 ns¹
- 5) Raw link bandwidth of up to 2.3 Gb/s depending on clocking speed
- 6) Double data rate (DDR) clocking
- 7) Rejects 30 dB of interference with the use of differential signaling
- 8) Low radiated emissions from differential signaling
- 9) Clocking frequency (up to 1.1GHz) under the control of FED
- 10) Supports 0-50 cm line lengths

¹ Streaming-data latency is affected by the number and word bit length of the streaming words in one RF-BB interface frame. Fewer streaming words and smaller word bit lengths will result in lower latency, but will also lower the bandwidth efficiency of the interface. If bandwidth is abundant, then the latency can be configured to be around 20 ns.

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RADIO FRONT END–BASEBAND (RF-BB) INTERFACE

(From JEDEC Board Ballot JCB-05-105, formulated under the cognizance of the JC-61 Committee on Wireless Interface Network.)

1 Scope

The normative information in this standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material.

This document addresses the following interface topics:

- 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks;
- 2) RF-BB Link layer: bits, clock-data synchronization, power modes;
- 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC;
- 4) RF-BB Interface Registers.

This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

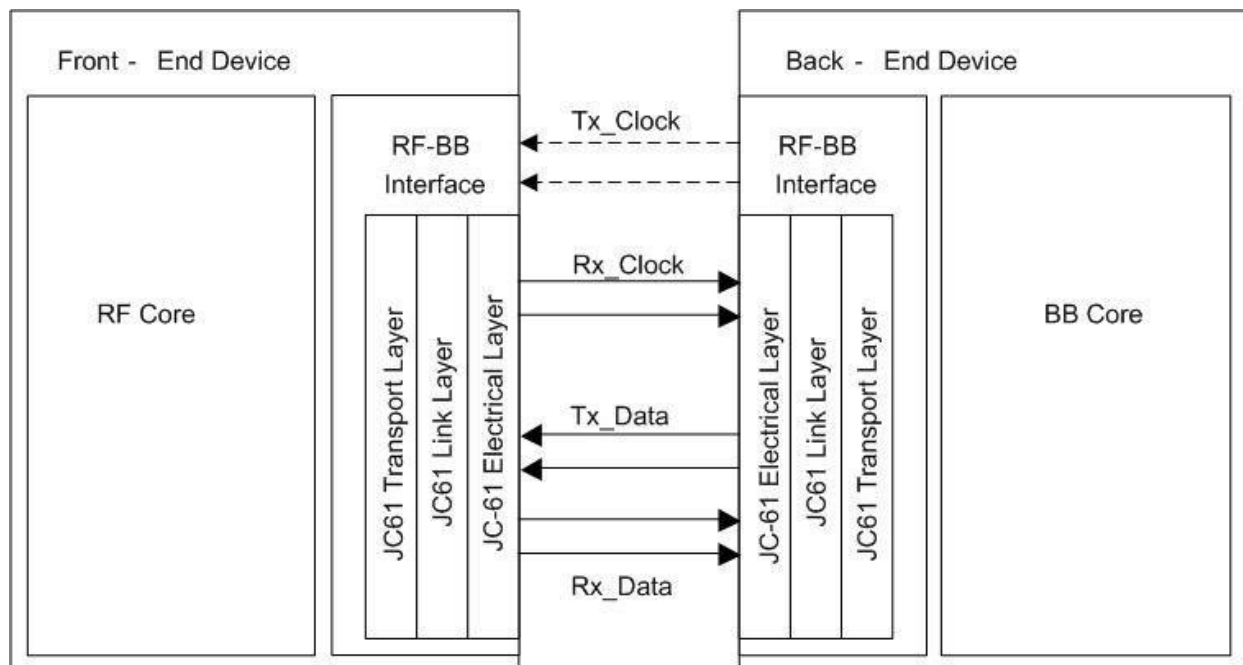


Figure 1 — Interface layer diagram

Specific implementations of this interface are beyond the scope of this standard.

2 References

2.1 Informative

The following standards contain provisions that, through references in the text, are informative in this standard. At the time of publication, the editions indicated were valid. All standards are subject to revisions.

IEEE Std 802.11-1999, *Wireless Local Area Network (WLAN) Standards*, (Reaffirmed 2003)

TIA/EIA-644-A, *Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits*, February 2001.

JESD8-13, *Scalable Low-Voltage Signaling for 400 mV (SLVS-400)*, October 2001.

High Speed Serialized AT Attachment rev. 1.0; 29 August 2001 Specification.

HyperTransport™ I/O Link Specification Revision 1.03.

2.2 Normative

JEP106M, *Standard Manufacture's Identification Code*, May 2003

3 Terminology

For the purpose of this standard, the following terms, definitions, acronyms and abbreviations apply.

3.1 Terms and definitions

base-band frequencies: Low frequencies neighboring and including 0 Hz. These frequencies are represented with real In-Phase (I) and Quadrature (Q) parts or together as a complex signal. In this document, the word “base-band” will usually refer to a base-band processor (part of the BED in this interface).

common mode voltage: The average voltage level of the two signals on a differential line.

deskew: The act of aligning a clock with incoming data so that the clock edge can be used to latch data in the middle of the data eye.

frame: A group of serial bits consisting of a Sync Mark, Header, and one or more of the following fields:
1) streaming data, 2) control data, 3) register data, and 4) parity bit.

radio: A device or a group of devices that translates the information bandwidth between base-band and the radio frequency portion of the spectrum.

Rx-direction: Direction of Receiving from Front End Device to Back End Device.

Rx-link: Data link that moves data from Front End Device to Back End Device.

TX-direction: Direction of transmitting from the Back End Device to the Front End Device.

TX-link: Data link that moves data from Back End Device to Front End Device.

little endian: The format in which the least significant bit (LSB) of a word is transferred first and the most significant bit is transferred last.

3 Terminology (cont'd)

3.1 Terms and definitions (cont'd)

big endian: The format in which the most significant bit (MSB) of a word is transferred first and the least significant bit is transferred last.

TX_IN: Single-ended combination of TX/TXN analog signals received by FED.

TX_DATA_VALID (FED): Indication the TX_IN signal contains data for the FED Transport Layer.

TX_CLK: Clock signal from FED Link Layer to the FED Transport Layer that has been deskewed for maximum data eye opening on TX_IN.

RX_OUT: Single-ended serial data from the FED Transport Layer to the FED Link Layer which is synchronized with CLK_90.

RX_DATA_VALID (FED): Indication that the RX_OUT signal contains data for the FED Link layer.

CLK_90: 90-degree-offset clock signal provided by the FED Link Layer to the FED Transport layer to synchronize outgoing RX_OUT.

LINK_REQUEST: Indication that the Transport layer requires FED Link Layer services. This could also serve as a data clock request.

DESKEW_REQUEST: Indication that the Transport layer needs the Link to deskew incoming data and clocks. One possible reason to send this is because of some CRC error seen in the Transport layer.

LINK_STATUS: This signal reports that the Link is ready, or not ready. It is related to DESKEW_STATUS as well.

TX_CM_DET: Indication to the FED Link layer from the FED Electrical layer that a minimum active common mode voltage has been detected on the TX/TXN lines.

RX_EN: Enables the RX/RXN drivers on the FED Electrical Layer to transmit.

CLK_0 (FED): FED: Single-ended zero-phase-offset clock from the FED Link layer for the CLK/CLKN driver in the FED Electrical Layer.

CLK_0 (BED): BED: Single-ended clock signal from the BED Electrical Layer to the BED Link Layer corresponding to CLK/CLKN.

CLK_EN: Enables the CLK/CLKN drivers on the FED Electrical Layer to transmit.

CLK_DET: Indication to the BED Link layer that the BED Electrical Layer has detected a minimum active common mode voltage on the CLK/CLKN lines.

RX_CM_DET: Indication from the BED Electrical layer to the BED Link Layer that a minimum common mode voltage was detected on the RX/RXN lines.

RX_IN: Single-ended analog BED signal corresponding to the received differential RX/RXN signal in the BED Electrical Layer.

TX_EN: Enables the TX/TXN drivers in the BED Electrical layer to transmit.

TX_OUT: Single-ended data to be driven differentially on TX/TXN.

3 Terminology (cont'd)

3.1 Terms and definitions (cont'd)

TX_DATA_VALID (BED): Indication from the BED Transport Layer that TX_OUT contains valid data for the BED Link Layer.

RX_DATA_VALID (BED): Indication that signals from the BED Link layer on RX_IN contains data for the BED Transport Layer.

3.2 Acronyms and abbreviations

BED	Back-end device. Relative to the RF-BB interface, the BED is the baseband processor.
BW	Bandwidth
CLK, CLKN	The Clock differential pair
DDR	Double data rate clocking. Data clocked on both the rising and falling edges of the interface clock signal.
Def	Default Value
FED	Front-end device. Relative to the RF-BB interface, the FED is the radio frequency device.
Flight Delay	Propagation time of the signal on a transmission line
HDR	Header
MAC	Medium access Control
PHY	A Wireless LAN, MAN or PAN physical layer interface . The bottom layer of the JC-61 RF-BB is called “electrical layer”.
RF	Relating to a Radio Frequency device.
RF-BB	Relating to the interface between a Radio Frequency device and a Baseband processor.
Rx	Receive
RX, RXN	The Receive differential pair signals
TX, TXN	The Transmit differential pair signals
Tr	Rising or falling transition time. The time it takes to transition from one defined signal level to another.
Tx	Transmit
UI	Unit interval or bit interval. For double data rate clocking, the unit interval is half of a clock cycle.
VCM	Common mode voltage.

3 Terminology (cont'd)

3.2 Acronyms and abbreviations (cont'd)

WLAN Wireless data packet network in a general sense, including IEEE 802.11, wireless Metropolitan Area Networks, including IEEE 802.16; and wireless Personal Area Networks, including IEEE 802.15.

3.3 Numeric representation

The numerical values are in decimal unless indicated otherwise. The values specified in decimal are coded in natural binary unless otherwise stated.

4 Electrical layer

The JC-61 physical data link is designed to deliver a scalable level of bandwidth and interconnect distance performance between a Front-End IC (FED) and a Back-End IC (BED) using a robust LVDS signaling variant similar to HyperTransport™.

The physical layer can operate in one of four power modes – which are distinguished by different transmission impedance levels. The high power mode utilizes a standard differential source and load termination impedance of 100 Ω . This mode enables data links with transmission rates up to 2.3 Gb/s per data pair and up to a maximum distance of 50 cm at full rate.

The three low-power modes utilize higher transmission impedance to save driver power. These modes utilize nominal differential termination impedances of 200 Ω or 300 Ω , or high impedance, and are restricted for use with shorter interconnect distances and lower rates as listed in Table 3. For the third power mode, the interface is operated with asymmetric termination impedances utilizing a 100 Ω (differential) source impedance of the driver together with high impedance termination at the receiver. Due to the high amount of reflection possible in this type of line interface, only lower data rates can be supported. Power consumption is reduced in the asymmetric termination mode for lower data rates.

It is required to use one of the termination impedance modes. An optional device impedance discovery process is also available for switching to low power modes. At power-up the termination on the FED and BED can be decided a priori or both the devices can power-up in the 100 Ω mode and then switch modes via register access.

4.1 Electrical layer overview

The basic I/O interface consists of three differential signals that utilize a total of 6-pins on each device. Figure 2 illustrates a typical RF-BB interface with DDR clock sourced from FED to BED. Synchronous serial NRZ data links are provided in both directions between FED and BED. . An optional pair of pins can be assigned for a return clock from the BED to the FED.

The RF-BB interface is distinguished from other LVDS serial interfaces by its ability to signal in either direction a wake-up signal to a receiver side that is powered off – by using the power enable in the driver to raise the common mode voltage level at the line receiver input. When powered off, the driver will pull down the differential termination voltages to ground. When powered on, the driver will raise the common mode voltage of the termination to specified levels. This capability allows the implementer of an attached device to manage the power dissipation in the interface and system so that the total power is minimized when the interface and/or system components are not in active use.

4 Electrical layer (cont'd)

4.1 Electrical layer overview (cont'd)

The RF-BB interface standard also provides the option for Clock and Data duty-cycling modes where the Data drivers and Clock driver may be powered down between frames. The fast common mode signaling capability (i.e., Duty-cycling modes) of this interface may be used to conserve additional power when full data link bandwidth is not needed.

For example, in an RF-BB link configuration, when the (RF) FED is powered off, the base-band (BED) may power up the FED oscillator and interface by common mode signaling on the Tx Data link pins.

Similarly, when the interface is powered off in the RF (FED) and base-band (BED) devices, the FED may signal a power-on request by common mode signaling on the Clock pins.

The I/O data bandwidth is scalable to rates greater than 2.3 Gb/s by adding additional data-link pairs in the direction desired (see 5.7). Any additional data-link pairs operate synchronously using the single common source clock. Power management of an expanded data interface is accomplished the same way by using common mode signaling between the designated driver and receiver.

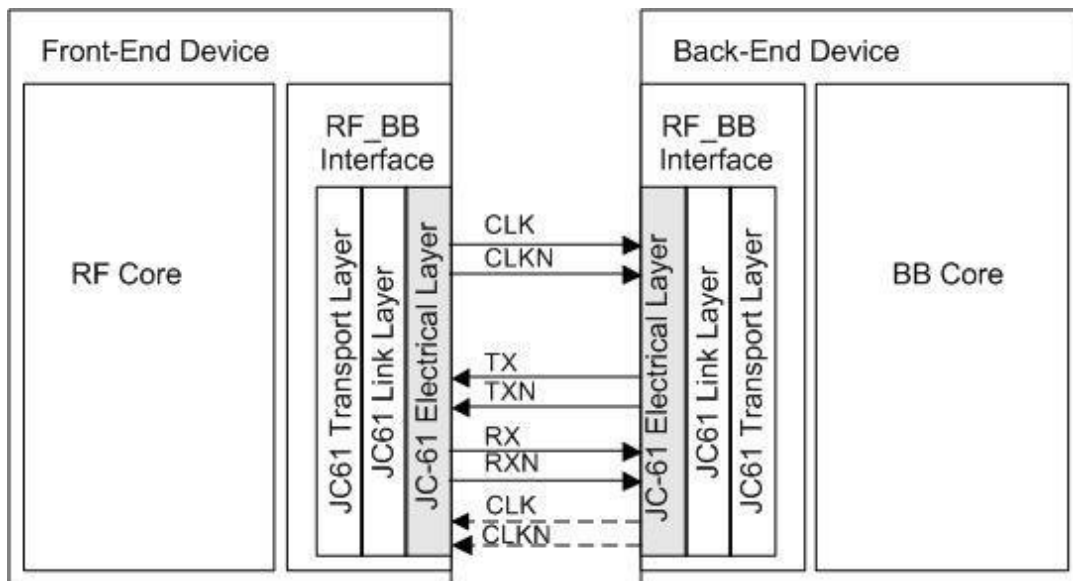


Figure 2 — Electrical Layer Connections

4.1.1 Common mode rise-time and detection delays

For the situation where duty-cycled power management options are not used, only the maximum total common-mode signal detection time is specified. Otherwise where duty-cycled power management options are used, the common mode activation rise-time and detection time delays are specified to be shorter than the maximum total common mode activation delay, in order to realize improved average power efficiency.

The Common Mode Activation Delay is defined as the total time required between the logic activation of the common mode power-up at the I/O driver cell to the detection of the common mode signal present at the I/O receiver cell logic.

4 Electrical layer (cont'd)

4.1.1 Common mode rise-time and detection delays (cont'd)

Maximum Common Mode Activation Delay shall be 100 ns, except when the optional duty-cycled modes are used.

In order to support low-overhead duty-cycled modes, the suggested driver maximum CMV rise time (20% to 80%) is 1 ns. The Common Mode Activation Delay time for these modes is required to be less than 10 ns.

4.1.2 Common mode noise

The RF-BB interface shall be designed to operate with Common Mode Noise levels between the driver and receiver of up to 200 mV p-p, including common mode DC offsets of up to 100 mV dc. The common mode noise may be anywhere in a bandwidth of DC to 200 MHz.

4.2 Power supply characteristics (informative)

The I/O supply is a single fixed supply with nominal VIO assumed to be in the range of +1.2 vdc to +3.3 vdc, excluding supply tolerance. Different supply voltages may be used for FED and BED devices with assurance that they will be compatible at the interface. Power supply characteristics provided in table 1 are for guidelines purposes only.

Table 1 — Link power supply characteristics

Parameter	Description	Min	Typ	Max	Units
VIO Nominal	Range of nominal I/O supply voltages supported for RF or BB devices	1.2		3.3	V
VIO Tolerance	Supply DC Tolerance	-10		+10	%
Supply Noise (External)	AC ripple noise peaks, DC to 10 MHz	-50		+50	mV
Typical driver current per pair*	100 Ω termination mode – High Power Mode 200 Ω termination mode – Low Power Mode 1 300 Ω termination mode – Low Power Mode 2		6.0 3.0 2.0		mA
Typical receiver current per pair*			1.0		mA
* These typical currents are not requirements; they are informative only and will depend on specific implementation details, including the current requirements of input/output pads and other supporting circuits.					

It is recommended that the RF-BB interface specifications support driver and receiver designs that consume zero supply current when in the sleep state.

4.3 Driver cell DC specifications

The DC specifications of the driver are valid and should be measured only when the circuitry has assumed steady-state conditions.

Figure 3 gives a reference circuit that can be used in ATE verification testing or simulations. The reference circuit utilizes ideal balanced DC termination resistance. Note that for drivers that support the low-power transmission options, it will be necessary to test with the optional higher impedance reference loads indicated in Table 2.

4 Electrical layer (cont'd)

4.3 Driver cell DC specifications (cont'd)

The DC specifications below apply directly at the transmitter output pins DO+ and DO-, and ensure that the driver circuits are adequately balanced and provide correct source impedance and correct differential and common mode output levels, from a DC perspective.

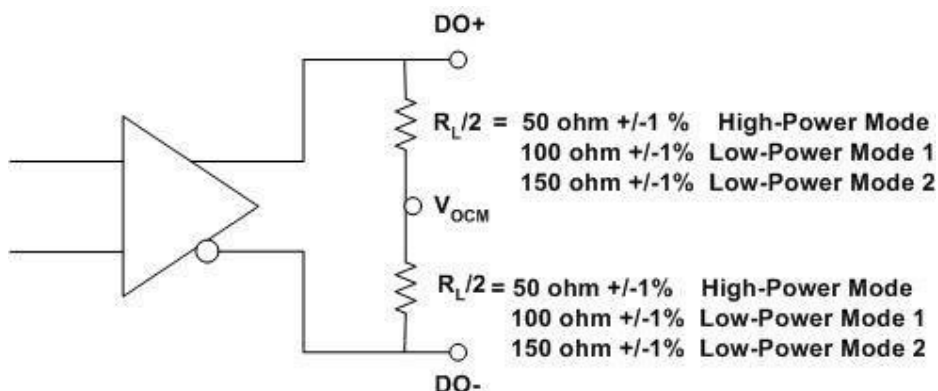


Figure 3 — DC Output reference system load

Table 2 — Driver DC Specifications

Parameter	Description	Min	Typ	Max	Units
Source resistance (each output leg)	High-power mode, Low-power mode 3	45	50	55	Ω
	Low-power mode 1	90	100	110	
	Low-power mode 2	112.5	150	187.5	
	Low-Power mode 3 (High Z)	37.5	50	62.5	
V_{OD}	Peak Differential output voltage ¹ - terminated modes	470	600	755	mv
	Low-power mode 2	400	600	900	
	Low-power mode 3		1200		
Change in V_{OD}	Change between logic "1" and "0" states	-20		+20	mv
V_{OCM} average	$(V_{OCM}^{11} + V_{OCM}^{00}) / 2$				mv
	High Power, Low power mode 1	495	600	715	
	Low power modes 2, 3	450		800	
Change in V_{OCM}	Change between logic "1" and "0" states	-20		+20	mv
Output impedance match	Absolute difference between logic "1" and logic "0" state output impedances	0		5	%

NOTE DC voltage specifications assume on-chip resistance calibration to +/-10% or better.

4.4 Driver cell AC specifications

These parameters place requirements on the driver under idealized load and add dynamic signal characteristics of the driver caused by signal transitions at the intended operating frequency and power supply limits. Since the specification supports a wide range of speed grades and interconnect/impedance options, the reference load and associated specifications are broken down into a number of "corner" limit cases that have specific recommended reference load circuits for ATE verification or simulation.

For all corner cases, the driver signal parameters associated are measured at the termination side of an idealized transmission line load relative to the average common mode voltage level at the termination.

4 Electrical layer (cont'd)

4.4 Driver cell AC specifications (cont'd)

Table 3 — AC reference system load characteristics

Case	Description	R_L	Max Clock Rate (MHz)	Line Length (cm)	Z_0 (Ω)	Line to Line Time Skew	C_L (pf)
1.	High-speed Long-length High-power	100	1150	50	50 (loss 1.2 dB)	<15 ps	2.0
2.	Med-speed Long-length High-power	100	600	100	50 (loss 1.5 dB)	<30 ps	4.0
3.	Med-speed Med-length Low-power 1	200	600	10 (PCB trace length)	100 (loss 0.3 dB)	<30 ps	2.0
4.	Med-speed Low-power 2	300	300	3.0 (PCB trace length)	130 nom.	<50 ps	2.2
5.	Low-speed Low-power 3 (100 Ω)	Hi-Z	200	5.0	50	<50 ps	4.0

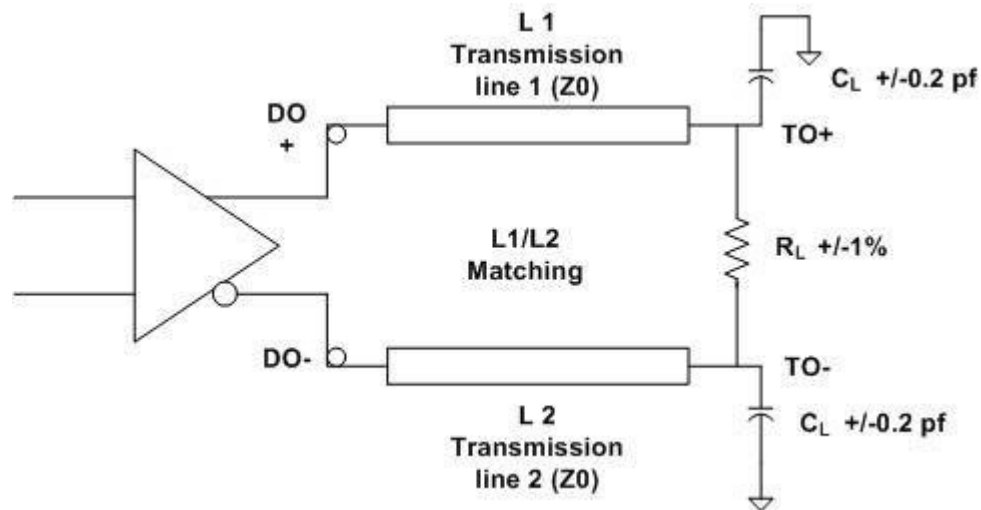


Figure 4 — AC reference system load

The AC reference system constitutes an ideal matched and balanced load, with appropriate skew tolerance on the complementary transmission lines. The characteristic line impedances (Z_0) of L1 and L2 for cases 1 and 2 shall be matched to within $\pm 2\%$.

For shorter interconnect distances, such as in cases 3, 4, and 5, the interconnections are likely to be controlled impedance traces on a PCB or module substrate. For these cases, the AC reference line impedance should be controlled to $\pm 10\%$ with matching of $\pm 5\%$ or better.

For case 4, the line is short enough to be considered a lumped trace capacitance. In this case, the combined driver output capacitance and receiver input capacitance is specified to be 4 pf maximum. Line impedance of 130 Ω $\pm 15\%$ shall be utilized for the reference load system.

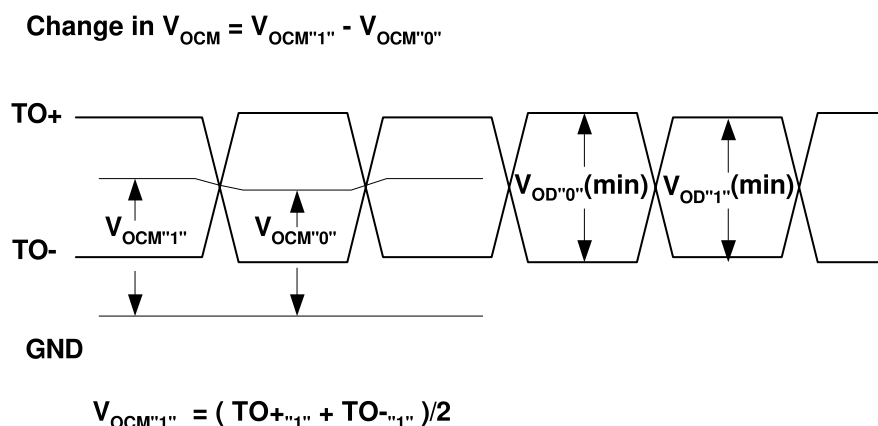
4 Electrical layer (cont'd)

4.4 Driver cell AC specifications (cont'd)

The five “corner” cases above are used within clause 4. These were selected to represent safe upper capability limits of speed, line type, and loading for RF-BB applications of practical interest. AC and timing specifications are given for these corner cases, with the understanding that some relaxation of specifications are possible for ranges between these corner case limits. The capacitive loading represents a model of typical IC + PCB pad node capacitance and may be exceeded in some implementations. Similarly, actual line lengths may exceed those in Table 3. For those cases, de-rated speed performance levels should be determined with appropriate design simulations. Suggested interconnect line specification limits for RF-BB interface designs corresponding to these corner cases are given in 4.6.1 and include wider tolerances than those called out here for the driver AC reference load circuits.

4.4.1 AC signal level parameters

AC signal level parameters are measured at designated clock speed at the end of the reference system transmission line at each terminal, TO+ and TO-, with respect to ground. The common mode voltage is an average of the complementary load voltages at TO+ and TO- for each logic state, as indicated in Figure 5. Since the waveform may have overshoot and undershoot due to impedance mismatches, the differential output signal level is measured with respect to the minimum points in the settled state of the waveform, as indicated.

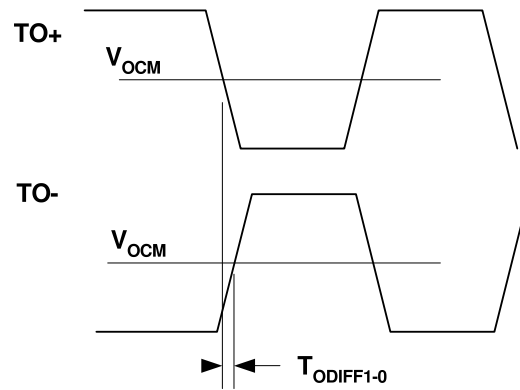


NOTE These parameters measure the effects of AC impedance imbalances, and non-linearity when coupled to an appropriately balanced and loaded line.

Figure 5 — Driver AC waveform parameters

4.4 Driver cell AC specifications (cont'd)

4.4.1 AC signal level program (cont'd)



$$T_{ODIFF} = (T_{ODIFF1-0} + T_{ODIFF0-1})/2$$

NOTE The parameter T_{ODIFF} defines the allowable differential skew as measured in a single-ended fashion at the average V_{OCM} level (midpoint) of the transition of the true signal and complement signal at the termination. It is the average difference for both logic 0-1 and 1-0 transitions.

Figure 6 — Differential output skew

4.4.2 Driver AC specifications

The specifications in Table 4 are broken down relative to the speed capabilities and corner case loading assumptions defined in Table 3.

Table 4 — AC specifications

Parameter	Description	Min	Typ	Max	Units
Output L (each leg)	IC output inductance with IC package			4.0	nH
Output C (each leg)	IC output pad capacitance with IC package Cases 1, 3, 4 Case 2, 5			1.8 3.0	pF
V_{OD}	Ave. (min.) peak differential voltage at termination Cases 1. & 2 Case 3. Case 4. Case 5.	250 350 250		650 750 800 1300	mV
V_{OD} change	Change between “1” and “0” states	-75		75	mV
V_{OCM}	Ave. output common mode voltage High Power, Low Power Mode 1 Low Power Modes 1 & 2	400 250		800 800	mV
V_{OCM} change	Change between “1” and “0” states	-50		50	mV
Rising and falling edge rate	Between +/-50 mV points on differential signal Case 1. Case 2. Case 3. & 4 Case 5.	2.5 1.5 1.0 1.0		8.0 6.0 4.0 5.0	V/ns
Edge rate matching	Mismatch of rise and fall rates			5	%
T_{ODIFF}	Midpoint skew between “+” and “-” output signals Cases 1. & 3. Case 2. & 5. Case 4.			35 70 100	ps

4.5 Receiver cell specifications

4.5.1 Receiver DC specifications

The DC specifications below apply directly at the receiver input pins RI+ and RI-, and ensure that the receiver operates statically over a range exceeding the worst case input signal range of a RF-BB link. The receiver may have on-chip termination resistor, off-chip resistor, or a combination of these. The reference circuit below assumes that the differential termination is internal.

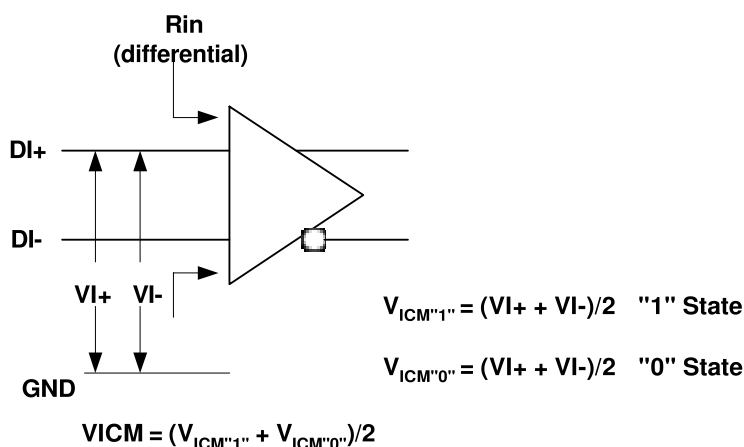


Figure 7 — Receiver reference circuit

Table 5 — Receiver DC specifications

Parameter	Description	Min	Typ	Max	Units
Differential input resistance	High-power mode Low-power mode 1 Low-power mode 2 Low-power mode 3	90 180 225 1000	100 200 300	110 220 375	Ω
Input voltages, VI+, VI-	Maximum allowable safe DC range at input terminal DI+ or DI-	-200		1200	mV
Differential input voltage	Peak magnitude $ (V_{I+} - V_{I-}) $ allowable, consistent with VICM and max safe limits	200		1300	mV
Change in diff. input voltage	Difference in amplitude from logic "1" to "0" state allowable in input signal	-100		100	mV
Input common mode voltage, VICM	Allowed VICM = $(V_{I+} + V_{I-})/2$ High Power, Low Power mode 1 Low power modes 2,3	360 200	600	860 900	mV

4.5.2 Receiver AC specifications

These parameters place requirements on the receiver, and are derived from the output parameters of the drivers and various interconnect characteristics. They include a parameter that defines the presence of common mode noise in a system between driver and receiver.

Input termination AC impedance specifications are provided and shall include the impedance tolerances for all configurations of external and on-chip terminations.