



ASSOCIATION CONNECTING  
ELECTRONICS INDUSTRIES®



# IPC/JEDEC-9702

## Monotonic Bend Characterization of Board-Level Interconnects

**This document version has been edited to include Addendum 1, May 2015:**  
This amendment provides a clerical correction to section 8.7, *Test Board Daisy-Chain Links*, which better expresses the intent of the IPC and JEDEC committees to recommend avoiding stress artifacts and to offer strategies to that end. Modified August 2016.

### IPC/JEDEC-9702

June 2004

A standard developed by IPC and JEDEC

2215 Sanders Road, Northbrook, IL 60062-6135  
Tel. 847.509.9700 Fax 847.509.9798  
[www.ipc.org](http://www.ipc.org)

2500 Wilson Blvd. Suite 220, Arlington, VA 22201  
Tel. 703.907.7559 Fax 703.907.7598  
[www.jedec.org](http://www.jedec.org)



**Documents**  
Document Sharing Hub

---

## The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

### Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

### Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

## Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

## IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee (TAEC) that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.  
Adopted October 6, 1998

## Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit [www.ipc.org](http://www.ipc.org) or call 847/790-5372.

Thank you for your continued support.



ASSOCIATION CONNECTING  
ELECTRONICS INDUSTRIES®



IPC/JEDEC-9702

# Monotonic Bend Characterization of Board-Level Interconnects

Developed by the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product Reliability Committee (6-10) of IPC and the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1)

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC  
2215 Sanders Road  
Northbrook, Illinois  
60062-6135  
Tel 847 509.9700  
Fax 847 509.9798

JEDEC  
Solid State Technology Association  
2500 Wilson Boulevard  
Arlington, VA 22201-3834  
Tel 703 907.7559  
Fax 703 907.7583



**Documents**

Document Sharing Hub

This Page Intentionally Left Blank

## Acknowledgment

Members of the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1) and the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product Reliability Committee (6-10) have worked together to develop this document. We would like to thank them for their dedication to this effort. Any document involving a complex technology draws material from a vast number of sources. While the principal members of the SMT Attachment Reliability Test Methods Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the JEDEC and IPC extend their gratitude.

### Product Reliability Committee

Chair  
Reza Ghaffarian, Ph.D.  
Jet Propulsion Laboratory

### JEDEC Reliability Test Methods for Packaged Devices Committee

Chair  
Jack McCullen  
Intel Corporation

### SMT Attachment Reliability Test Methods Task Group

Chair  
Reza Ghaffarian, Ph.D.  
Jet Propulsion Laboratory  
  
Vice-Chair  
Werner Engelmaier  
Engelmaier Associates, L.C.

### Technical Liaisons of the IPC Board of Directors

Peter Bigelow  
IMI Inc.

Sammy Yi  
Flextronics International

### SMT Attachment Reliability Test Methods Task Group

Mudasir Ahmad, Cisco Systems, Inc.  
Patricia J. Amick, Boeing Aircraft & Missiles  
Pierre Audette, Nortel Networks  
Jean Bobgan, Guidant Corporation  
Dr. John Kirk Bonner, Jet Propulsion Laboratory  
Mark Brillhart, Cisco Systems Inc.  
Nicole Butel, Agilent Technologies  
Srinivas Chada, Ph.D., Jabil Circuit, Inc.  
Phillip Chen, Northrop Grumman Canada Corporation  
Beverley Christian, Ph.D., Research In Motion Limited  
Thomas Clifford, Lockheed Martin Space Systems Company  
Yves Desrochers, Nortel Networks  
Howard S. Feldmesser, Johns Hopkins University  
Jean-Yves Gagne, Nortel Networks  
Mahendra S. Gandhi, Northrop Grumman  
Phil Geng, Intel Corporation

Denis Gignac, Nortel Networks  
Lavanya Gopalakrishnan, Ciena Corporation  
Michael R. Green, Lockheed Martin Space Systems Company  
Samy Hanna, AT&S Austria Technologie & Systemtechnik  
Hana Hsu, Mitac International Corporation  
Kim Hyland, Solectron Corp.  
Thomas E. Kemp, Rockwell Collins  
Vincent B. Kinol, Umicore America Inc.  
Gregg Klawson, General Dynamics - C4 Systems  
Dennis Krizman, Celestica  
Kuan-Shaur Lei, Hewlett-Packard Company  
James F. Maguire, Intel Corporation  
Wesley R. Malewicz, Draeger Medical Systems, Inc.  
John Manock, Lucent Technologies, Inc.  
Susan S. Mansilla, Robisan Laboratory Inc.

Lei L. Mercado, Ph.D., P.E., Intel Corporation  
Frank Mortan, Texas Instruments  
Keith G. Newman, Sun Microsystems Inc.  
Bob Ogden, Raytheon Systems Company  
Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information  
Mel Parrish, Soldering Technology International  
Kumar Pavuluri, Texas Instruments Inc.  
Mike Pfeifer, Motorola Inc.  
Sundar Sethuraman, Solectron Corporation  
Rocky Shih, Hewlett-Packard Company  
Vern Solberg, Tessera Technologies, Inc.  
Vish Sundararaman, Ph.D., Texas Instruments Inc.  
Vasu S. Vasudevan, Intel Corporation  
Dewey Whittaker, Honeywell Inc.  
Greg Wood, ACI EMP

# Table of Contents

|                                                      |   |                                                                             |    |
|------------------------------------------------------|---|-----------------------------------------------------------------------------|----|
| <b>1 FOREWORD</b> .....                              | 1 | <b>ANNEX A</b> .....                                                        | 9  |
| <b>2 INTRODUCTION</b> .....                          | 1 | <b>ANNEX B</b> .....                                                        | 12 |
| <b>3 SCOPE</b> .....                                 | 1 |                                                                             |    |
| <b>4 TERMS AND DEFINITIONS</b> .....                 | 1 |                                                                             |    |
| <b>5 SYMBOLS AND ABBREVIATED TERMS</b> .....         | 2 |                                                                             |    |
| <b>6 SAMPLING</b> .....                              | 2 |                                                                             |    |
| <b>7 APPARATUS</b> .....                             | 2 |                                                                             |    |
| 7.1 Universal Tester .....                           | 2 |                                                                             |    |
| 7.2 Strain Measurement Equipment .....               | 3 |                                                                             |    |
| 7.3 Continuity Monitoring Equipment .....            | 3 |                                                                             |    |
| <b>8 PROCEDURE</b> .....                             | 3 |                                                                             |    |
| 8.1 Component Sample .....                           | 3 |                                                                             |    |
| 8.2 Test Board Material .....                        | 3 |                                                                             |    |
| 8.3 Test Board Thickness and Metal Layer Count ..... | 3 |                                                                             |    |
| 8.4 Test Board Surface Finish .....                  | 4 |                                                                             |    |
| 8.5 Test Board Land Pads .....                       | 4 |                                                                             |    |
| 8.6 Test Board Layout .....                          | 4 |                                                                             |    |
| 8.7 Test Board Daisy-Chain Links .....               | 4 |                                                                             |    |
| 8.8 Board Assembly .....                             | 6 |                                                                             |    |
| 8.9 Storage .....                                    | 6 |                                                                             |    |
| 8.10 Strain Gages .....                              | 6 |                                                                             |    |
| 8.11 Set-Up Test Board .....                         | 6 |                                                                             |    |
| 8.12 Four-Point Bend Test .....                      | 6 |                                                                             |    |
| <b>9 FAILURE CRITERIA AND ANALYSIS</b> .....         | 7 |                                                                             |    |
|                                                      |   | <b>Figures</b>                                                              |    |
|                                                      |   | Figure 7-1 Universal Tester .....                                           | 2  |
|                                                      |   | Figure 8-1 Test Board Layout .....                                          | 4  |
|                                                      |   | Figure 8-2 Rectangular Package Orientation .....                            | 5  |
|                                                      |   | Figure 8-3 Single Package Daisy-Chain Configuration<br>(Example) .....      | 5  |
|                                                      |   | Figure 8-4 Strain Gage Placement .....                                      | 7  |
|                                                      |   | Figure 9-1 Interconnect Fracture Modes (Solder<br>Ball Array Devices) ..... | 8  |
|                                                      |   | Figure A.1 Example Configuration (PWB Thickness<br>= 1.00 mm) .....         | 9  |
|                                                      |   | Figure A.2 Example Configuration (PWB Thickness<br>= 1.55 mm) .....         | 10 |
|                                                      |   | Figure A.3 Example Configuration (PWB Thickness<br>= 2.35 mm) .....         | 11 |
|                                                      |   | <b>Tables</b>                                                               |    |
|                                                      |   | Table 7-1 Universal Tester Requirements .....                               | 2  |
|                                                      |   | Table 8-1 Recommended Test<br>Board Thickness & Layer Count .....           | 3  |
|                                                      |   | Table 8-2 Test Board Layout Requirements .....                              | 4  |
|                                                      |   | Table 8-3 Monotonic Bend Test Requirements .....                            | 7  |
|                                                      |   | Table B.1 Test Report Recommendations<br>(Equipment & Materials) .....      | 12 |
|                                                      |   | Table B.2 Test Report Recommendations<br>(Board Assembly) .....             | 12 |
|                                                      |   | Table B.3 Test Report Recommendations<br>(Test Results) .....               | 12 |