

3.12.2 Package-on-Package (PoP) and Internal Stacked Module (ISM)

General Rules for Pattern Development LPDDR2 PoP Design Guidelines (GLs)

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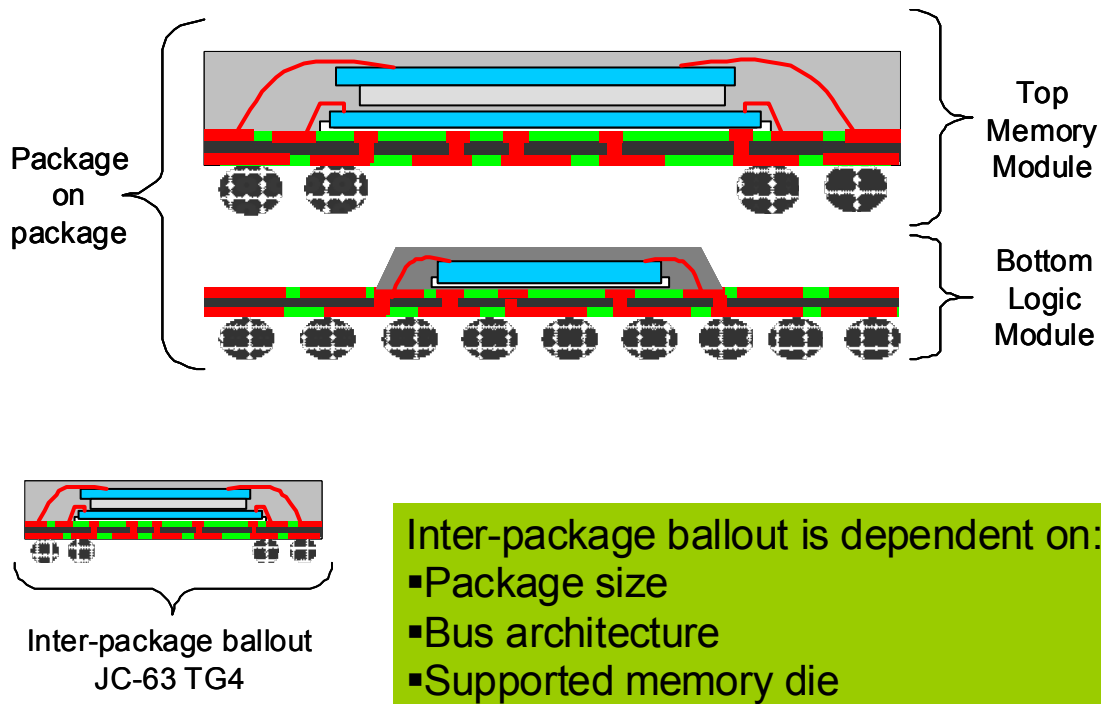


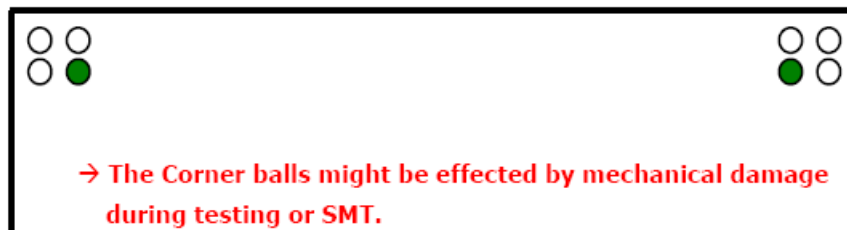
Figure 3.12.2-1 - Inter-Package Ballout

General Rules Used for Pattern Development

- "Consideration given to wire routing and layout to maximize performance
- "Consideration given to power and ground pairs to maximize performance
- "Alignment to silicon pad sequence standardization efforts for various technologies
- "Address & Data bus will be in sequential order where possible
- "Corner balls designated as NC - no connect - and should be used for mechanical stability."
- "Support multiple packages on a single test platform when possible
 - * Fixed placement of ground balls
 - * Strategic placement of ""RFU"" balls on larger package to support fewer
 - * balls on smaller package
 - * Outer row of larger package becomes inner row of smaller package

LPDDR2 PoP Design Guidelines (GL's)

- **GL1: VDD1/VDD2/VSS should be grouped together for good power delivery and match the silicon allocation and close location (Example: silicon contains these groups on top, center, and bottom of each side of die, package should reflect this distribution)**
- **GL2: 12PoP (0.5, 168ball) CA[4:0] should be reversed (vs silicon) as they wrap around ball package corners to provide better routing on memory top package.**
- **GL3: Assign 4 DU balls on the each corner. 3 would be acceptable w/ 4th ball as power delivery option if required, depending on design.**



- **GL4: Follow JEDEC PAD ordering to execute easy routing**
- **GL5: Number/location of Power/GND ball with matching ratio 1:1 (for every VSS/VSSQ, a matching VDD/VDDQ exists on 1:1 basis) To reduce the Power/GND Noise through balancing**

NOTE: Acceptable practice, actual ratio may vary depending on requirement

- GL6: Assign VDDQ / VSSQ as diagonal type to shield signal lines by power lines



- GL7: Assign CLK /CLK# differential signals side/side within row with paired order to reduce noise effect. DQS# /DQS diagonal placement coupled with VSSQ/VDDQ (on other two balls within 4-ball group) for good noise isolation



- GL8: Vref balls should be placed with 2ea/Ch. (DQ-Vref and CA-Vref on each side) Vss should be assigned to Vref ball by pair to minimize power noise Single Vref may be shared per ch. but may limit performance/ spec, such occurrence should be noted and validated by system analysis.



- **GL9:** ZQ ball should be assigned by 1ea/Channel. 1 ZQ pin can access 2 different dies using time interval method (Single ZQ ball shared with two die in stack)
- **GL10:** VDDQ/VSSQ/DQ ratio needs to be 1/1/4. (1/1/4 (25%) is minimum ratio requirement, actual silicon is 14/14/32 (43%))

NOTE: Depends on design requirements, more data simulation required to use this practice as a minimum. Higher ratio the better.

- **GL11:** minimize CA Length. CA ball group should be assigned at near area from Pad. The CS, CKE Balls might be place next to CA balls. (CS and CKE not as timing critical, so placement locate on side of CA channel vs in center may be acceptable)

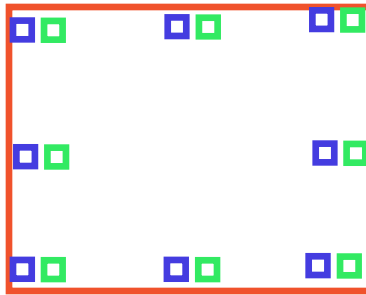
NOTE: Agree to minimize CA ball group trace length. No consensus on CS/CKE placement outside of CA channel

PoP Metric Examples

(used to evaluate new PoP proposals)

Example = 2 channel LPDDR2 PoP x32

- VDD1/2 count, GL 1, (8/10 – actual count respectively)
- VDD1/2 distributed per si score (16/16, 4 corners, 4 sides center)
 - Represents VDD1/2 group 



- Vref, GL 6 (2/channel, 4 total for 2 independent x32 channels)
- IO Power delivery ratio, GL 10, (VDDQ/VSSQ pair per byte) 2.75:1
 - This ratio based on total of 11VDDQ/VSSQ pairs per x32 channel broken down per Byte
- Differential signals, GL 7,
 - DQS/DQS# and CLK/CLK# - Next to each other on inner/outer rows vs inner row



TOP VIEW

11.00mm

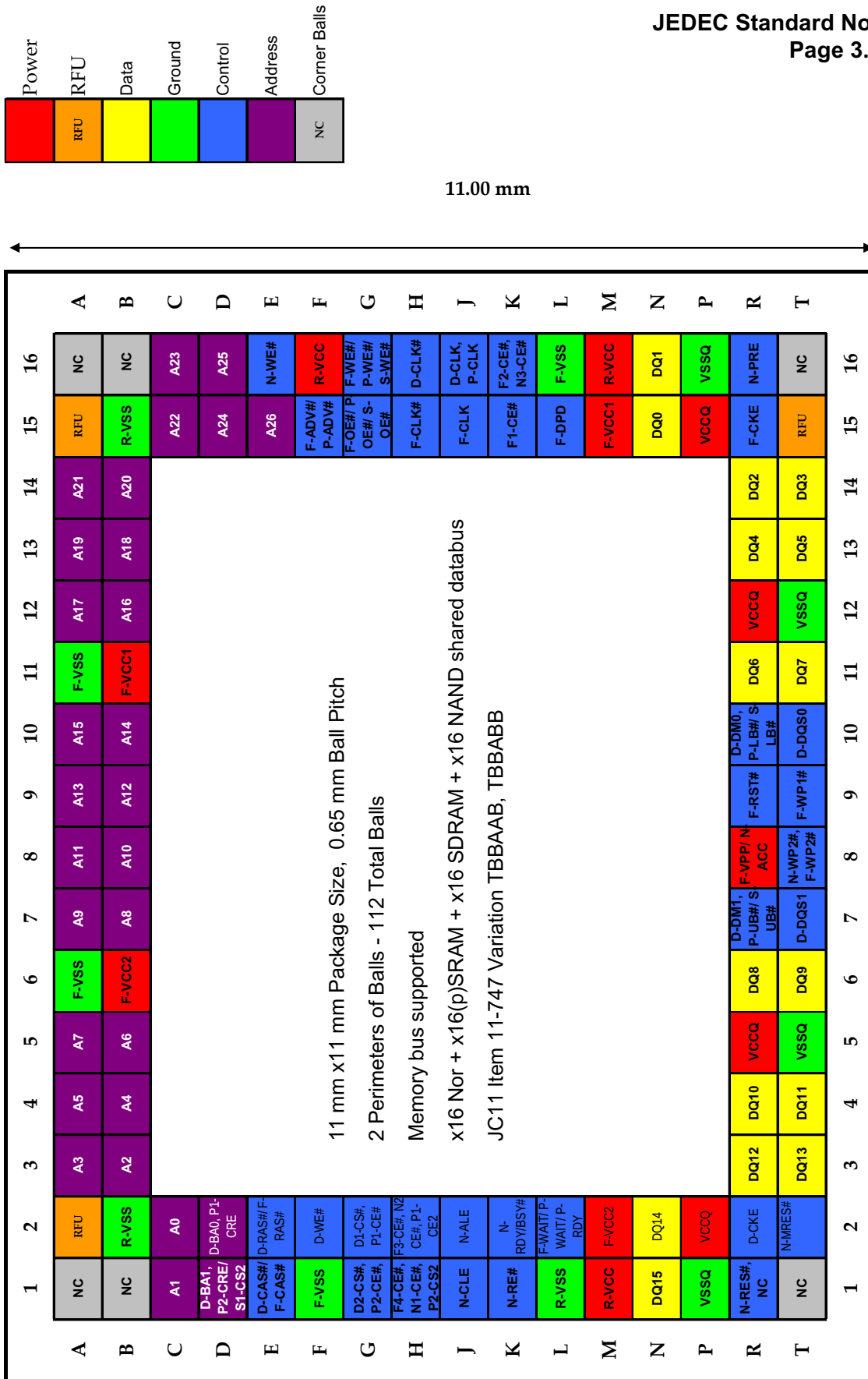


Figure 3.12.2-2
Ball Outline – 112-Ball BGA, 0.65 mm Pitch, 11 mm x 11 mm Package

11.00mm

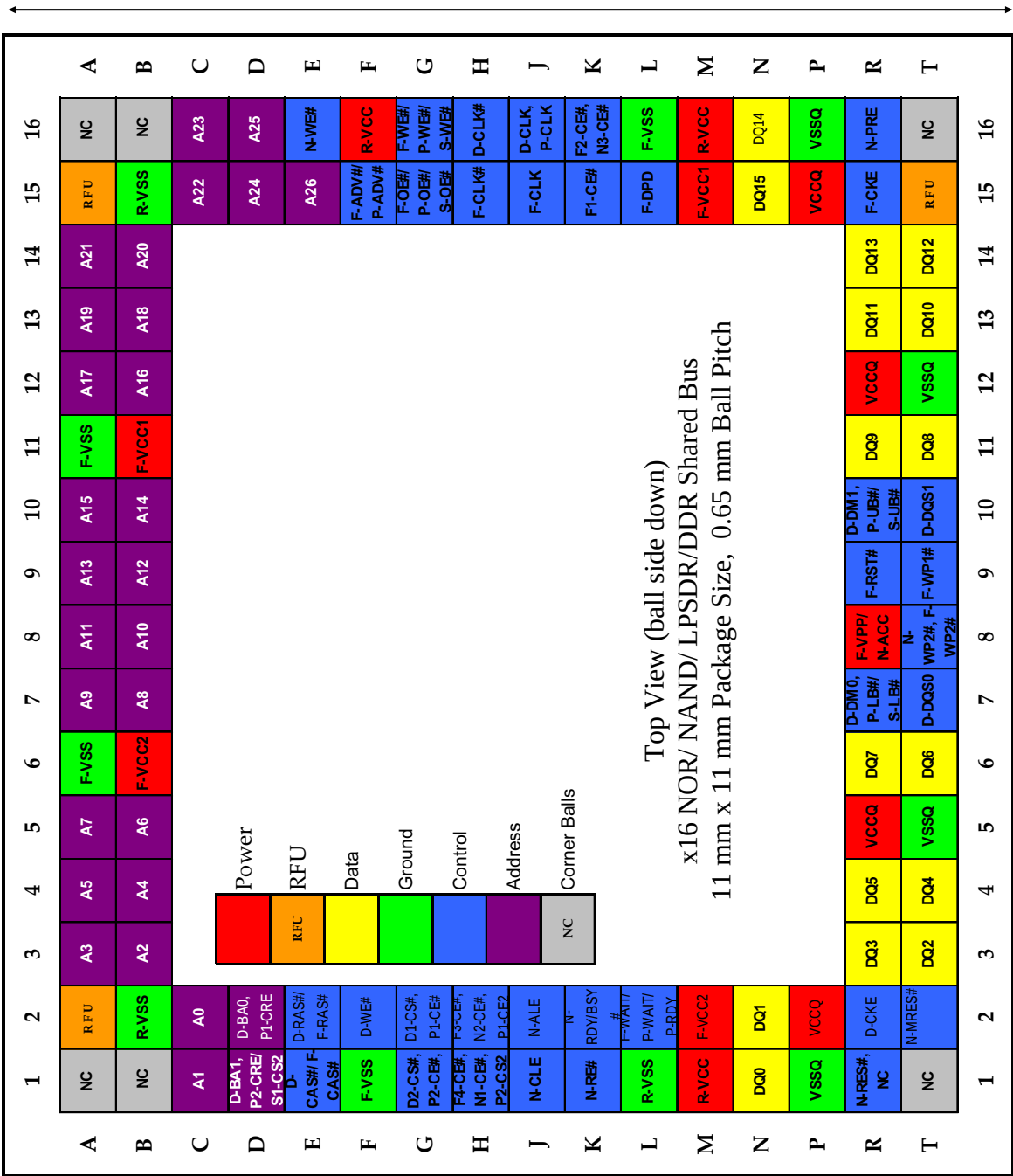


Figure 3.12.2-3
Ball Outline – Flipped DQ Sequence
112-Ball BGA, 0.65 mm Pitch, 11 mm x 11 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	RTU	A3	A3	B3	A2	R3	DQ12	T3	DQ13	A15	RTU	A16	NC		
B1	NC	B2	R-VSS	A4	A5	B4	A4	R4	DQ10	T4	DQ11	B15	R-VSS	B16	NC		
C1	A1	C2	A0	A5	A7	B5	A6	R5	VCCQ	T5	VSSQ	C15	A22	C16	A23		
D1	D-BA1, P2-CE#, S1-CS2	D2	D-BA0, P1-CE	A6	F-VSS	B6	F-VCC2	R6	DQ8	T6	DQ9	D15	A24	D16	A25		
E1	D-CAS#, F-CAS#	E2	D-RAS#, F-RAS#	A7	A9	B7	A8	R7	D-DM1, P-UB#, S-UB#	T7	D-DQS1	E15	A26	E16	N-WE#		
F1	F-VSS	F2	D-WE#	A8	A11	B8	A10	R8	F-VPPI, N-ACC	T8	N-WP2#, F-WP2#	F15	F-ADV#, P-ADV#	F16	R-VCC		
G1	D2-CS#, P2-CE#,	G2	D1-CS#, P1-CE#	A9	A13	B9	A12	R9	F-RST#	T9	F-WP1#	G15	F-OE#, P-OE#, S-OE#	G16	F-WE#, P-WE#, S-WE#		
H1	F4-CE#, M1-CE#, P2-CS2	H2	F3-CE#, N2-CE#, P1-CE2	A10	A15	B10	A14	R10	D-DW0, P-LB#, S-LB#	T10	D-DQS0	H15	F-CLK#	H16	D-CLK#		
J1	N-CLE	J2	N-ALE	A11	F-VSS	B11	F-VCC1	R11	DQ6	T11	DQ7	J15	F-CLK	J16	D-CLK, P-CLK		
K1	N-RE#	K2	N-RDY/BSY#	A12	A17	B12	A16	R12	VCCQ	T12	VSSQ	K15	F1-CE#	K16	F2-CE#, N3-CE#		
L1	R-VSS	L2	F-WAIT/F-WAIT/PRDY	A13	A19	B13	A18	R13	DQ4	T13	DQ5	L15	F-DPD	L16	F-VSS		
M1	R-VCC	M2	F-VCC2	A14	A21	B14	A20	R14	DQ2	T14	DQ3	M15	F-VCC1	M16	R-VCC		
N1	DQ15	N2	DQ14									N15	DQ0	N16	DQ1		
P1	VSSQ	P2	VCCQ									P15	VCCQ	P16	VSSQ		
R1	N-RES#, NC	R2	D-CKE									R15	F-CKE	R16	N-PRE		
T1	NC	T2	N-MRES#									T15	RTU	T16	NC		

Figure 3.12.2-4
Ball List - 112-Ball BGA, 0.65 mm Pitch, 11 mm X 11 mm Package

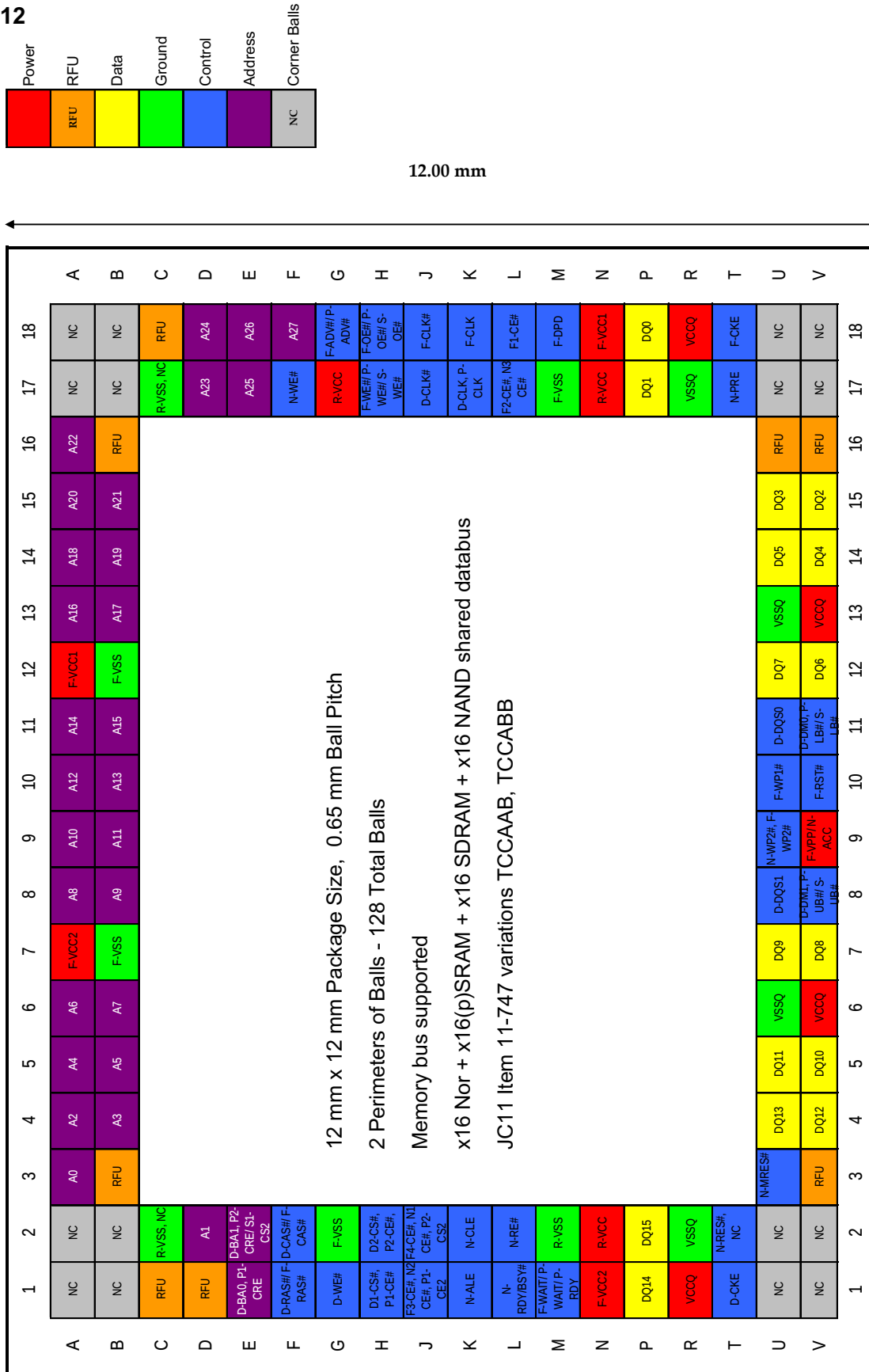
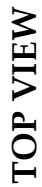


Figure 3.12.2-5
Ball Outline – 128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

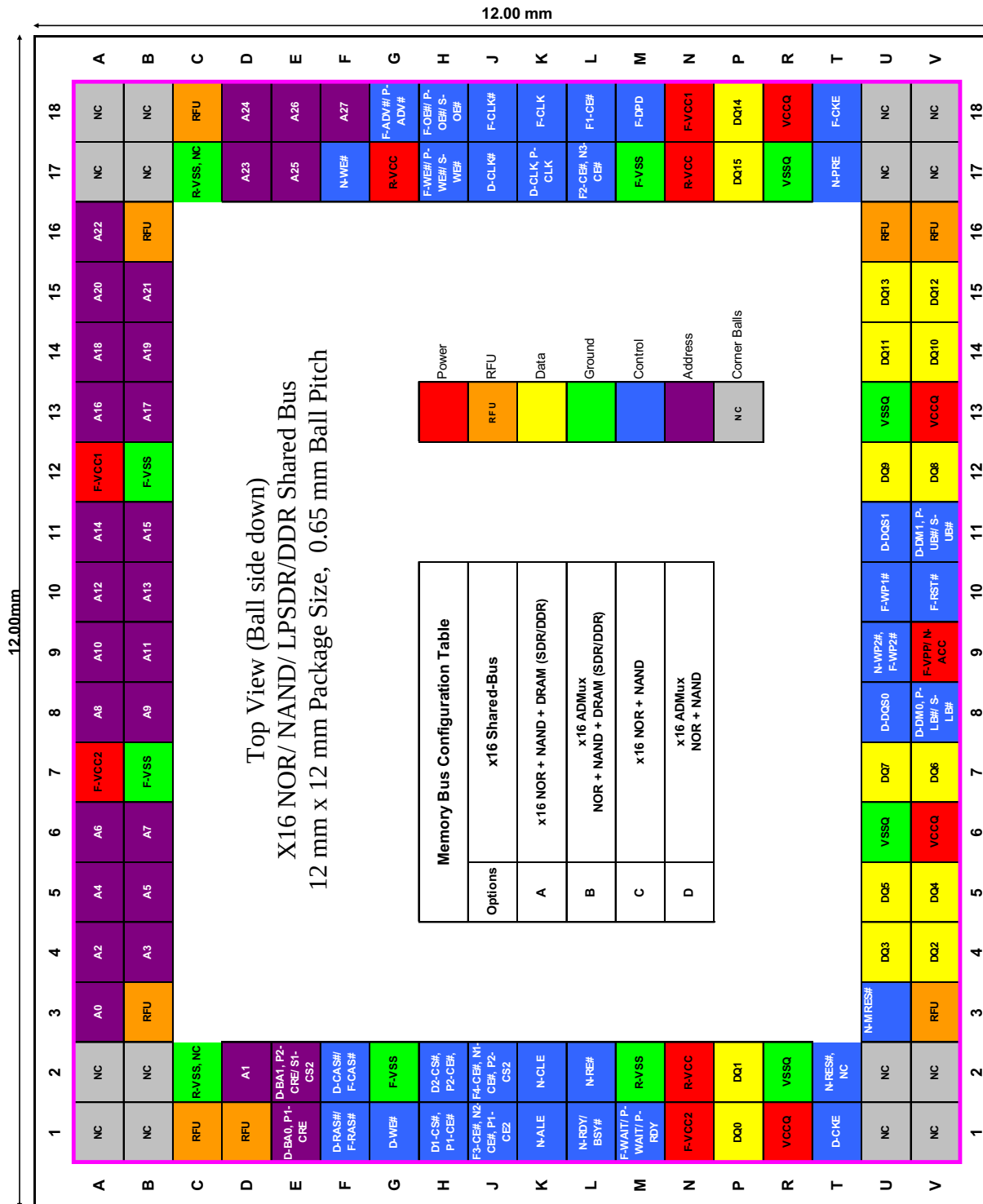


Figure 3.12.2-6
Ball Outline – Flipped DQ Sequence
128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package