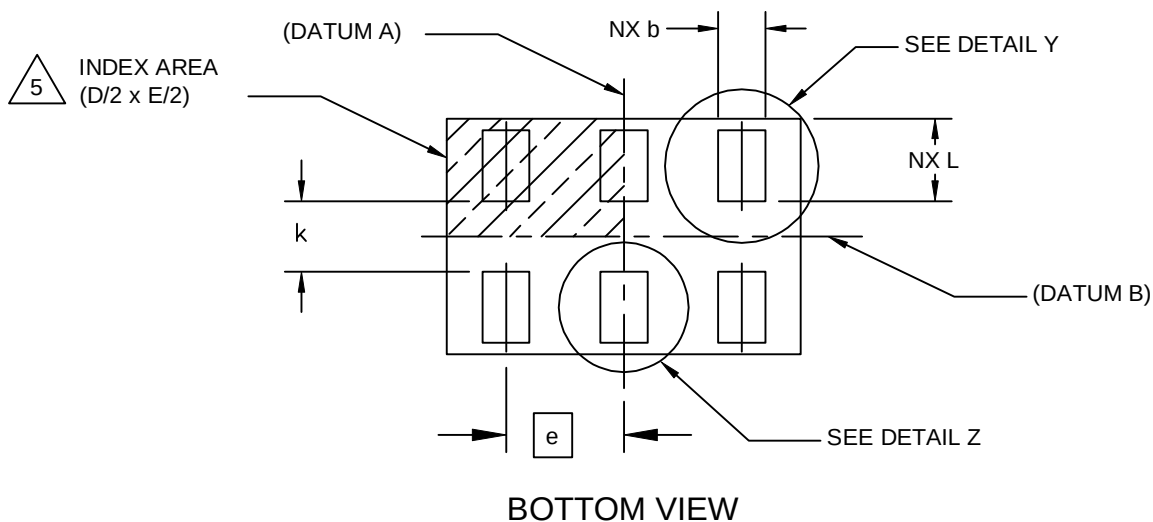
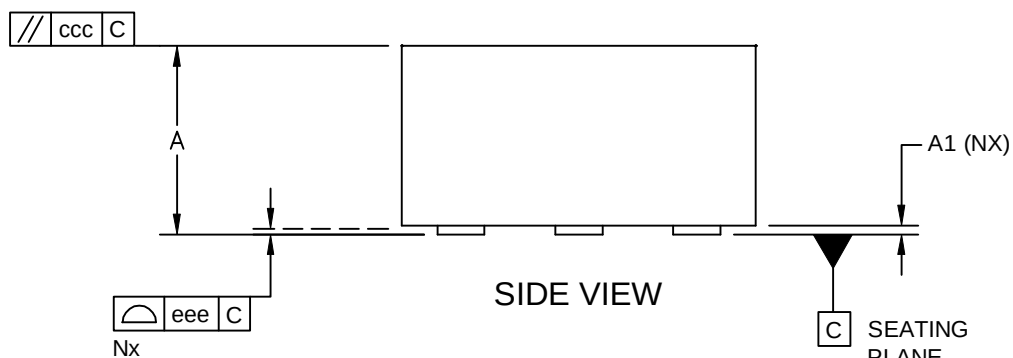
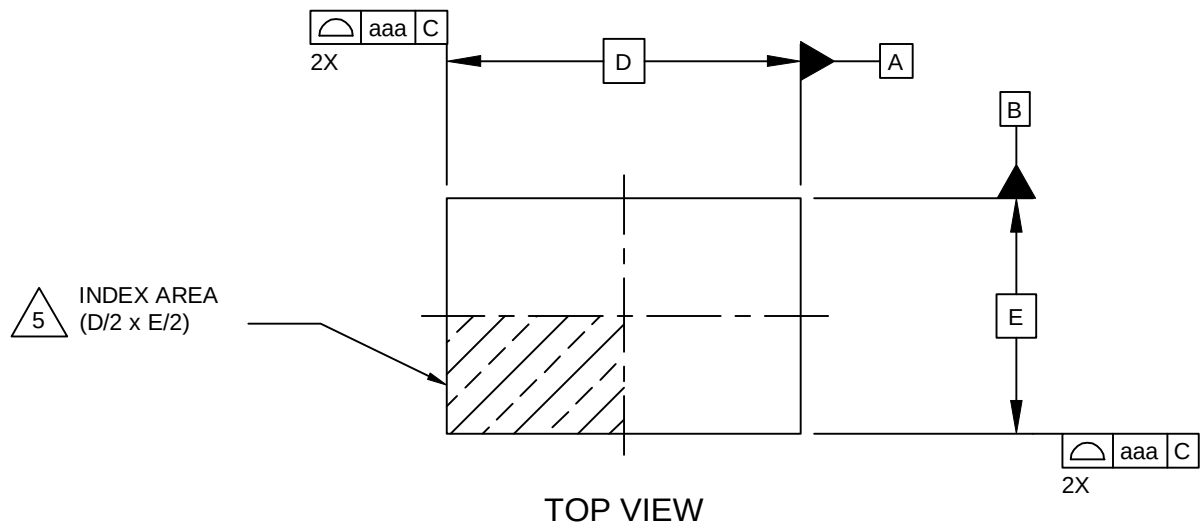




JEDEC
SOLID STATE
PRODUCT OUTLINE

THIS *REGISTERED OUTLINE* HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.

TITLE
PLASTIC VERY VERY THIN, ULTRA THIN AND
EXTREMELY THIN, FINE PITCH DUAL SMALL
OUTLINE, NON-LEADED PACKAGE FAMILY

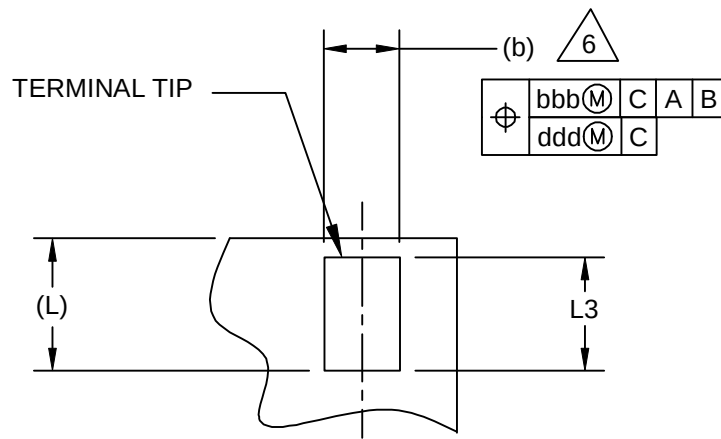
PACKAGE DESIGNATOR
(W,U,X)F-PSON

ISSUE
D

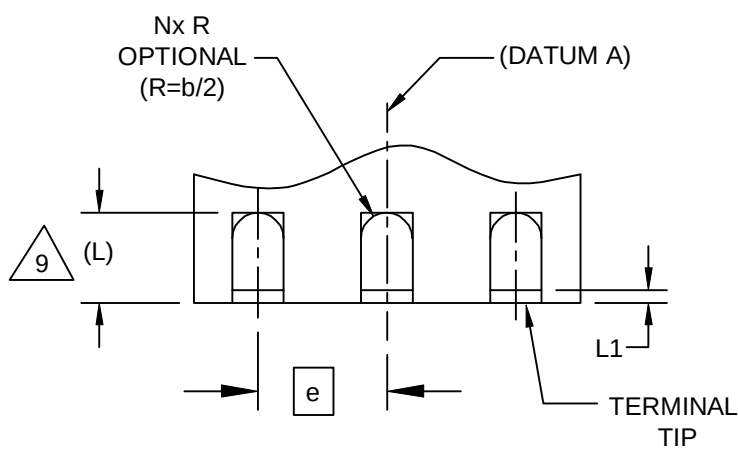
DATE
MAR
2010

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1 OF 9

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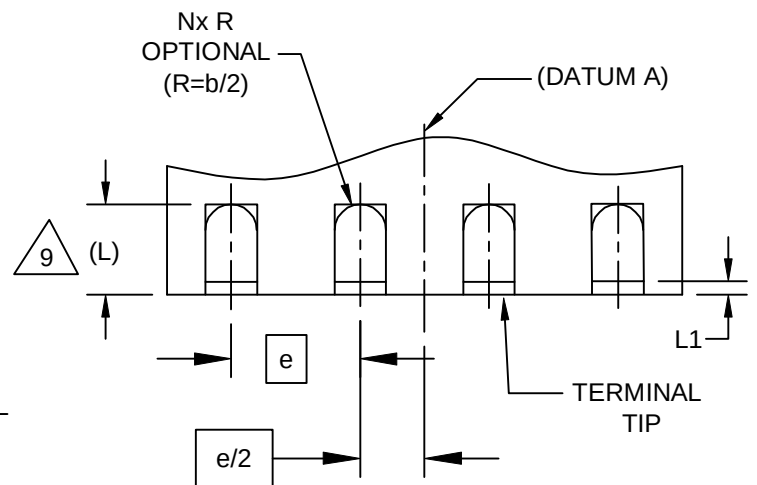


DETAIL Y



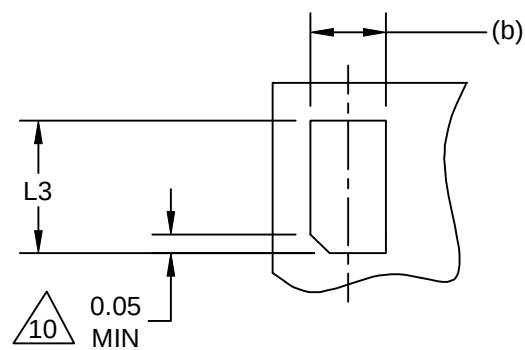
ODD TERMINALS
PER SIDE

DETAIL Z



EVEN TERMINALS
PER SIDE

ELONGATION AND CHAMFER



PIN 1 ID BOTTOM

JEDEC SOLID
STATE PRODUCT
OUTLINE

TITLE

PLASTIC VERY VERY THIN, ULTRA THIN AND
EXTREMELY THIN, FINE PITCH DUAL SMALL
OUTLINE, NON-LEADED PACKAGE FAMILY

ISSUE

D

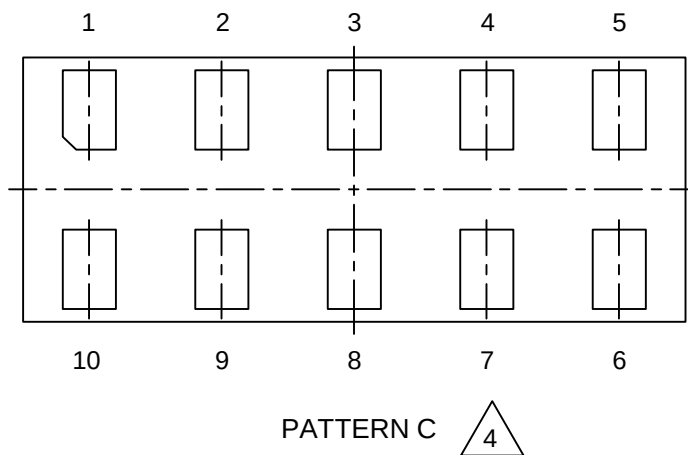
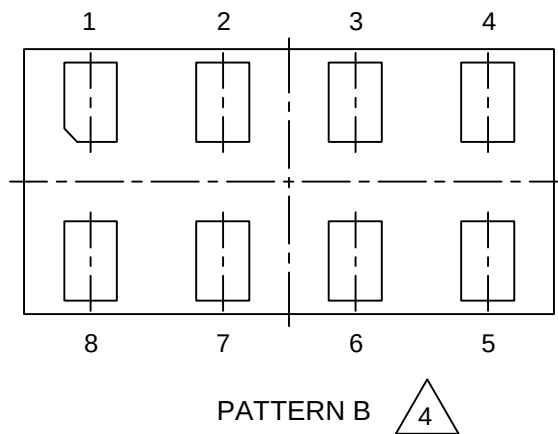
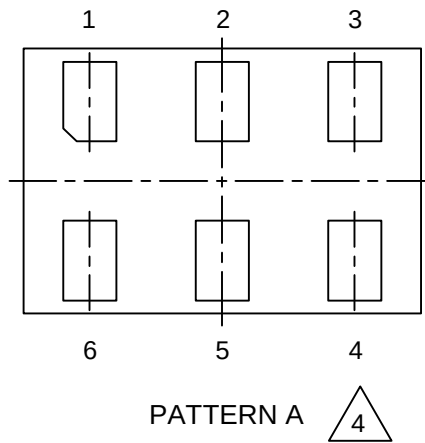
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FIGURE 2
TERMINAL PATTERN
BOTTOM VIEWS



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STATE PRODUCT
OUTLINE

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