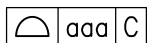


PATENT CLAIMS

21



3 TERMINAL A1 CORNER INDEX AREA



(DATUM A)

B

E

(DATUM B)

A

D

TOP VIEW



DETAIL A

DETAIL B

(DATUM A)



6 4X ALIGNMENT FEATURE AREA

DETAIL E

(DATUM B)

DETAIL D

0,0

DETAIL C

D1

BOTTOM VIEW

SIDE VIEW

5

VARIATION xxxA

JEDEC SOLID STATE
PRODUCT OUTLINE
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THIS **REGISTERED OUTLINE** HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE
AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY;
CHANGES ARE LIKELY TO OCCUR.

TITLE
WIDE I/O MICROPILLAR GRID
ARRAY PACKAGE (MPGA)

PACKAGE DESIGNATOR
(X2,X3,X4)F(R)-SCDS

NUMBER
MO-305

ISSUE

DATE

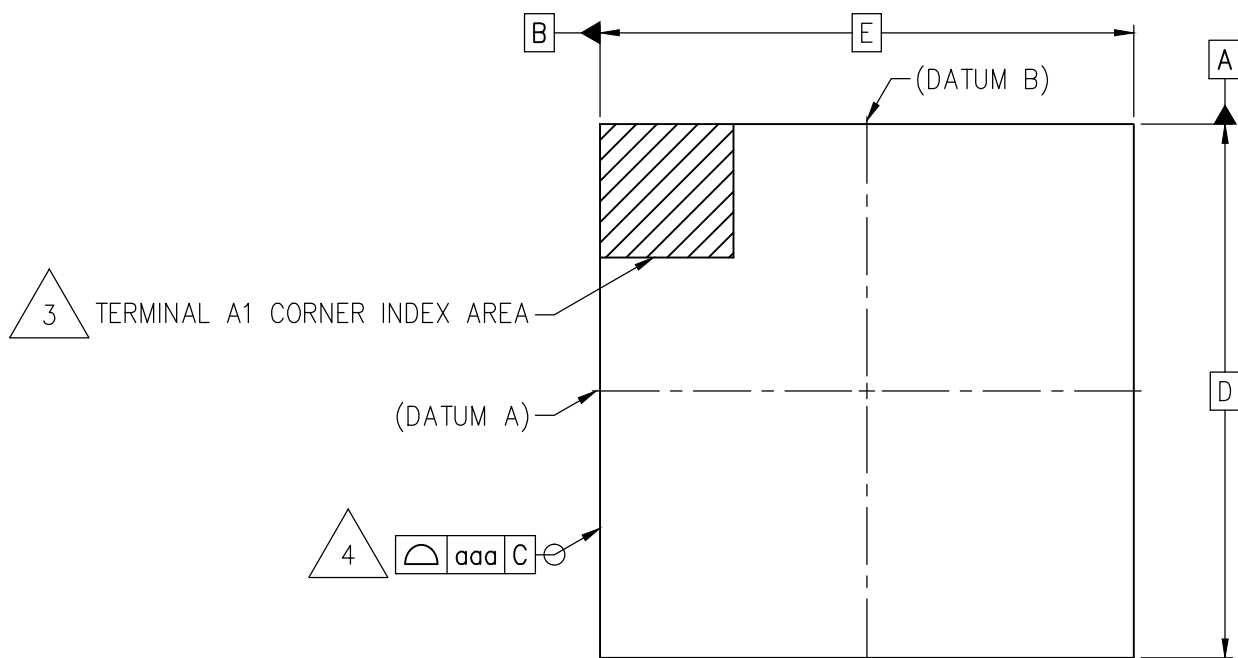
SHEET



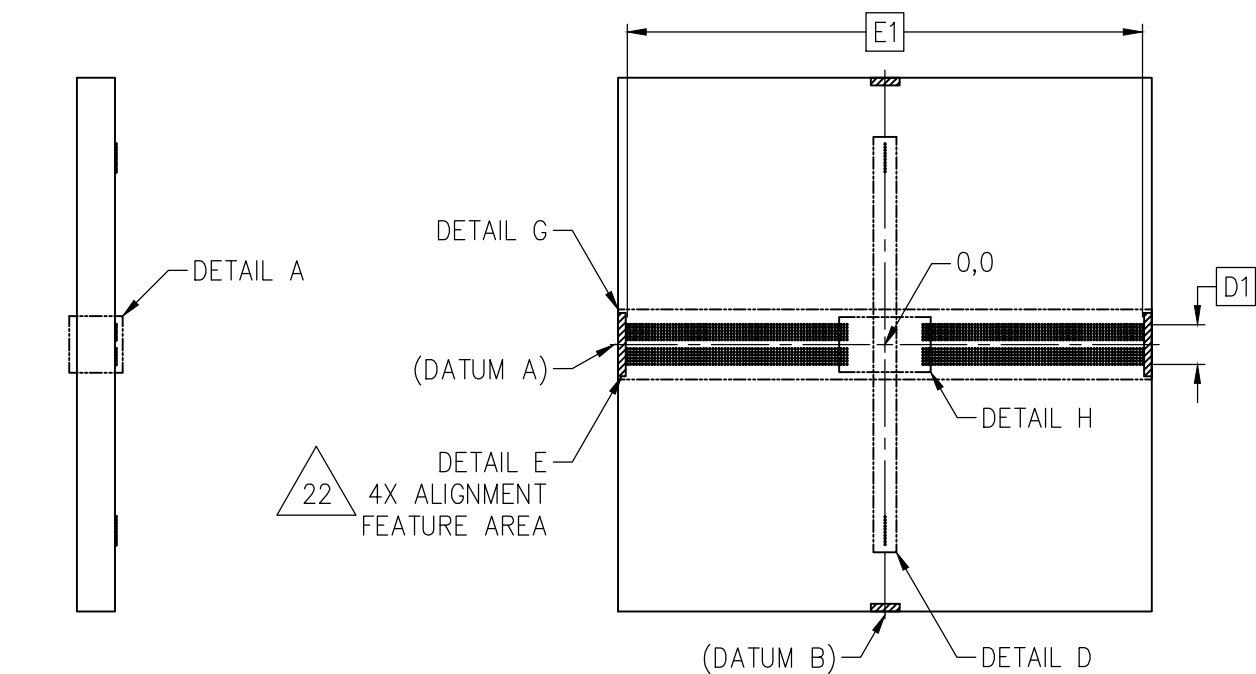
OCT 2013

1 OF 16

Documents
Document Sharing Hub



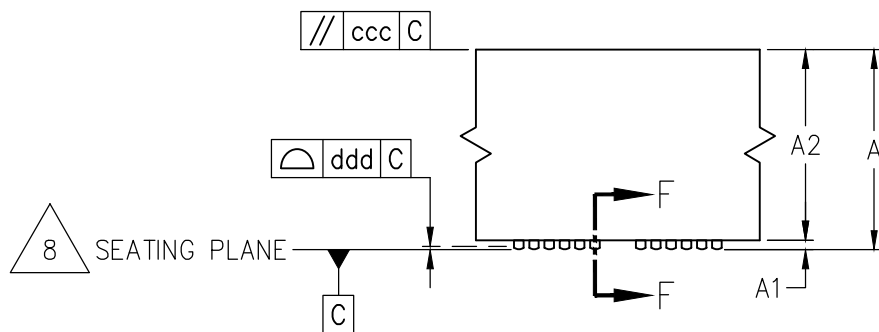
TOP VIEW



SIDE VIEW 5

BOTTOM VIEW

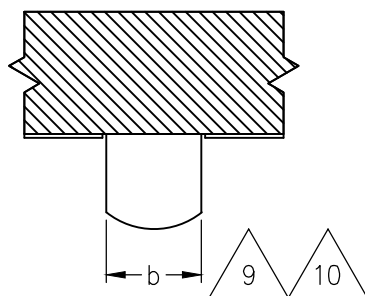
VARIATION xxxB



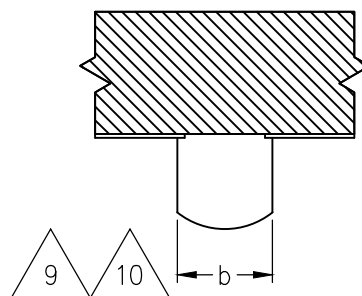
DETAIL A
(ROTATED 90° CW)



TYPE 1

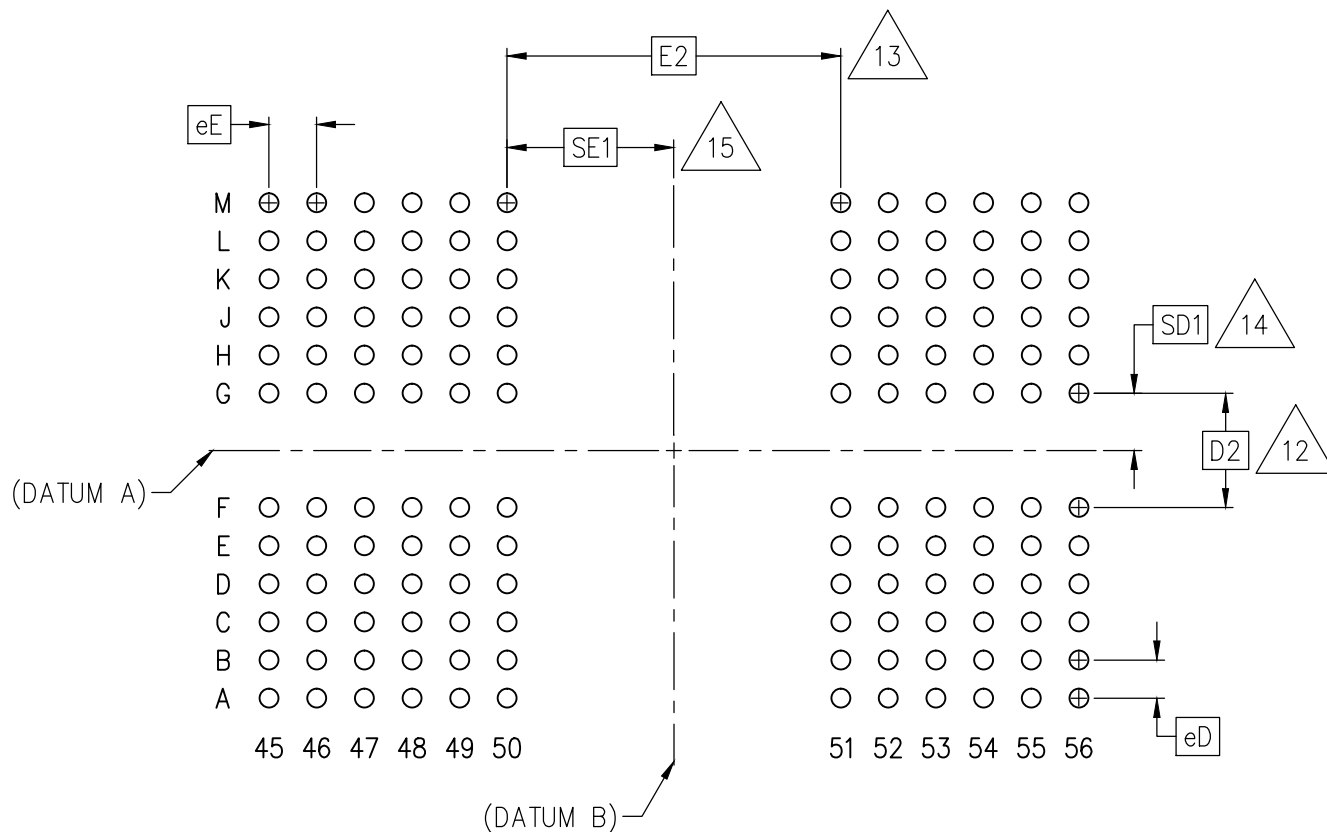


TYPE 2

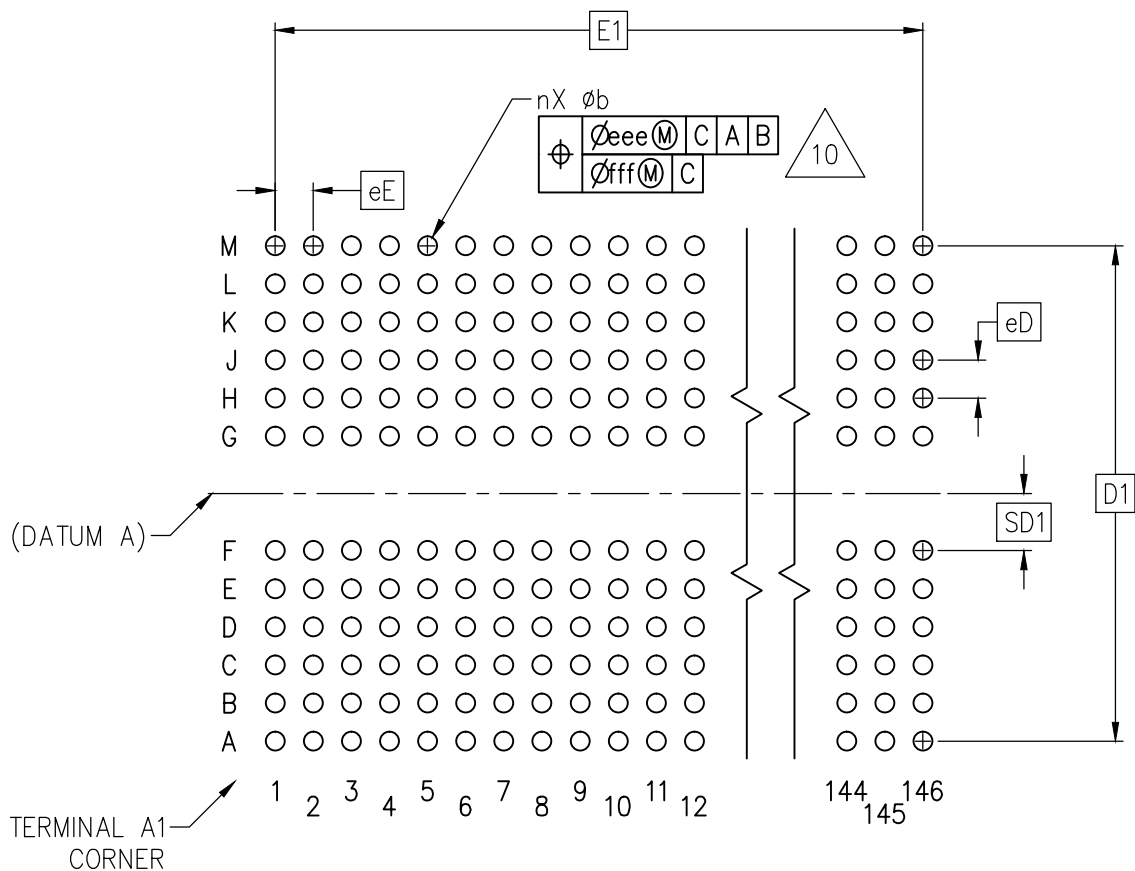


SECTION F-F





DETAIL C 
VARIATION xxxA



DETAIL G 
 VARIATION xxxB