

4.2 One Byte Memory Modules

4.2.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2-1

– 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2-1

– 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a “presence detect” feature which consists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2-1

4.2.2 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4.2-2

4.2.3 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2-3
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

4.2.4 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—
SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2-4

– 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—
SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2-5

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PHYSICAL CONFIGURATION		4 DEVICES LONG				8 OR 9 DEVICES LONG			
		SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION		N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
[1]	1	\$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
[2]	2	VDD	VDD	A8	A8	CE	CE	CE	CE
[3]	3	D0	RE0	VDD	VDD	DQ0	DQ0	DQ0	DQ0
[4]	4	Q0	Q	D0	DQ0	A0	A0	A0	A0
[5]	5	CE	A3	Q0	DQ1	A1	A1	A1	A1
[6]	6	A7	A6	CE	CE	DQ1	DQ1	DQ1	DQ1
[7]	7	A5	D	A7	A7	A2	A2	A2	A2
[8]	8	A4	W	A5	A5	A3	A3	A3	A3
[9]	9	D1	RE1	A4	A4	VSS	VSS	VSS	VSS
[10]	10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
[11]	11	W	A7	Q1	DQ3	A4	A4	A4	A4
[12]	12	A1	A8	W	W	A5	A5	A5	A5
[13]	13	A3	CE	A1	A1	DQ3	DQ3	DQ3	DQ3
[14]	14	A6	RE2	A3	A3	A6	A6	A6	A6
[15]	15	Q2	A2	A6	A6	A7	A7	A7	A7
[16]	16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
[17]	17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
[18]	18	A0	A4	A2	A2	* A9	* A9	A9	* A9
[19]	19	RE	RE3	A0	A0	* A10	NC	A10	RE2
[20]	20	D3	A5	RE1	RE	DQ5	DQ5	DQ5	DQ5
[21]	21	Q0	VDD	D3	DQ6	W	W	W	W
[22]	22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
[23]	23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
[24]	24			*** RE2	NC	# NC	PD1	A11	PD1
[25]	25					DQ7	DQ7	DQ7	DQ7
[26]	26					Q8	PD2	NC	PD2
[27]	27					RE	RE	RE	RE1
[28]	28					CE8	NC	NC	NC
[29]	29					D8	DQ8	NC	DQ8
[30]	30					VDD	VDD	VDD	VDD

TOP VIEW

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMMODATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

\$ OPTIONAL VSS WHEN A8 NOT NEEDED

OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

PRESENCE DETECT TRUTH TABLE			
SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

FIGURE 4.2-1

22, 24,& 30 PIN DRAM MODULES

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