

**4.20.11 - 200-Pin DDR2 SDRAM Unbuffered SO-DIMM Design
Specification**

**PC2-6400/PC2-5300/PC2-4200/PC2-3200
DDR2 Unbuffered SO-DIMM
Reference Design Specification
Revision 2.5
July, 2008**

Contents

Product Description	4
Product Family Attributes	4
Raw Card Summary	5
Environmental Requirements	6
Absolute Maximum Ratings	6
Architecture.....	6
Pin Description	6
Input/Output Functional Description	7
DDR2 SDRAM SO-DIMM Pinout	8
Block Diagram: Raw Card Version A, G(Populated as 2 ranks of x16 SDRAMs).....	9
Block Diagram: Raw Card Version B(Populated as 1 rank of x8 SDRAMs)	10
Block Diagram: Raw Card Version C, H(Populated as 1 rank of x16 SDRAMs)	11
Block Diagram: Raw Card Version D(Populated as 2 ranks of x8 stacked SDRAMs).....	12
Block Diagram: Raw Card Version E(Populated as 2 ranks of x8 SDRAMs)	13
Block Diagram: Raw Card Version F(Populated as 2 ranks of x8 SDRAMs).....	14
Component Details	15
SO-DIMM Common landing pattern for x8 and x16	15
x8 Ballout for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DDR2 SDRAMs (Top View).....	17
x16 Ballout for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DDR2 SDRAMs (Top View).....	17
DDR2 SDRAM FBGA Component Specifications	18
x16 Ballout for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DDR2 SDRAMs (Top View).....	18
Unbuffered SO-DIMM Details.....	19
DDR2 SDRAM Module Configurations (Reference Designs)	19
Input Loading Matrix.....	20
DDR2 SO-DIMM Gerber File Releases	21
Example Raw Card Component Placement.....	22
SO-DIMM Wiring Details.....	24
Signal Groups	24
General Net Structure Routing Guidelines	24
Explanation of Net Structure Diagrams	24
Differential Clock Net Structures	25
Clock Net Wiring CK[1:0], CK[1:0] (Raw Cards A, G and B).....	25
Clock Net Wiring CK[1:0], CK[1:0] (Raw Card C, H).....	26
Clock Net Wiring CK[1:0], CK[1:0] (Raw Card D)	27
Clock Net Wiring CK[1:0], CK[1:0] (Raw Card E).....	28
Clock Net Wiring CK[1:0], CK[1:0] (Raw Card F)	29
Data Net Structures.....	30
Data Net Structures DQ[63:0], DM[7:0], DQS[7:0], DQS[7:0] (Raw cards A, E, F, G).....	30
Data Net Structures DQ[63:0], DM[7:0], DQS[7:0], DQS[7:0] (Raw cards B, C, D, H)	31

Control Net Structures S[1:0], CKE[1:0], ODT[1:0] (Raw cards A, G and C, H)	32
Control Net Structures S[0], CKE[0], ODT[0] (Raw card B)	33
Control Net Structures S[1:0], CKE[1:0], ODT[1:0] (Raw card D)	34
Control Net Structures S[1:0], CKE[1:0], ODT[1:0] (Raw card E)	35
Control Net Structures S[1:0], CKE[1:0], ODT[1:0] (Raw card F)	36
Address/Command Net Structures Ax, BAx, RAS, CAS, WE (Raw cards A, G and B)	37
Address/Command Net Structures Ax, BAx, RAS, CAS, WE (Raw card C, H)	38
Address/Command Net Structures Ax, BAx, RAS, CAS, WE (Raw card D)	39
Address/Command Net Structures Ax, BAx, RAS, CAS, WE (Raw card E)	40
Address/Command Net Structures Ax, BAx, RAS, CAS, WE (Raw card F)	41
Cross Section Recommendations	42
Test Points	44
Serial Presence Detect Definition	55
Serial Presence Detect Data Example	55
Product Label	58
SO-DIMM Mechanical Specifications	60

1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC2-6400 memory module, a 200-pin, 400MHz clock (800 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate 2 (DDR2) DRAM Small Outline Dual In-Line Memory Module (DDR2 SDRAM SO-DIMMs). It also defines slower versions, the PC2-5300, PC2-4200 and PC2-3200 with a 333MHz 267MHz and 200MHz clock (667 MT/s, 533 MT/s and 400 MT/s data rate) DDR2 SDRAMs. These DDR2 SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 333MHz clock rate support. Other designs are acceptable, and all Unbuffered DDR2 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
SO-DIMM Organization	x 64	
Dimensions (nominal)	30.0 mm high, 67.60 mm wide / MO-224 variation CB 25.4 mm high, 67.60 mm wide / MO-224 variation AB	
SO-DIMM Types Supported	Unbuffered	
Pin Count	200	
SDRAMs Supported	256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb	
Capacity	128 MB, 256 MB, 512 MB, 1 GB, 2GB, 4 GB, 8 GB	
Serial Presence Detect	Consistent with JEDEC latest Rev.	
Voltage Options, Nominal	1.8 V V_{DD} 1.8 V V_{DDQ} 1.8 V to 3.3 V V_{DDSPD}	1, 2
Interface	SSTL_18	
Note 1: V_{DDSPD} is not tied to V_{DD} or V_{DDQ} on the DDR2 SO-DIMM. Note 2: SO-DIMMs that include an optional temperature sensor may require a restricted VDDSPD operating voltage range for proper operation of the temperature sensor. Refer to the thermal sensor specification for details regarding the supported voltage range. All other functions of the SO-DIMM SPD are supported across the full VDDSPD range.		

Raw Card Summary

Raw Card	Number of DDR2 SDRAMs	SDRAM Organization	Number of Ranks	Comments
A, G	8	x16	2	G is low profile version(maximum DRAM size, W x L) 11.0 mm x 13.0mm
B	8	x8	1	
C, H	4	x16	1	H is low profile version(maximum DRAM size, W x L) 11.0 mm x 13.0mm
D	16	x8	2	Uses stacked memory
E	16	x8	2	Planar (maximum DRAM size, W x L) 12.0 mm x 11.5 mm
F	16	x8	2	Planar (maximum DRAM size, W x L) 11.0 mm x 13.65 mm

2. Environmental Requirements

PC2-6400 DDR2 SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.				

3. Architecture

Pin Description

CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$ [1:0]	Clock inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$ [7:0]	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1			
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SO-DIMM)	1
$\overline{S}$ [1:0]	Chip Selects	2			
A[9:0],A[11:15]	Address Inputs	15	V _{DD}	Core and I/O Power	12
A10/AP	Address Input/Autoprecharge	1	V _{SS}	Ground	57
BA[2:0]	SDRAM Bank Address	3	V _{REF}	Input/Output Reference	1
ODT[1:0]	On-die termination control	2	V _{DD} SPD	SPD and TS Power	1
SCL	Serial Presence Detect (SPD) and Thermal sensor Clock Input	1	$\overline{Event}$ Pin	Reserved for optional hardware temperature sensing	1
SDA	SPD and TS Data Input/Output	1	NC	Reserved for future use	3
SA[1:0]	SPD and TS address	2		Total:	200
Note: 4 rank SO-DIMM specific signals($\overline{RESET}$, $\overline{S2}$, $\overline{S3}$) are not included in this table.					

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/ $\overline{\text{CK}}0$, CK1/ $\overline{\text{CK}}1$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S}}[1:0]$	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S}}0$; Rank 1 is selected by $\overline{\text{S}}1$.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ and $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR2 SDRAM internal bank of four or eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[15:11]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
$\overline{\text{DQS}}[7:0]$, DQS[7:0]	In/Out	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V _{DD} , V _{DD} SPD, V _{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, Thermal sensor, and ground for the module.
V _{REF}	Supply	—	Reference voltage for SSTL18 inputs.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM or Thermal sensor. A resistor must be connected from the SDA bus line to V _{DD} SPD on the system planar to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor.
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).
$\overline{\text{Event}}$	Wire-OR Out	Active Low	The optional EVENT pin is reserved for use to flag critical module temperatures and is used in conjunction with a SPD temperature sensing option.

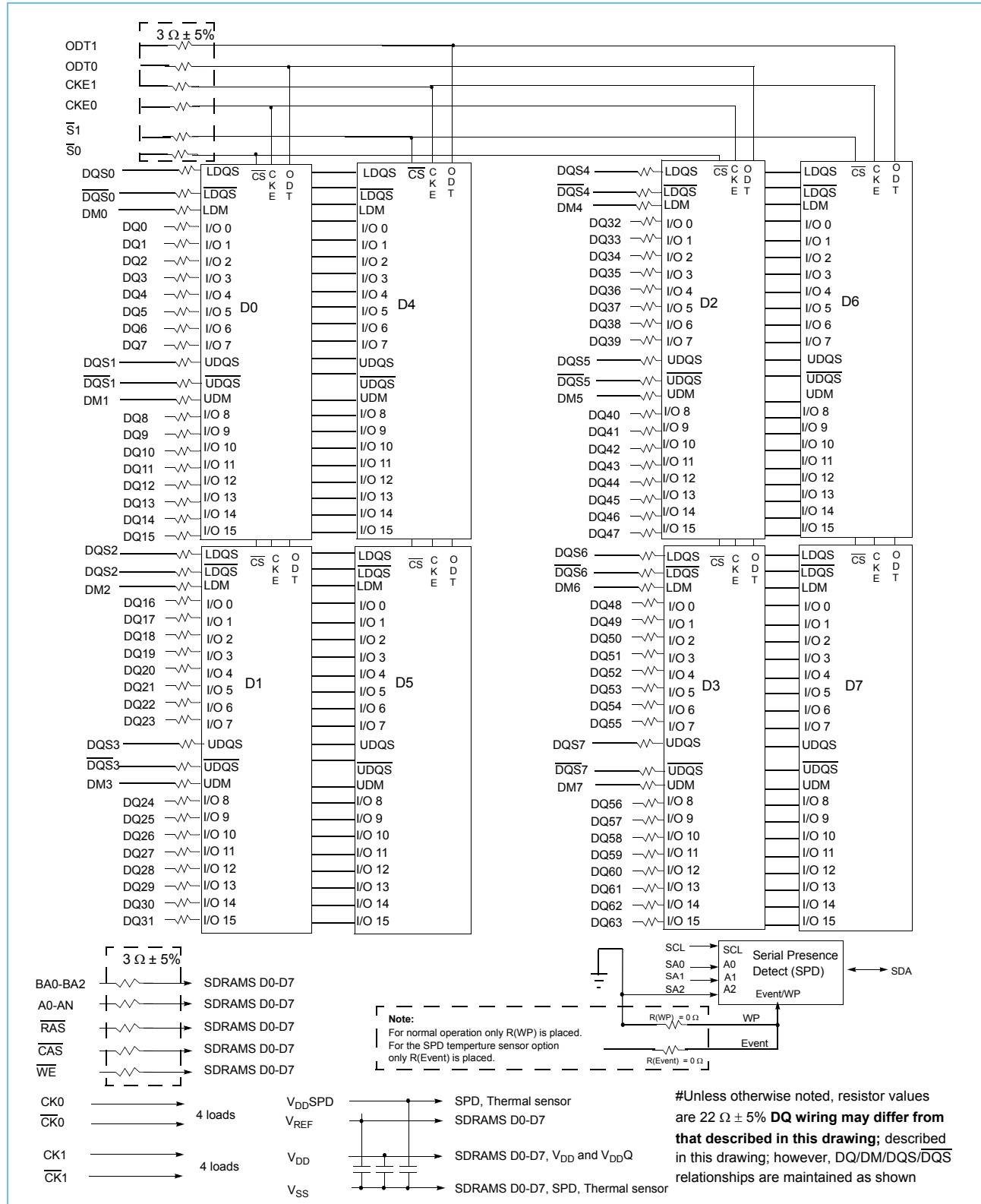
DDR2 SDRAM SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REF}	2	V _{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V _{SS}	4	DQ4	53	V _{SS}	54	V _{SS}	103	V _{DD}	104	V _{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V _{SS}	156	V _{SS}
7	DQ1	8	V _{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{\text{RAS}}$	157	DQ48	158	DQ52
9	V _{SS}	10	DM0	59	V _{SS}	60	V _{SS}	109	$\overline{\text{WE}}$	110	$\overline{\text{S0}}$	159	DQ49	160	DQ53
11	$\overline{\text{DQS0}}$	12	V _{SS}	61	DQ24	62	DQ28	111	V _{DD}	112	V _{DD}	161	V _{SS}	162	V _{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{\text{CAS}}$	114	ODT0	163	NC,TEST	164	CK1
15	V _{SS}	16	DQ7	65	V _{SS}	66	V _{SS}	115	NC/ $\overline{\text{S1}}$	116	NC / A13	165	V _{SS}	166	$\overline{\text{CK1}}$
17	DQ2	18	V _{SS}	67	DM3	68	$\overline{\text{DQS3}}$	117	V _{DD}	118	V _{DD}	167	$\overline{\text{DQS6}}$	168	V _{SS}
19	DQ3	20	DQ12	69	NC/ $\overline{\text{RE SET}}$	70	DQS3	119	NC / ODT1	120	NC/ $\overline{\text{S3}}$	169	DQS6	170	DM6
21	V _{SS}	22	DQ13	71	V _{SS}	72	V _{SS}	121	V _{SS}	122	V _{SS}	171	V _{SS}	172	V _{SS}
23	DQ8	24	V _{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V _{SS}	28	V _{SS}	77	V _{SS}	78	V _{SS}	127	V _{SS}	128	V _{SS}	177	V _{SS}	178	V _{SS}
29	$\overline{\text{DQS1}}$	30	CK0	79	CKE0	80	NC / CKE1	129	$\overline{\text{DQS4}}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{\text{CK0}}$	81	V _{DD}	82	V _{DD}	131	DQS4	132	V _{SS}	181	DQ57	182	DQ61
33	V _{SS}	34	V _{SS}	83	NC/ $\overline{\text{S2}}$	84	NC / A15	133	V _{SS}	134	DQ38	183	V _{SS}	184	V _{SS}
35	DQ10	36	DQ14	85	NC/BA2	86	NC / A14	135	DQ34	136	DQ39	185	DM7	186	$\overline{\text{DQS7}}$
37	DQ11	38	DQ15	87	V _{DD}	88	V _{DD}	137	DQ35	138	V _{SS}	187	V _{SS}	188	DQS7
39	V _{SS}	40	V _{SS}	89	A12	90	A11	139	V _{SS}	140	DQ44	189	DQ58	190	V _{SS}
41	V _{SS}	42	V _{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V _{SS}	193	V _{SS}	194	DQ63
45	DQ17	46	DQ21	95	V _{DD}	96	V _{DD}	145	V _{SS}	146	$\overline{\text{DQS5}}$	195	SDA	196	V _{SS}
47	V _{SS}	48	V _{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{\text{DQS2}}$	50	Event	99	A3	100	A2	149	V _{SS}	150	V _{SS}	199	V _{DD} SPD	200	SA1

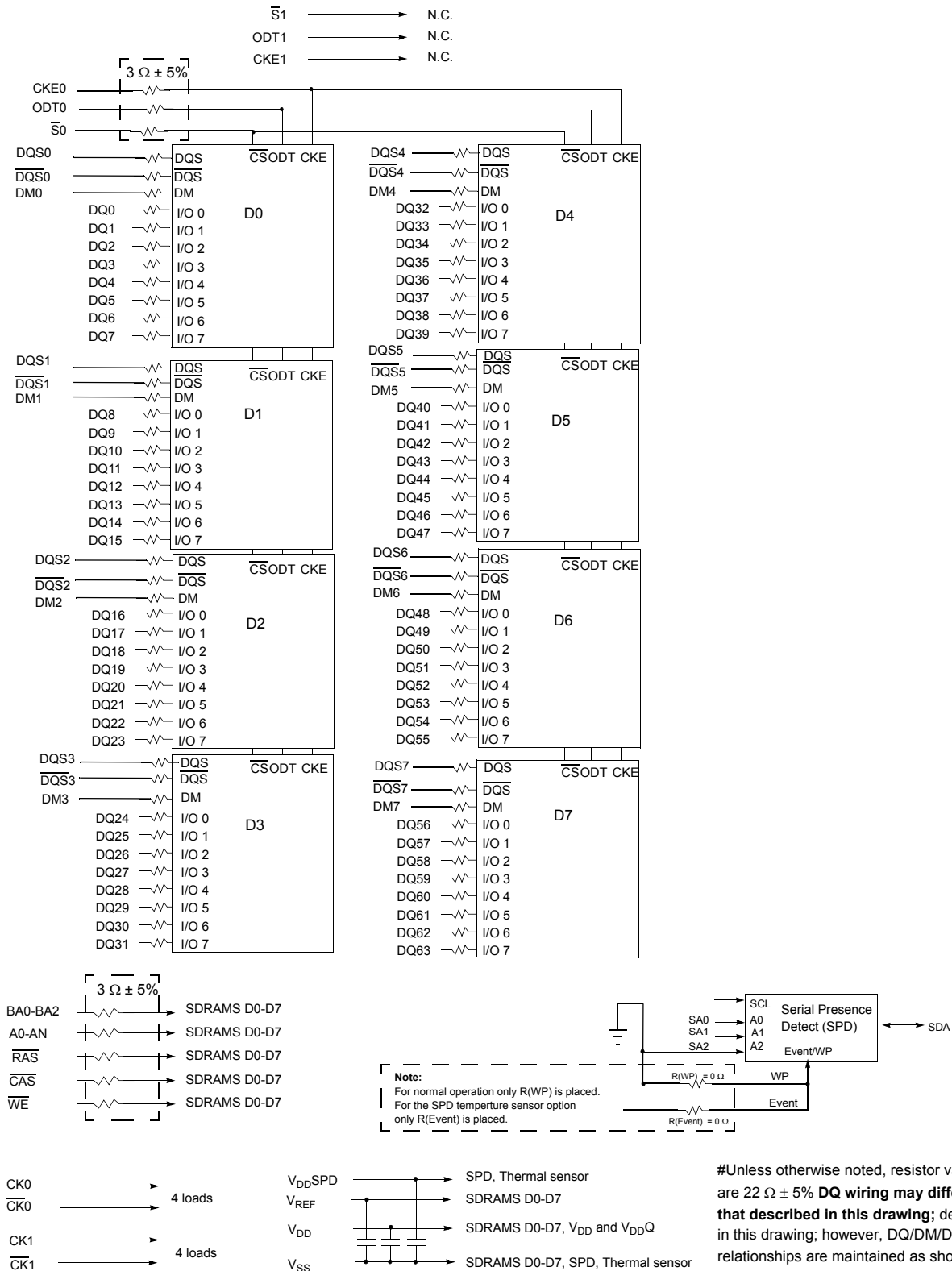
Note:

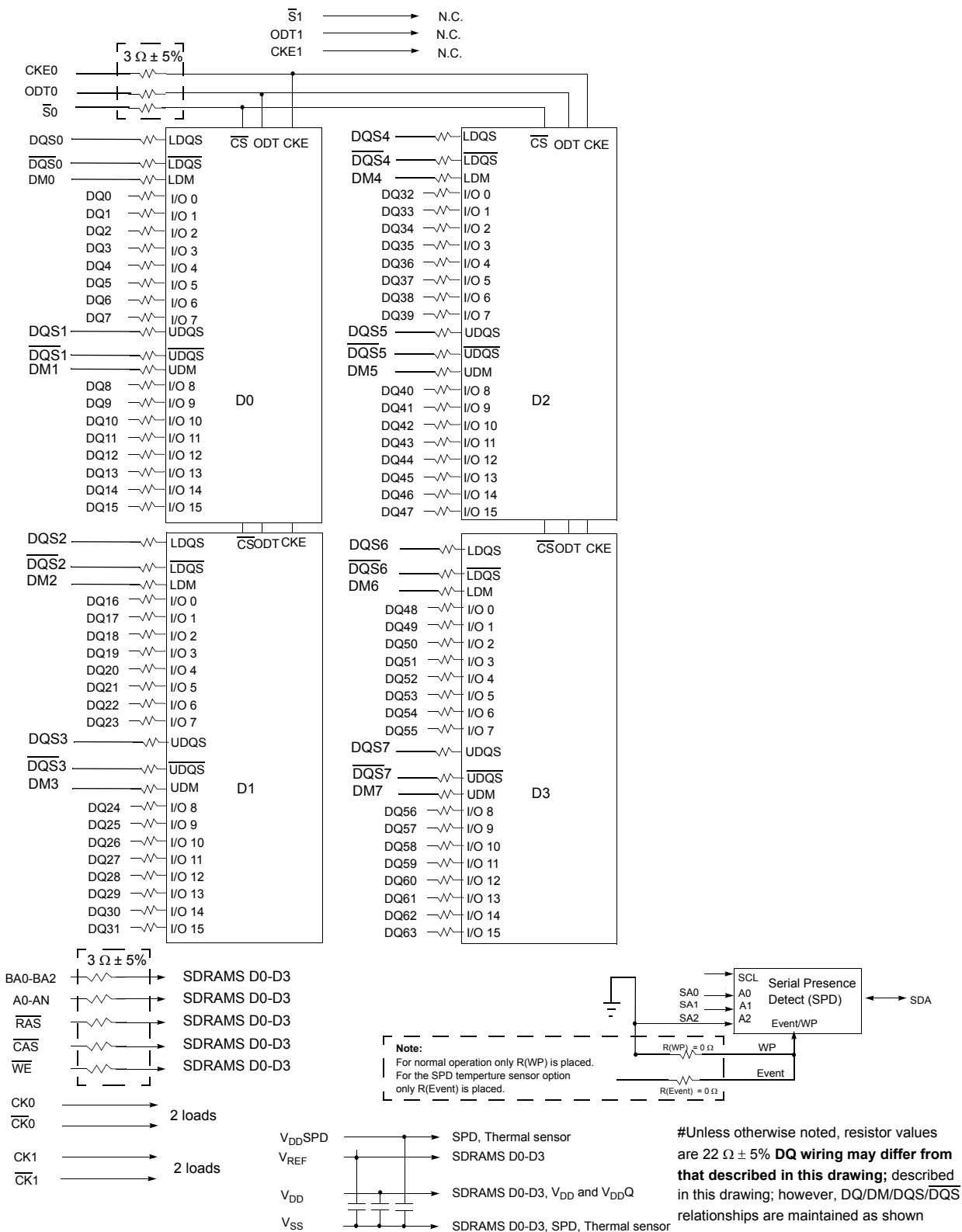
1. NC = No Connect; NC,TEST(pin 163) is for bus analysis tool and is not connected on normal memory modules.
2. Pins 69, 83, 120 used by 4 rank DDR2 SO-DIMMs.

Block Diagram: Raw Card Version A, G (Populated as 2 ranks of x16 SDRAMs)

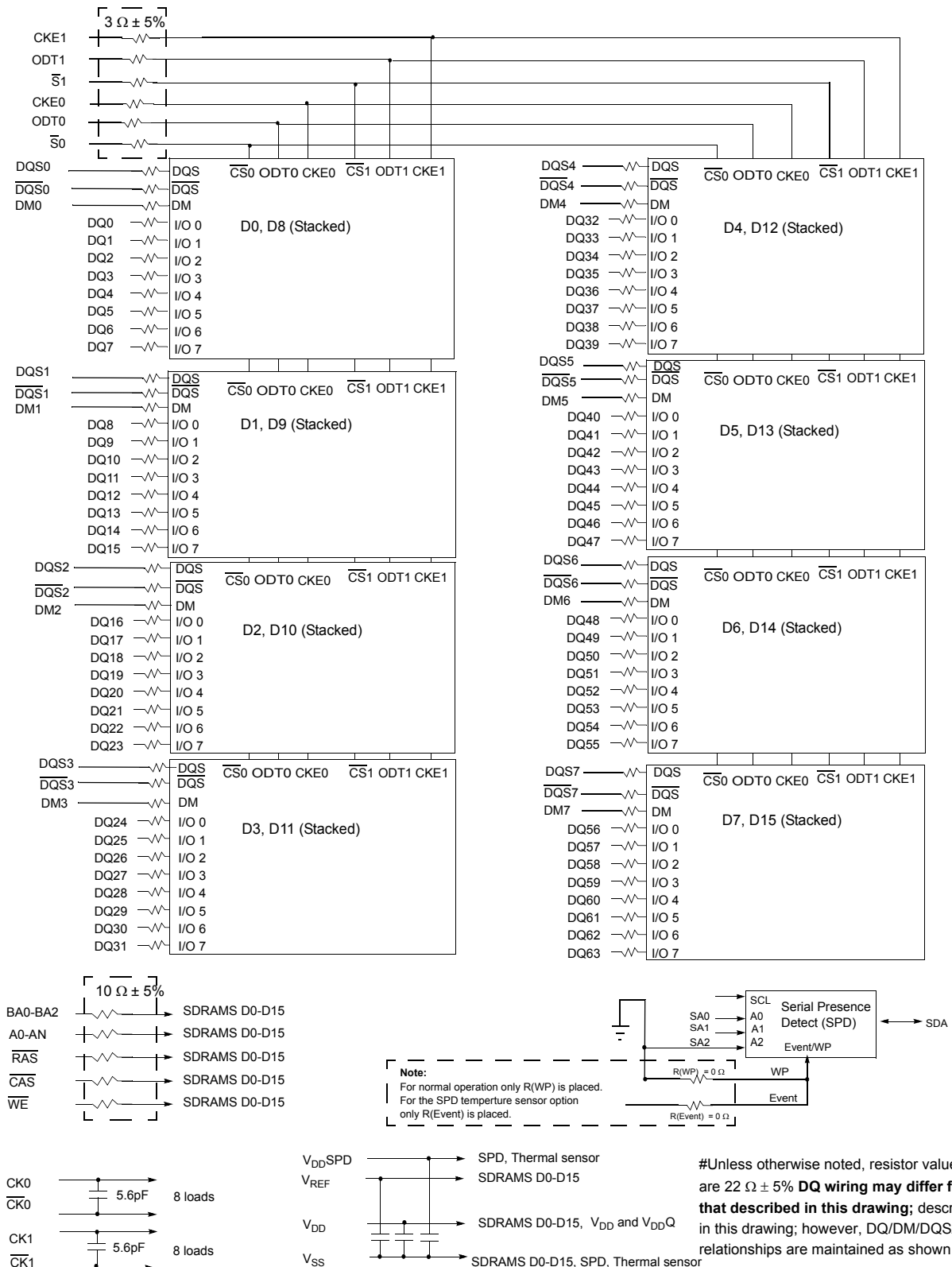


Block Diagram: Raw Card Version B (Populated as 1 rank of x8 SDRAMs)

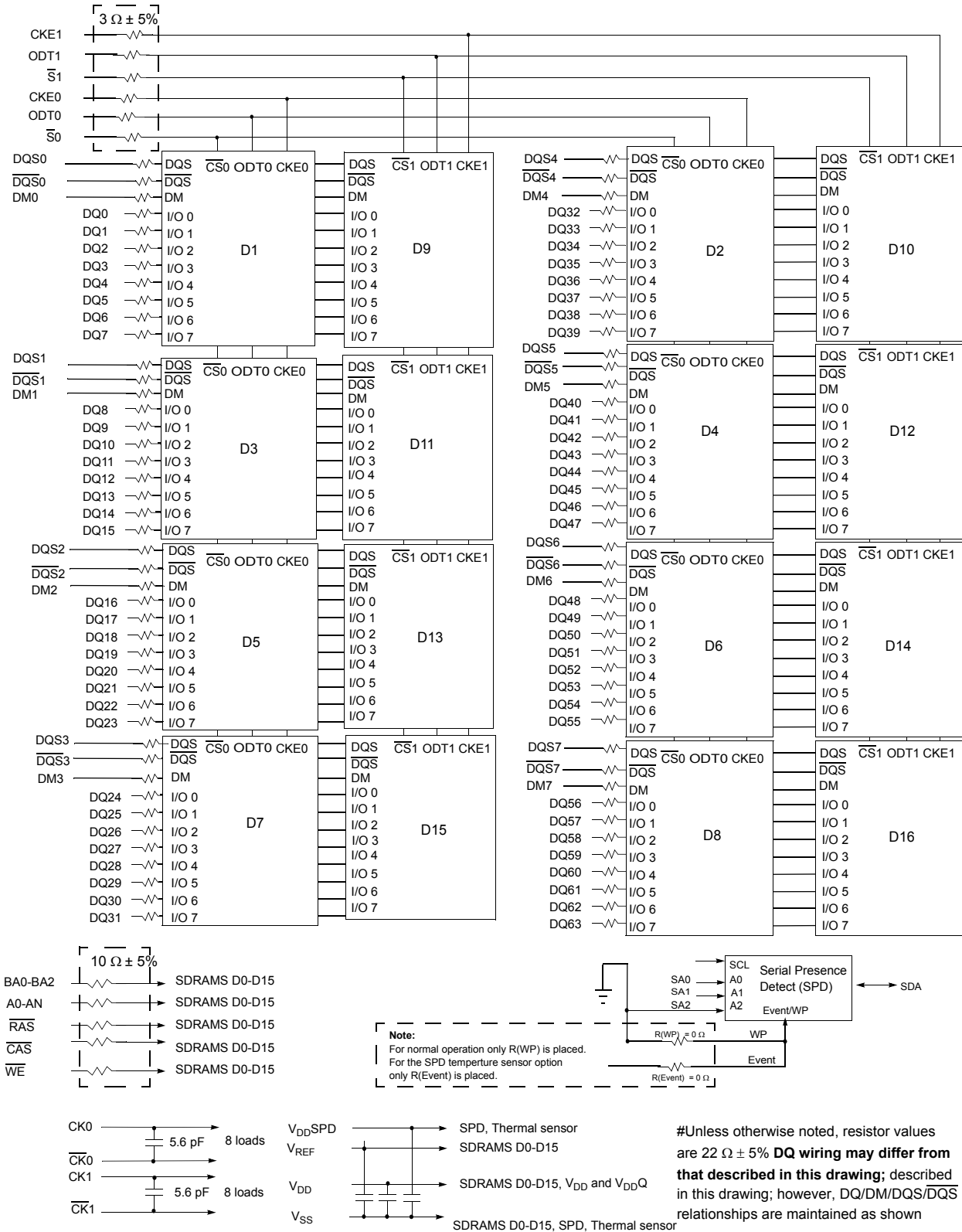




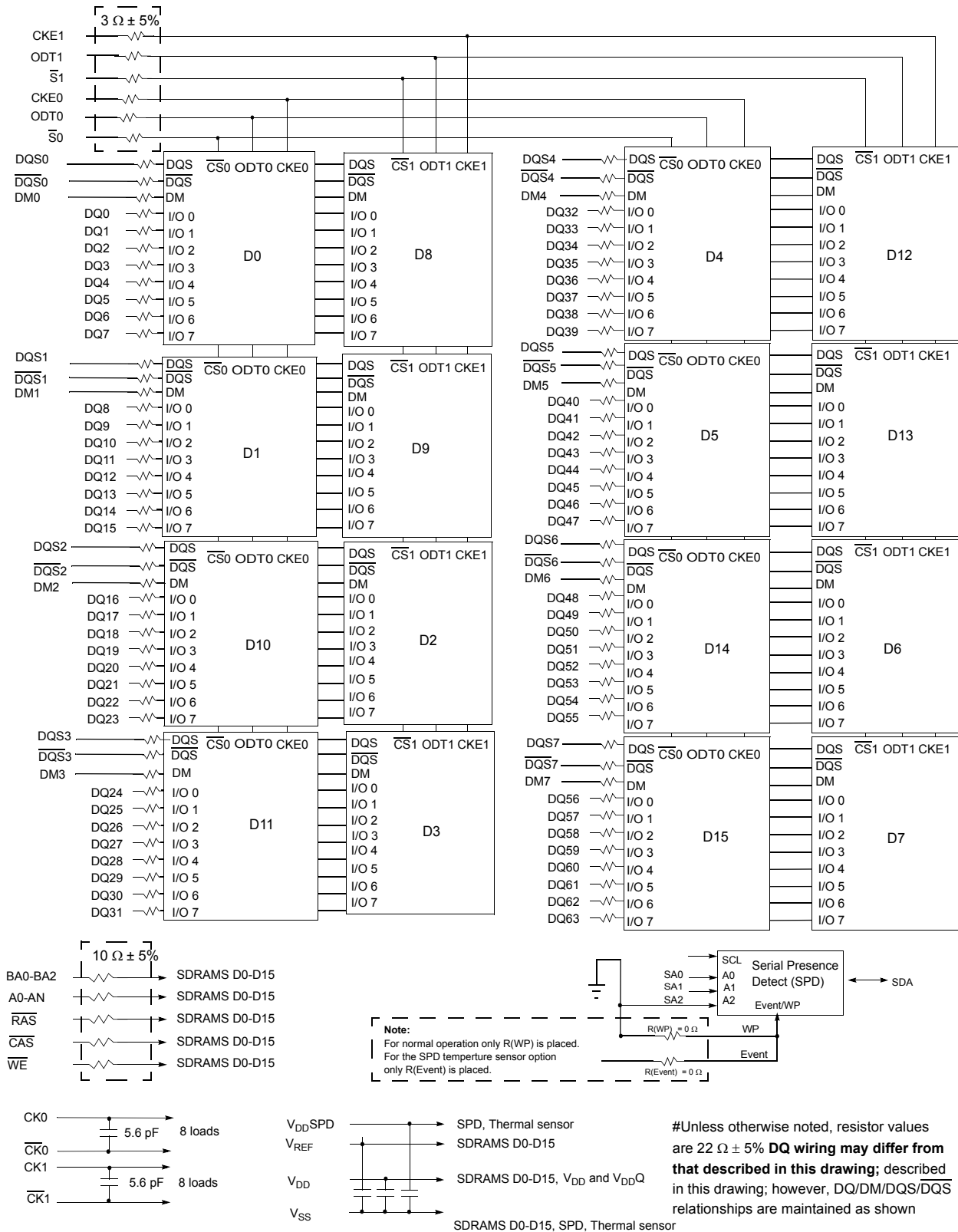
Block Diagram: Raw Card Version D (Populated as 2 rank of x8 SDRAMs)



Block Diagram: Raw Card Version E (populated as 2 rank of x8 SDRAMs)



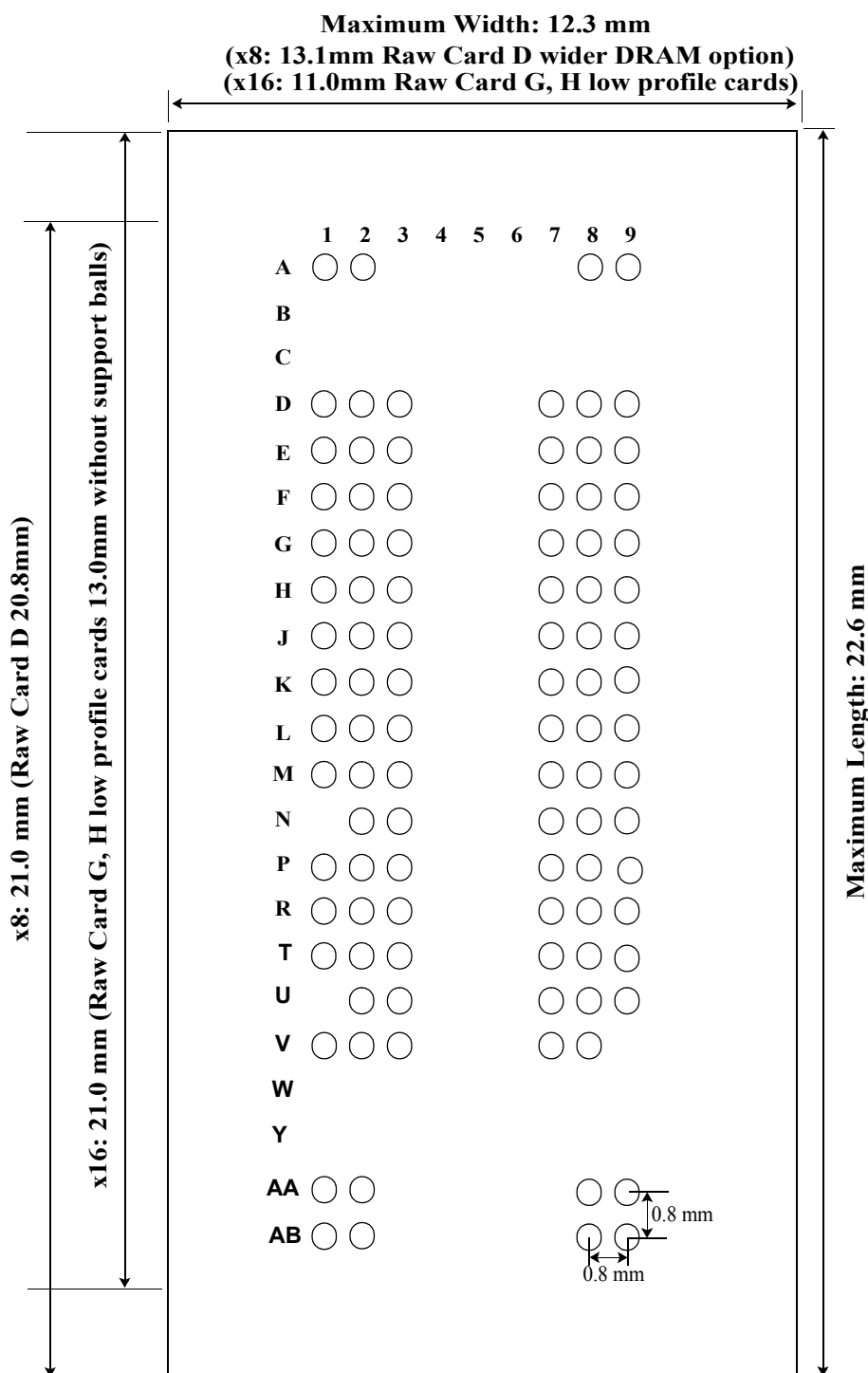
Block Diagram: Raw Card Version F (populated as 2 rank of x8 SDRAMs)

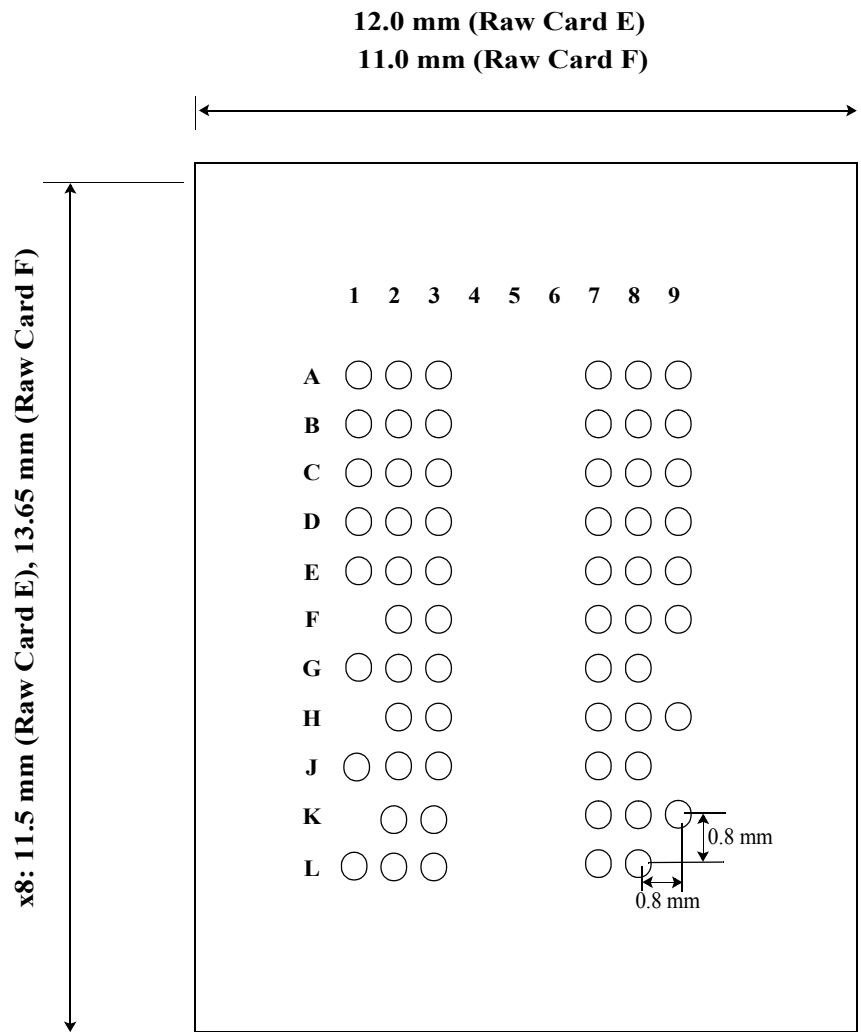


4. Component Details

SO-DIMM Common landing pattern for x8 and x16 -

256 Mb, 512 Mb, 1 Gb, 2 Gb, and 4 Gb DDR2 SDRAM Planar Components (Top View)





x8 Ballout for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DDR2 SDRAMs (Top View)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
VDD	NC	VSS	D	VSSQ	NC	VDDQ
NC	NC	NC	E	NC	NC	NC
NC	NC	NC	F	NC	NC	NC
NC	NC	NC	G	NC	NC	NC
VDD	NU/RDQS	VSS	H	VSSQ	DQS	VDDQ
DQ6	VSSQ	DM/RDQS	J	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	K	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	L	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	M	VSSDL	CK	VDD
	CKE0	WE	N	RAS	CK	ODT
BA2	BA0	BA1	P	CAS	CS0	CS1
CKE1	A10	A1	R	A2	A0	VDD
VSS	A3	A5	T	A6	A4	ODT1
	A7	A9	U	A11	A8	VSS
VDD	A12	A14	V	A15	A13	
			W			
			Y			
NC	NC		AA		NC	NC
NC	NC		AB		NC	NC
1. The above landing pattern also applies for stacked components. For non-stacked components, remove pads at R1 (CKE1), P9(CS1) and T9 (ODT1) locations.						

x16 Ballout for 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb DDR2 SDRAMs (Top View)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
VDD	NC	VSS	D	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	E	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	F	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	UDQ3	G	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	H	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	J	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	K	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	L	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	M	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	N	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	P	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	R	A2	A0	VDD
VSS	A3	A5	T	A6	A4	
	A7	A9	U	A11	A8	VSS
VDD	A12	A14	V	A15	A13	
			W			
			Y			
NC	NC		AA		NC	NC
NC	NC		AB		NC	NC

DDR2 SDRAM FBGA Component Specifications

The DDR2 SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC MO-207, variations DL-Z, DK-Z, DM-Z, DJ-Z. The MO-207 specification allows for a maximum component width of 12.5 mm. The DDR2 SO-DIMM is designed for a variety of maximum component widths and maximum lengths, refer to the applicable raw card for exact component size allowed. Components used on DDR2 SO-DIMMs are also limited to a maximum height (as shown in dimension "A" of MO-207) of 1.35 mm.

Reference SPD Component Specifications

The Serial Presence Detect EEPROMs have their own power pin, V_{DDSPD} , so that they can be programmed or read without powering up the rest of the module. The wide voltage range permits use with 1.8V, 2.5V or 3.3V serial buses.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{DDSPD}	Core Supply Voltage	1.7	3.6	V	1

Note: Note: SO-DIMMs that include an optional temperature sensor may require a restricted V_{DDSPD} operating voltage range for proper operation of the temperature sensor. Refer to the thermal sensor specification for details regarding the supported voltage range. All other functions of the SO-DIMM SPD are supported across the full V_{DDSPD} range.