

**4.20.12 - 214-Pin DDR2 SDRAM Unbuffered MicroDIMM Design
Specification**

**PC2-4200/PC2-3200 DDR2 Unbuffered MicroDIMM
Reference Design Specification**

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1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC2-4200 memory module, a 214-pin, 267 MHz clock (533 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate 2(DDR2) DRAM Micro Dual In-Line Memory Module (DDR2 SDRAM MicroDIMMs). It also defines a slower version, the PC2-3200, using 200MHz clock (400 MT/s data rate) DDR2 SDRAMs. These DDR2 SDRAM MicroDIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered MicroDIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 267 MHz clock rate support. Other designs are acceptable, and all Unbuffered DDR2 MicroDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
MicroDIMM Organization	x 64	
MicroDIMM Dimensions (nominal)	30 mm high, 54.0mm wide	
MicroDIMM Types Supported	Unbuffered	
Pin Count	214	
SDRAMs Supported	256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb	
Capacity	128 MB, 256 MB, 512 MB, 1 GB, 2GB, 4 GB	
Serial Presence Detect	Consistent with JEDEC Rev. 1.0	
Voltage Options, Nominal	1.8 V V_{DD} 1.8 V V_{DDQ} 1.8 V to 3.3 V V_{DDSPD}	1
Interface	SSTL_18	
Note 1: V_{DDSPD} is not tied to V_{DD} or V_{DDQ} on the DDR2 MicroDIMM.		

Raw Card Summary

Raw Card	Number of DDR2 SDRAMs	SDRAM Organization	Number of Ranks
A	8	x16	2
B	4	x16	1

2. Environmental Requirements

PC2-4200 DDR2 SDRAM Unbuffered MicroDIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$ [1:0]	Clock inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$ [7:0]	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1			
$\overline{WE}$	Write Enable	1	NC, TEST	Logic Analyzer specific test pin (No connect on MicroDIMM)	1
$\overline{S}$ [1:0]	Chip Selects	2			
A[9:0], A[15:11]	Address Inputs	15	V _{DD}	Core and I/O Power	15
A10/AP	Address Input/Autoprecharge	1	V _{SS}	Ground	56
BA[2:0]	SDRAM Bank Address	3	V _{REF}	Input/Output Reference	1
ODT[1:0]	On-die termination control	2	V _{DD} SPD	SPD Power	1
SCL	Serial Presence Detect (SPD) Clock Input	1	RFU	Reserved for future use	12
SDA	SPD Data Input/Output	1	NC	No connect	4
SA[1:0]	SPD address	2			
					Total: 214

Input/Output Functional Description

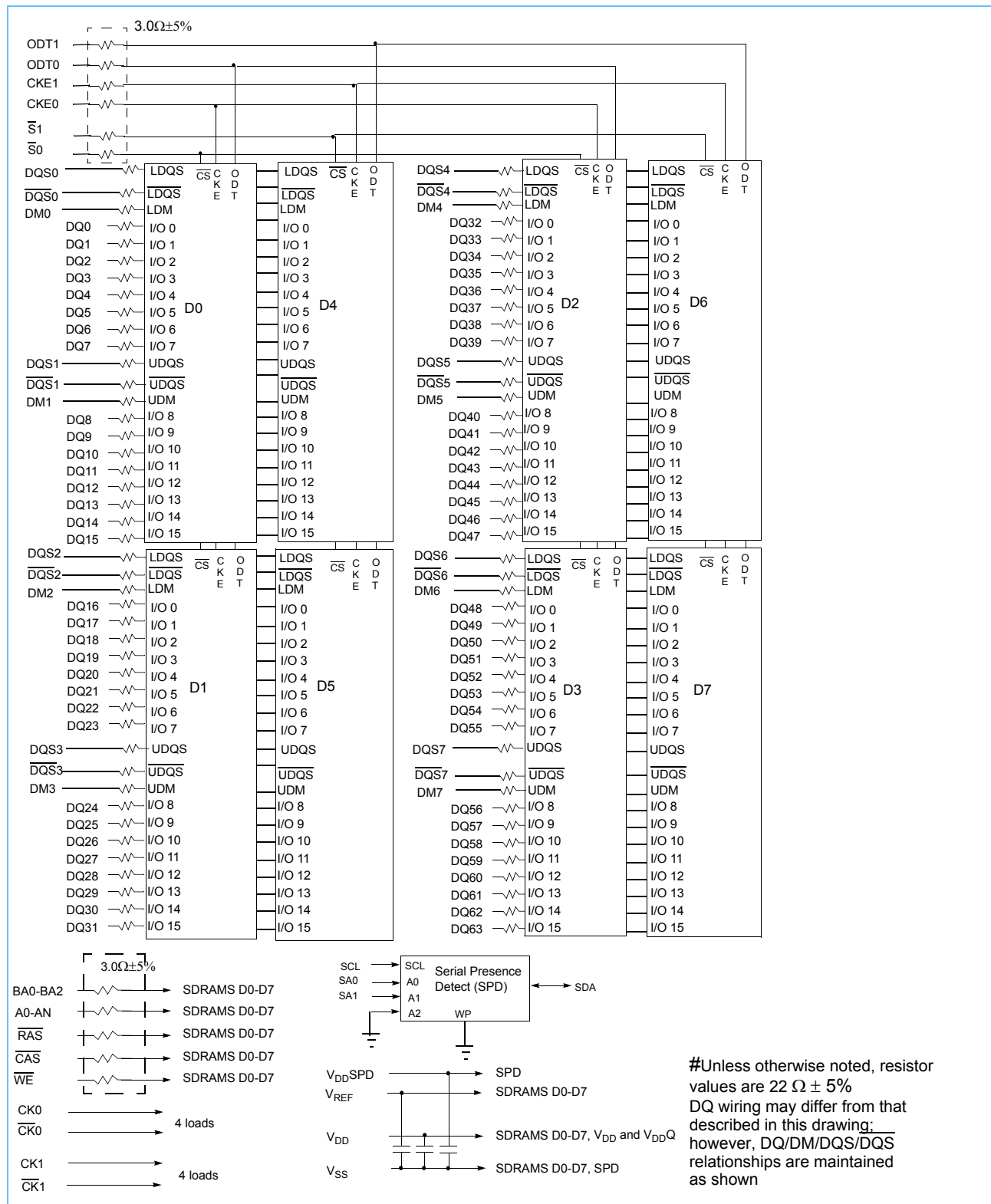
Symbol	Type	Polarity	Function
CK0/ $\overline{\text{CK0}}$, CK1/ $\overline{\text{CK1}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. RFU pins for 2 CK pairs reserved.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode. RFU pins for 2 CKEs reserved.
$\overline{\text{S}}$ [1:0]	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$. Ranks are also called "Physical banks". RFU pins for 2 $\overline{\text{S}}$ s reserved.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR2 SDRAM internal bank of four or eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. RFU pins for 2 ODTs reserved.
A[9:0], A10/AP, A[15:11]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
$\overline{\text{DQS}}$ [7:0], DQS[7:0]	In/Out	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V _{DD} , V _{DD} SPD, V _{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V _{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V _{DD} to act as a pull up.
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect base address. RFU pins for 2nd SPD reserved.
NC, TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (MicroDIMMs).

DDR2 SDRAM MicroDIMM Pinout

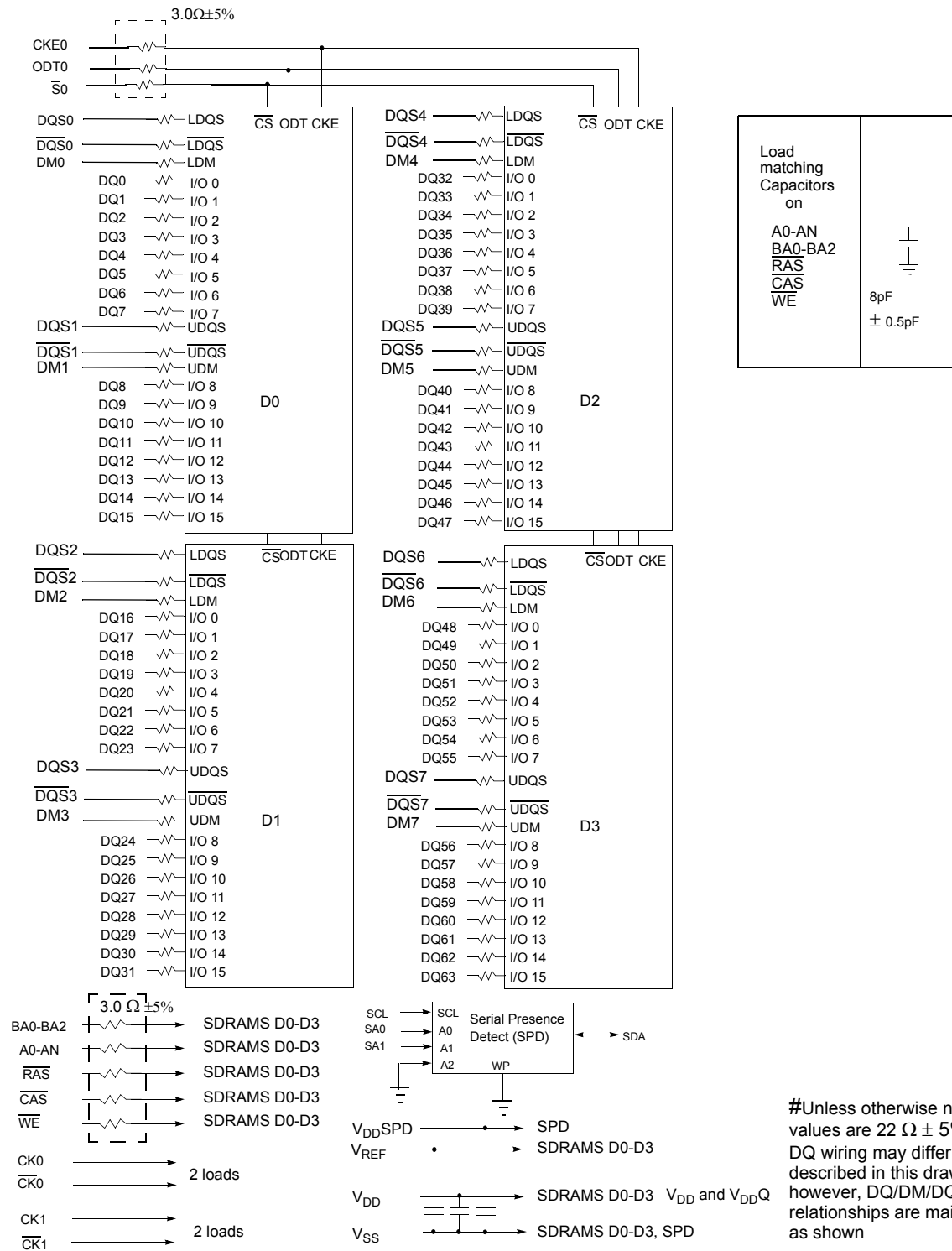
Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side
1	V _{REF}	108	V _{SS}	28	DQS2	135	V _{SS}	55	BA0	162	BA1	82	DQ43	189	DQ47
2	V _{SS}	109	DQ4	29	V _{SS}	136	DQ28	56	$\overline{WE}$	163	$\overline{RAS}$	83	V _{SS}	190	V _{SS}
3	DQ0	110	DQ5	30	DQ18	137	DQ29	57	V _{DD}	164	V _{DD}	84	DQ48	191	DQ52
4	DQ1	111	V _{SS}	31	DQ19	138	V _{SS}	58	RFU($\overline{S2}$)	165	$\overline{S0}$	85	DQ49	192	DQ53
5	V _{SS}	112	DM0	32	V _{SS}	139	$\overline{DQS3}$	59	RFU(OD T2)	166	ODT0	86	V _{SS}	193	V _{SS}
6	$\overline{DQS0}$	113	V _{SS}	33	DQ24	140	DQS3	60	$\overline{CAS}$	167	A13	87	RFU(CK 3)	194	CK1
7	DQS0	114	DQ6	34	DQ25	141	V _{SS}	61	V _{DD}	168	V _{DD}	88	RFU($\overline{CK}$ 3)	195	$\overline{CK1}$
8	V _{SS}	115	DQ7	35	V _{SS}	142	DQ30	62	$\overline{S1}$	169	RFU($\overline{S3}$)	89	V _{SS}	196	V _{SS}
9	DQ2	116	V _{SS}	36	DM3	143	DQ31	63	ODT1	170	RFU(OD T3)	90	DM6	197	$\overline{DQS6}$
10	DQ3	117	DQ12	37	V _{SS}	144	V _{SS}	64	V _{DD}	171	V _{DD}	91	V _{SS}	198	DQS6
11	V _{SS}	118	DQ13	38	DQ26	145	NC, TEST	65	NC	172	NC	92	DQ50	199	V _{SS}
12	DQ8	119	V _{SS}	39	DQ27	146	V _{DD}	66	V _{SS}	173	V _{SS}	93	DQ51	200	DQ54
13	DQ9	120	DM1	40	V _{SS}	147	CKE1	67	DQ32	174	DQ36	94	V _{SS}	201	DQ55
14	V _{SS}	121	V _{SS}	41	NC	148	RFU(CK E3)	68	DQ33	175	DQ37	95	DQ56	202	V _{SS}
15	RFU(CK 2)	122	CK0	42	V _{DD}	149	V _{DD}	69	V _{SS}	176	V _{SS}	96	DQ57	203	DQ60
16	RFU($\overline{CK}$ 2)	123	$\overline{CK0}$	43	CKE0	150	A15	70	$\overline{DQS4}$	177	DM4	97	V _{SS}	204	DQ61
17	V _{SS}	124	V _{SS}	44	RFU(CK E2)	151	A14	71	DQS4	178	V _{SS}	98	$\overline{DQS7}$	205	V _{SS}
18	$\overline{DQS1}$	125	DQ14	45	V _{DD}	152	V _{DD}	72	V _{SS}	179	DQ38	99	DQS7	206	DM7
19	DQS1	126	DQ15	46	BA2	153	A12	73	DQ34	180	DQ39	100	V _{SS}	207	V _{SS}
20	V _{SS}	127	V _{SS}	47	A11	154	A9	74	DQ35	181	V _{SS}	101	DQ58	208	DQ62
21	DQ10	128	DQ20	48	A7	155	A8	75	V _{SS}	182	DQ44	102	DQ59	209	DQ63
22	DQ11	129	DQ21	49	V _{DD}	156	V _{DD}	76	DQ40	183	DQ45	103	V _{SS}	210	V _{SS}
23	V _{SS}	130	V _{SS}	50	A5	157	A6	77	DQ41	184	V _{SS}	104	SDA	211	SA0
24	DQ16	131	DM2	51	A4	158	A3	78	V _{SS}	185	$\overline{DQS5}$	105	SCL	212	RFU(*1)
25	DQ17	132	V _{SS}	52	A2	159	A1	79	DM5	186	DQS5	106	NC	213	SA1
26	V _{SS}	133	DQ22	53	V _{DD}	160	V _{DD}	80	V _{SS}	187	V _{SS}	107	V _{DD} SPD	214	RFU(*2)
27	$\overline{DQS2}$	134	DQ23	54	A10/AP	161	A0	81	DQ42	188	DQ46				

Note: NC = No Connect; NC, TEST (pin 145) is for bus analysis tool and is not connected on normal memory modules. (*1) = SA0 for 2nd SPD, (*2) = SA1 for 2nd SPD.

Block Diagram: Raw Card Version A (Populated as 2 ranks of x16 SDRAMs)



Block Diagram: Raw Card Version B (Populated as 1 rank of x16 SDRAMs)



#Unless otherwise noted, resistor values are 22 Ω $\pm$ 5%
DQ wiring may differ from that described in this drawing; however, DQ/DM/DQS/DQS relationships are maintained as shown

4. Component Details

x16 Ballout for 256Mb, 512Mb, 1Gb, 2Gb and 4Gb DDR2 SDRAMs (Top View)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
VDD	NC	VSS	D	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	E	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	F	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	UDQ3	G	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	H	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	J	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	K	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	L	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	M	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	N	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	P	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	R	A2	A0	VDD
VSS	A3	A5	T	A6	A4	
	A7	A9	U	A11	A8	VSS
VDD	A12	A14	V	A15	A13	
			W			
			Y			
NC	NC		AA		NC	NC

DDR2 SDRAM FBGA Component Specifications

The DDR2 SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC MO-207 DK-Z and DL-Z.

Reference SPD Component Specifications

The Serial Presence Detect EEPROMs have their own power pin, V_{DDSPD} , so that they can be programmed or read without powering up the rest of the module. The wide voltage range permits use with 1.8V, 2.5V or 3.3V serial buses.

SPD Component DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
V_{DDSPD}	Core Supply Voltage	1.7	3.6	V