

**4.20.14 - 244-Pin PC2-4200/PC2-3200 DDR2 Registered Mini-DIMM Design
Specification**

PC2-4200/PC2-3200 DDR2 Registered Mini-DIMM

Design Specification

Revision 2.0

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Product Description

This specification defines the electrical and mechanical requirements for 244-pin, 1.8Volt, PC2-4200/PC2-3200, 72 bit-wide, Registered Double Data Rate Synchronous DRAM Mini Dual In-Line Memory Modules (DDR2 SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-3200 refers to the JEDEC standard DIMM naming convention in which PC2-4200/PC2-3200 indicates a 244-pin DIMM running at 266/200 MHz clock speed and offering 4200/3200 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered Mini-DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-3200 support. All registered Mini-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions (nominal) / MO-number, Variation	30.0 mm (height) x 82.0 mm (width) x 3.80 mm (thickness) / MO-244, variation AA
Pin count	244
SDRAMs supported	256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb
Capacity	128 MB, 256 MB, 512 MB, 1 GB, 2 GB, 4 GB
Serial PD	Consistent with JC 42.5
Voltage options	1.8 volt (V_{DD}/V_{DDQ})
Interface	SSTL_18

Environmental Requirements

DDR2 SDRAM Registered Mini-DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating temperature (ambient)	0 to +55	°C	3
H _{OPR}	Operating humidity (relative)	10 to 90	%	1
T _{STG}	Storage temperature	-50 to +100	°C	1
H _{STG}	Storage humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

Architecture

Pin Description

CK0	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
$\overline{\text{CK0}}$	Clock input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
$\overline{\text{RAS}}$	Row Address Strobe	1	DQS[8:0]	Data strobes	9
$\overline{\text{CAS}}$	Column Address Strobe	1	$\overline{\text{DQS}}$ [8:0]	Data strobes, negative line	9
$\overline{\text{WE}}$	Write Enable	1	DM[8:0]	Data Masks / Data strobes	9
$\overline{\text{S}}$ [3:0]	Chip Selects	4	RFU	Reserved for Future Use	2
A[9:0], A[15:11]	Address Inputs	15	NC	No Connect	14
A10/AP	Address Input/Autoprecharge	1	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
BA[2:0]	SDRAM Bank Addresses	3	V _{DD}	Core Power	11
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{DDQ}	I/O Power	11
SDA	SPD Data Input/Output	1	V _{SS}	Ground	64
SA[2:0]	SPD Address Inputs	3	V _{REF}	Input/Output Reference	1
$\overline{\text{RESET}}$	Register and PLL control pin	1	V _{DDSPD}	SPD Power	1
Par_In	Parity bit for the Address and Control bus	1			
$\overline{\text{Err_Out}}$	Parity error found on the Address and Control bus	1		total	244

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{\text{CK0}}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{\text{S}}[3:0]$	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{\text{S}}[0:1]$ are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, $\overline{\text{S}}[2:3]$ operate similarly to $\overline{\text{S}}[0:1]$ for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA[2:0]	IN	—	Selects which SDRAM bank of four or eight is activated.
A[15:11, 10/AP,9:0]	IN	—	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be pre-charged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD} , V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
DQS[8:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
$\overline{\text{DQS}}[8:0]$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operation.
$\overline{\text{RESET}}$	IN		The $\overline{\text{RESET}}$ pin is connected to the $\overline{\text{RST}}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus. ("1": Odd, "0": Even)
Err_Out	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools (unused on memory DIMMs)

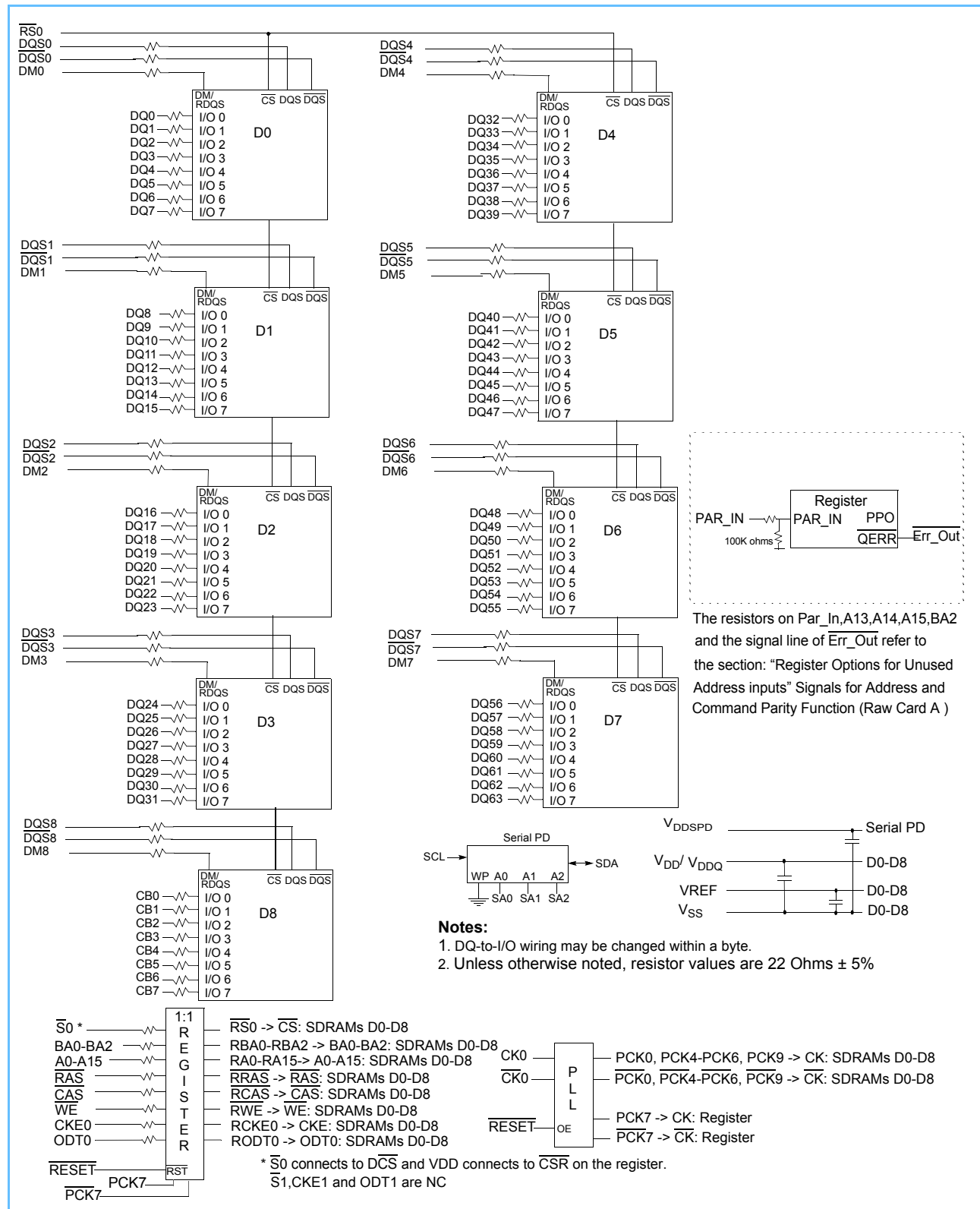
DDR2 244-pin DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REF}	123	V _{SS}	32	V _{SS}	154	DQ28	63	V _{DDQ}	185	A3	92	DQ41	214	V _{SS}
2	V _{SS}	124	DQ4	33	DQ24	155	DQ29	64	A2	186	A1	93	V _{SS}	215	DM5/DQS14
3	DQ0	125	DQ5	34	DQ25	156	V _{SS}	65	V _{DD}	187	V _{DD}	94	$\overline{\text{DQS}}_5$	216	NC, $\overline{\text{DQS}}_{14}$
4	DQ1	126	V _{SS}	35	V _{SS}	157	DM3/DQS12	KEY				95	DQS5	217	V _{SS}
5	V _{SS}	127	DM0/DQS9	36	$\overline{\text{DQS}}_3$	158	NC, $\overline{\text{DQS}}_{12}$					96	V _{SS}	218	DQ46
6	$\overline{\text{DQS}}_0$	128	NC, $\overline{\text{DQS}}_9$	37	DQS3	159	V _{SS}	66	V _{SS}	188	CK0	97	DQ42	219	DQ47
7	DQS0	129	V _{SS}	38	V _{SS}	160	DQ30	67	V _{SS}	189	$\overline{\text{CK}}_0$	98	DQ43	220	V _{SS}
8	V _{SS}	130	DQ6	39	DQ26	161	DQ31	68	NC, PAR_IN	190	V _{DD}	99	V _{SS}	221	DQ52
9	DQ2	131	DQ7	40	DQ27	162	V _{SS}	69	V _{DD}	191	A0	100	DQ48	222	DQ53
10	DQ3	132	V _{SS}	41	V _{SS}	163	CB4	70	A10/ AP	192	BA1	101	DQ49	223	V _{SS}
11	V _{SS}	133	DQ12	42	CB0	164	CB5	71	BA0	193	V _{DD}	102	V _{SS}	224	RFU, $\overline{\text{S}}_2$
12	DQ8	134	DQ13	43	CB1	165	V _{SS}	72	V _{DD}	194	$\overline{\text{RAS}}$	103	SA2	225	RFU, $\overline{\text{S}}_3$
13	DQ9	135	V _{SS}	44	V _{SS}	166	DM8/DQS17	73	$\overline{\text{WE}}$	195	V _{DDQ}	104	NC(TEST)	226	V _{SS}
14	V _{SS}	136	DM1/DQS10	45	$\overline{\text{DQS}}_8$	167	NC, $\overline{\text{DQS}}_{17}$	74	V _{DDQ}	196	$\overline{\text{S}}_0$	105	V _{SS}	227	DM6/DQS15
15	$\overline{\text{DQS}}_1$	137	NC, $\overline{\text{DQS}}_{10}$	46	DQS8	168	V _{SS}	75	$\overline{\text{CAS}}$	197	V _{DDQ}	106	$\overline{\text{DQS}}_6$	228	NC, $\overline{\text{DQS}}_{15}$
16	DQS1	138	V _{SS}	47	V _{SS}	169	CB6	76	V _{DDQ}	198	ODT0	107	DQS6	229	V _{SS}
17	V _{SS}	139	RFU	48	CB2	170	CB7	77	NC, $\overline{\text{S}}_1$	199	A13, NC	108	V _{SS}	230	DQ54
18	$\overline{\text{RESET}}$	140	RFU	49	CB3	171	V _{SS}	78	NC, ODT1	200	V _{DD}	109	DQ50	231	DQ55
19	NC	141	V _{SS}	50	V _{SS}	172	NC	79	V _{DDQ}	201	NC	110	DQ51	232	V _{SS}
20	V _{SS}	142	DQ14	51	NC	173	V _{DDQ}	80	NC	202	V _{SS}	111	V _{SS}	233	DQ60
21	DQ10	143	DQ15	52	V _{DDQ}	174	NC, CKE1	81	V _{SS}	203	DQ36	112	DQ56	234	DQ61
22	DQ11	144	V _{SS}	53	CKE0	175	V _{DD}	82	DQ32	204	DQ37	113	DQ57	235	V _{SS}
23	V _{SS}	145	DQ20	54	V _{DD}	176	A15, NC	83	DQ33	205	V _{SS}	114	V _{SS}	236	DM7/DQS16
24	DQ16	146	DQ21	55	BA2	177	A14, NC	84	V _{SS}	206	DM4/DQS13	115	$\overline{\text{DQS}}_7$	237	NC, $\overline{\text{DQS}}_{16}$
25	DQ17	147	V _{SS}	56	NC, Err_OUT	178	V _{DDQ}	85	$\overline{\text{DQS}}_4$	207	NC, $\overline{\text{DQS}}_{13}$	116	DQS7	238	V _{SS}
26	V _{SS}	148	DM2/DQS11	57	V _{DDQ}	179	A12	86	DQS4	208	V _{SS}	117	V _{SS}	239	DQ62
27	$\overline{\text{DQS}}_2$	149	NC, $\overline{\text{DQS}}_{11}$	58	A11	180	A9	87	V _{SS}	209	DQ38	118	DQ58	240	DQ63
28	DQS2	150	V _{SS}	59	A7	181	V _{DD}	88	DQ34	210	DQ39	119	DQ59	241	V _{SS}
29	V _{SS}	151	DQ22	60	V _{DD}	182	A8	89	DQ35	211	V _{SS}	120	V _{SS}	242	SDA
30	DQ18	152	DQ23	61	A5	183	A6	90	V _{SS}	212	DQ44	121	SA0	243	SCL
31	DQ19	153	V _{SS}	62	A4	184	V _{DDQ}	91	DQ40	213	DQ45	122	SA1	244	VDDSPD

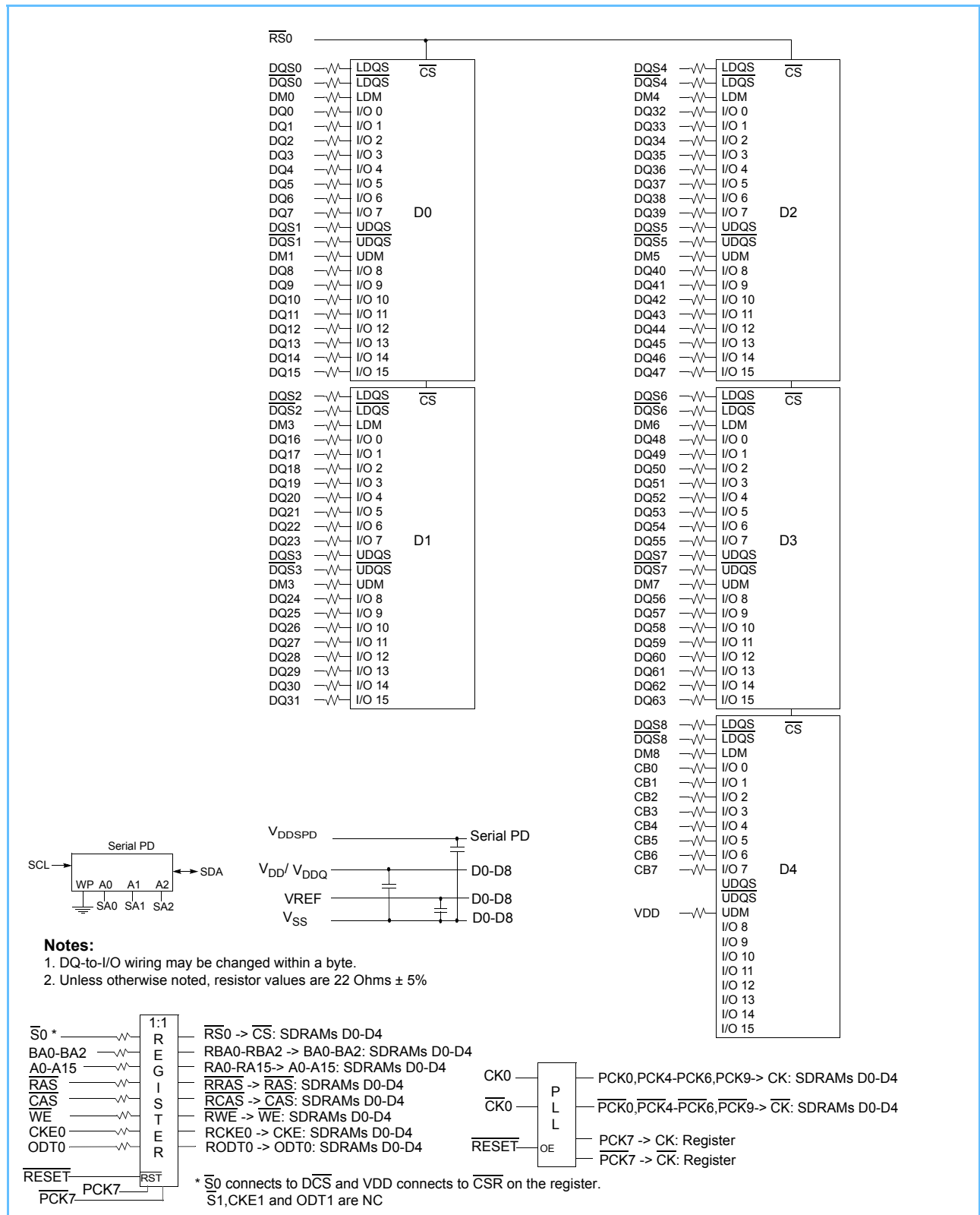
NC = No Connect; NU = Not Useable; RFU = Reserved Future Use.

1. CK1, $\overline{\text{CK}}_1$, CK2, $\overline{\text{CK}}_2$ (pins 139, 140, 224, 225) are for Unbuffered Mini-DIMM clock. These pins are RFU on registered Mini-DIMMs.
2. $\overline{\text{RESET}}$ (pin 18) is connected to both OE of the PLL and Reset of the register.
3. The TEST pin (pin 104) is reserved for bus analysis probes and is not connected on normal modules (Mini-DIMMs).
4. NC/Err_Out (pin 56) and NC/Par_In (pin 68) are optional function to check address and command parity.

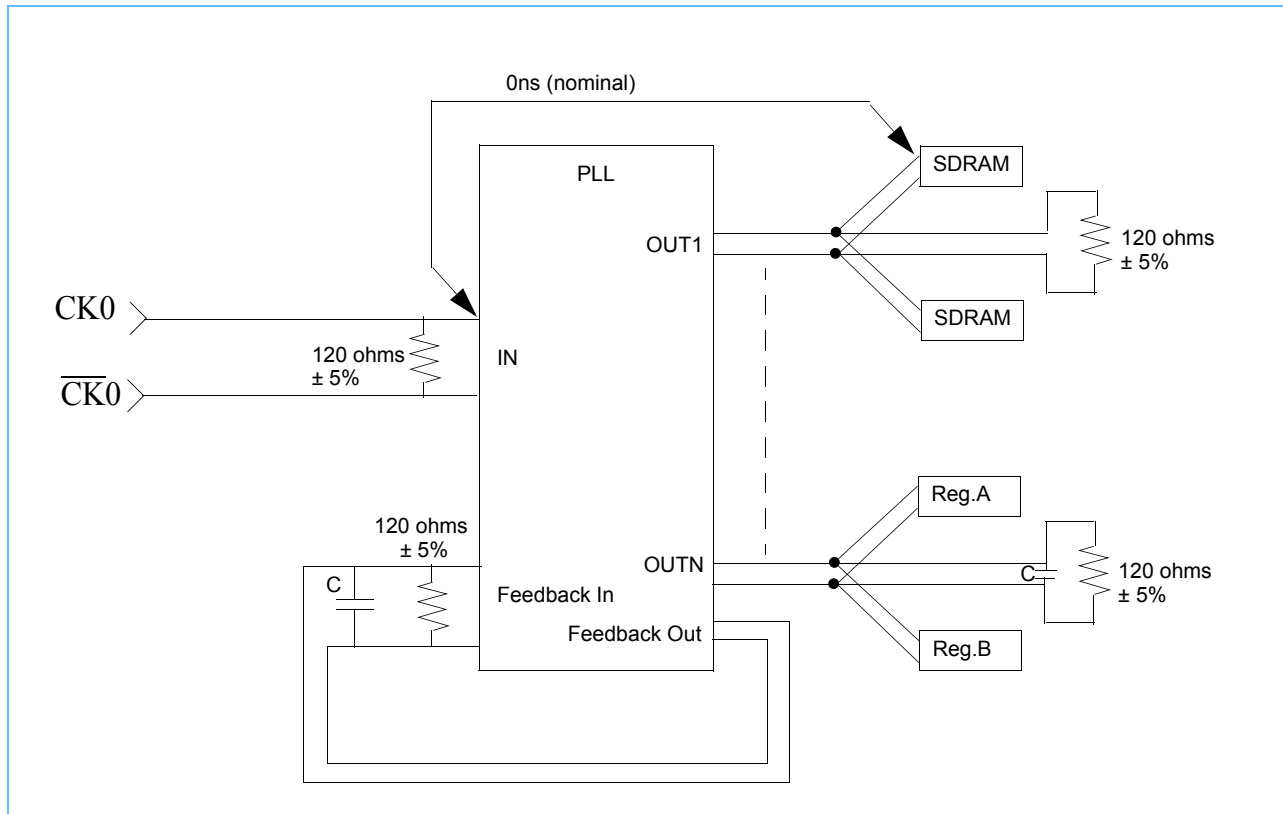
Block Diagram: Raw Card Version A (x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs)



Block Diagram: Raw Card Version B (x72 DIMM, populated as one physical rank of x16 DDR2 SDRAMs)



Differential Clock Net Wiring (CK0, $\overline{\text{CK0}}$)



1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal).
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.

Component Details

Pin Assignments for 256Mb to 4Gb; DDR2 SDRAM (Top View)

Without support balls

(MO-207 Variation DJ-z, 60Balls FBGA 0.8mm x 0.8mm pitch)

x8 Ballout of DDR2 SDRAMs (Top view) x16 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NU/ RDQS	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	$\overline{\text{UDQS}}$	VDDQ
B	DQ14	VSSQ	UDM	UDQS	VSSQ	DQ15
C	VDDQ	DQ9	VDDQ	VDDQ	DQ8	VDDQ
D	DQ12	VSSQ	DQ11	DQ10	VSSQ	DQ13
E	VDD	NC	VSS	VSSQ	$\overline{\text{LDQS}}$	VDDQ
F	DQ6	VSSQ	LDM	LDQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
L	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x8 and x16 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to next footprint on PCB.

Pin Assignments for 256Mb to 4Gb; DDR2 SDRAM (Top View)

With support balls

(MO-207 Variation DM-z, 60Balls FBGA 0.8mm x 0.8mm pitch)

x8 Ballout of DDR2 SDRAMs (Top view) x16 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NU/ RDQS	VSS	VSSQ	DQS	VDDQ
F	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	WE	RAS	CK	ODT
L	BA2	BA0	BA1	CAS	CS	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D	VDD	NC	VSS	VSSQ	UDQS	VDDQ
E	DQ14	VSSQ	UDM	UDQS	VSSQ	DQ15
F	VDDQ	DQ9	VDDQ	VDDQ	DQ8	VDDQ
G	DQ12	VSSQ	DQ11	DQ10	VSSQ	DQ13
H	VDD	NC	VSS	VSSQ	LDQS	VDDQ
J	DQ6	VSSQ	LDM	LDQS	VSSQ	DQ7
K	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
L	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
M	VDDL	VREF	VSS	VSSDL	CK	VDD
N		CKE	WE	RAS	CK	ODT
P	BA2	BA0	BA1	CAS	CS	
R		A10	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14,NC	A15,NC	A13,NC	
W						
X						
AA	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x8 and x16 DDR2 SDRAMs.
2. NC balls on A1,A2,A8,A9,W1,W2,W8 and W9 in the double line area for x8,
NC balls on A1,A2,A8,A9, AA1,AA2,AA8 and AA9 in the double line area for x16, are optional support balls.
3. Above coordinates of ball out corresponds to next footprint on PCB.
4. On the actual DIMM A1 & A9 in the double line area for x8, have via connections to VDD and VDDQ respectively.

SDRAM Landing Pattern on DIMM (Top View)

x8 footprint on PCB (Top view) x16 footprint on PCB (Top view)

	1	2	3	7	8	9		1	2	3	7	8	9
A	NU	NU			NU	NU	A	NU	NU			NU	NU
B							B						
C							C						
D	VDD	NU	VSS	VSS	NU	VDDQ	D	VDD	NU	VSS	VSS	$\overline{\text{UDQS}}$	VDD
E	NU	NU	NU	NU	NU	NU	E	DQ14	VSS	UDM	UDQS	VSS	DQ15
F	NU	NU	NU	NU	NU	NU	F	VDD	DQ9	VDD	VDD	DQ8	VDD
G	NU	NU	NU	NU	NU	NU	G	DQ12	VSS	DQ11	DQ10	VSS	DQ13
H	VDD	$\overline{\text{RDQS}}$	VSS	VSS	$\overline{\text{DQS}}$	VDD	H	VDD	NU	VSS	VSS	$\overline{\text{LDQS}}$	VDD
J	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7	J	DQ6	VSS	LDM	LDQS	VSS	DQ7
K	VDD	DQ1	VDD	VDD	DQ0	VDD	K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	DQ4	VSS	DQ3	DQ2	VSS	DQ5	L	DQ4	VSS	DQ3	DQ2	VSS	DQ5
M	VDD	VREF	VSS	VSS	CK	VDD	M	VDDL	VREF	VSS	VSSDL	CK	VDD
N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$		P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
R		A10	A1	A2	A0	VDD	R		A10	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4		T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS	U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13		V	VDD	A12	A14	A15	A13	
W							W						
X							X						
AA	NU	NU			NU	NU	AA	NU	NU			NU	NU
AB	NC	NU			NU	NU	AB	NU	NU			NU	NU

1. Above coordinates of footprint corresponds to previous ballout of DDR2 SDRAMs.
2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.
NC solder pads may be mated with any balls of an SDRAM.
3. "NU" means that the solder pad is present and may or may not be electrically connected a an active signal on the PCB. NU solder pads may only be mated with NC balls of an SDRAMs

Pin Assignment for SSTU32864 1:1 Register without Address and Command Parity Function (Top View)

96-Ball LFBGA 0.8 x 0.8 mm pitch [MO-205 CC], programmable pinout configuration

1:1 Register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	NC	VREF	VDD	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	NC	GND	GND	QODT	DNU
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCS}$	DNU
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25

1. NC (: No-Connect) denotes a ball that is not connected to the die.
2. DNU (: Do-Not-Use) denotes a ball that is connected to the die but it should be left open circuit.

Pin Assignments for PLL Clock Driver CU877 (Top View)

52-Ball FBGA 0.65 mm x 0.65 mm pitch [MO-225 BA]

	1	2	3	4	5	6
A	Y1	Y0	$\overline{Y0}$	$\overline{Y5}$	Y5	Y6
B	$\overline{Y1}$	GND	GND	GND	GND	$\overline{Y6}$
C	$\overline{Y2}$	GND			GND	$\overline{Y7}$
D	Y2	VDDQ	VDDQ	VDDQ	OS	Y7
E	CK	VDDQ			VDDQ	Fbin
F	$\overline{CK}$	VDDQ			OE	$\overline{Fbin}$
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	$\overline{Fbout}$
H	AVDD	GND			GND	Fbout
J	Y3	GND	GND	GND	GND	Y8
K	$\overline{Y3}$	$\overline{Y4}$	Y4	Y9	$\overline{Y9}$	$\overline{Y8}$