

## 4.20.16 - 144-Pin EP2-2100 DDR2 SDRAM 32b SO-DIMM Design Specification

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# EP2-2100 DDR2 SDRAM 32b-SO-DIMM

## Reference Design Specification

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## 1. Product Description

This reference specification defines the electrical and mechanical requirements for the EP2-2100 memory module, a 144-pin, 267 MHz clock (533 MT/s data rate), 32-bit wide, Unbuffered Synchronous Double Data Rate 2 (DDR2) SDRAM 32-bit Dual In-Line Memory Module (DDR2 32b-SO-DIMM). It also defines a slower version, the EP2-1600, using 200 MHz clock (400 MT/s data rate) DDR2 SDRAMs. These DDR2 32b-SO-DIMMs are intended for use in cost sensitive, low pin count applications such as peripheral devices.

Reference design examples are included which provide an initial basis for 32b-SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 267MHz clock rate support. Other designs are acceptable, and all 32b-SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

### Product Family Attributes

| Attribute:                       | Values:                                                         | Notes: |
|----------------------------------|-----------------------------------------------------------------|--------|
| 32b-SO-DIMM Organization         | x 32                                                            |        |
| 32b-SO-DIMM Dimensions (nominal) | 30.0 mm high, 67.60 mm wide / MO-274 variation AA               |        |
| 32b-SO-DIMM Types Supported      | Unbuffered                                                      |        |
| Pin Count                        | 144                                                             |        |
| Pin pitch                        | 0.8 mm                                                          |        |
| DDR SDRAMs Supported             | 256 Mb, 512 Mb, 1 Gb                                            |        |
| Capacity                         | 64 MB, 128 MB, 256 MB, 512 MB, 1 GB                             |        |
| Serial Presence Detect           | Should be consistent with JEDEC latest Revision                 |        |
| Voltage Options, Nominal         | 1.8 V $V_{DD}$<br>1.8 V $V_{DDQ}$<br>1.8 V to 3.3 V $V_{DDSPD}$ | 1      |
| Interface                        | SSTL_18                                                         |        |

Note 1:  $V_{DDSPD}$  is not tied to  $V_{DD}$  or  $V_{DDQ}$  on the DDR2 32b-SO-DIMM.

### Raw Card Summary

| Raw Card | Number of DDR SDRAMs | SDRAM Organization | Number of Ranks |
|----------|----------------------|--------------------|-----------------|
| A        | 2 or 4               | x16                | 1 or 2          |
| B        | 4 or 8               | x8                 | 1 or 2          |

## 2. Environmental Requirements

PC2-2100 DDR2 SDRAM Unbuffered 32b-SO-DIMMs are intended for use in computing peripheral environments that have limited capacity for heat dissipation.

### Absolute Maximum Ratings

| Symbol           | Parameter                                 | Rating      | Units | Notes |
|------------------|-------------------------------------------|-------------|-------|-------|
| T <sub>OPR</sub> | Operating Temperature (ambient)           | 0 to +65    | °C    | 1     |
| H <sub>OPR</sub> | Operating Humidity (relative)             | 10 to 90    | %     | 1     |
| T <sub>STG</sub> | Storage Temperature                       | -50 to +100 | °C    | 1     |
| H <sub>STG</sub> | Storage Humidity (without condensation)   | 5 to 95     | %     | 1     |
|                  | Barometric Pressure (operating & storage) | 105 to 69   | kPa   | 1, 2  |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Up to 9850 ft.

## 3. Architecture

### Pin Description

|                              |                                          |    |                               |                                                              |                   |
|------------------------------|------------------------------------------|----|-------------------------------|--------------------------------------------------------------|-------------------|
| CK[1:0]                      | Clock Inputs, positive line              | 2  | DQ[31:0]                      | Data Input/Output                                            | 32                |
| $\overline{\text{CK}}$ [1:0] | Clock inputs, negative line              | 2  | DM[3:0]                       | Data Masks                                                   | 4                 |
| CKE[1:0]                     | Clock Enables                            | 2  | DQS[3:0]                      | Data strobes                                                 | 4                 |
| $\overline{\text{RAS}}$      | Row Address Strobe                       | 1  | $\overline{\text{DQS}}$ [3:0] | Data strobes                                                 | 4                 |
| $\overline{\text{CAS}}$      | Column Address Strobe                    | 1  | TEST                          | Logic Analyzer specific test pin (No connect on 32b-SO-DIMM) | 1                 |
| $\overline{\text{WE}}$       | Write Enable                             | 1  |                               |                                                              |                   |
| $\overline{\text{S}}$ [3:0]  | Chip Selects                             | 4  | V <sub>DD</sub>               | SDRAM Core and I/O Power                                     | 13                |
| A[9:0],A[11:15]              | Address Inputs                           | 15 | V <sub>SS</sub>               | Common Ground                                                | 30                |
| A10/AP                       | Address Input/Autoprecharge              | 1  | V <sub>REF</sub>              | Input/Output Reference                                       | 1                 |
| BA[2:0]                      | SDRAM Bank Address                       | 3  | V <sub>DD</sub> SPD           | SPD Power                                                    | 1                 |
| ODT[3:0]                     | On-die termination                       | 4  | NC,V <sub>REFCA</sub>         | V <sub>REFCA</sub> for future use                            | 1                 |
| SCL                          | Serial Presence Detect (SPD) Clock Input | 1  |                               |                                                              |                   |
| SDA                          | SPD Data Input/Output                    | 1  | NC                            | Reserved for future use                                      | 12                |
| SA[2:0]                      | SPD address                              | 3  |                               |                                                              | <b>Total: 144</b> |

## Input/Output Functional Description

| Symbol                                                                        | Type   | Polarity    | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------------------------------------------------------------------|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK0/ $\overline{\text{CK0}}$ ,<br>CK1/ $\overline{\text{CK1}}$                | Input  | Cross point | The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CKE[1:0]                                                                      | Input  | Active High | Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| $\overline{\text{S}}[3:0]$                                                    | Input  | Active Low  | Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$ ; Rank 1 by $\overline{\text{S1}}$ ; Rank 2 by $\overline{\text{S2}}$ ; Rank 3 by $\overline{\text{S3}}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ ,<br>$\overline{\text{WE}}$ | Input  | Active Low  | When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ , $\overline{\text{CAS}}$ , $\overline{\text{RAS}}$ , and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| BA[2:0]                                                                       | Input  | —           | Selects which DDR2 SDRAM internal bank of four or eight is activated.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| A[9:0],<br>A10/AP,<br>A[15:11]                                                | Input  | —           | During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. |
| ODT[3:0]                                                                      | Input  | Active high | Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ if enabled via the DDR2 SDRAM mode register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| DQ[31:0]                                                                      | In/Out | —           | Data Input/Output pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| DM[3:0]                                                                       | Input  | Active High | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| $\overline{\text{DQS}}[3:0]$ ,<br>DQS[3:0]                                    | In/Out | All edges   | The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. When the DDR2 SDRAM is programmed via mode register for differential data strobe, timing is relative to the crosspoint of associated DQS and $\overline{\text{DQS}}$ signals.                                                                                                                                                                                                                                                                                                                                                                                                            |
| VREF                                                                          | Supply | —           | Supply reference voltage for SSTL_18 inputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| V <sub>DD</sub> , V <sub>DDSPD</sub> ,<br>V <sub>SS</sub>                     | Supply | —           | Power supplies for core, I/O, Serial Presence Detect, and common ground for the module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| SDA                                                                           | In/Out | —           | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V <sub>DDSPD</sub> on the system planar to act as a pull up.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| SCL                                                                           | Input  | —           | This signal is used to clock data into and out of the SPD EEPROM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SA[2:0]                                                                       | Input  | —           | Address pins used to select the Serial Presence Detect base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| TEST                                                                          | In/Out | —           | The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (32b-SO-DIMMs).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

## DDR2 SDRAM 32b-SO-DIMM Pinout

| Pin#       | Front Side       | Pin # | Back Side              | Pin # | Front Side      | Pin # | Back Side       | Pin # | Front Side      | Pin # | Back Side           |
|------------|------------------|-------|------------------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|---------------------|
| 1          | V <sub>REF</sub> | 2     | NC, V <sub>REFCA</sub> | 49    | DQ3             | 50    | CK0#            | 99    | DQ13            | 100   | V <sub>SS</sub>     |
| 3          | V <sub>SS</sub>  | 4     | NC                     | 51    | V <sub>SS</sub> | 52    | V <sub>SS</sub> | 101   | V <sub>SS</sub> | 102   | CK1                 |
| 5          | DQ16             | 6     | NC                     | 53    | NC, DQS0#       | 54    | NC, CKE1        | 103   | DQ14            | 104   | CK1#                |
| 7          | DQ17             | 8     | NC                     | 55    | DQS0            | 56    | V <sub>DD</sub> | 105   | DQ15            | 106   | V <sub>SS</sub>     |
| 9          | V <sub>SS</sub>  | 10    | NC                     | 57    | V <sub>SS</sub> | 58    | NC, ODT0        | 107   | V <sub>SS</sub> | 108   | NC, S1#             |
| 11         | DQ18             | 12    | NC                     | 59    | DM0             | 60    | CKE0            | 109   | DQ24            | 110   | V <sub>DD</sub>     |
| 13         | DQ19             | 14    | NC                     | 61    | V <sub>SS</sub> | 62    | WE#             | 111   | DQ25            | 112   | BA0                 |
| 15         | V <sub>SS</sub>  | 16    | NC                     | 63    | DQ4             | 64    | V <sub>DD</sub> | 113   | V <sub>SS</sub> | 114   | A1                  |
| 17         | DQS2#            | 18    | NC                     | 65    | DQ5             | 66    | NC, S3#         | 115   | DQ26            | 116   | A5                  |
| 19         | DQS2             | 20    | NC                     | 67    | V <sub>SS</sub> | 68    | BA1             | 117   | DQ27            | 118   | V <sub>DD</sub>     |
| 21         | V <sub>SS</sub>  | 22    | V <sub>DD</sub>        | 69    | DQ6             | 70    | A10/AP          | 119   | V <sub>SS</sub> | 120   | A9                  |
| 23         | DM2              | 24    | NC, A14                | 71    | DQ7             | 72    | V <sub>DD</sub> | 121   | DQS3#           | 122   | A12                 |
| 25         | V <sub>SS</sub>  | 26    | NC, A13                | 73    | V <sub>SS</sub> | 74    | A3              | 123   | DQS3            | 124   | V <sub>DD</sub>     |
| 27         | DQ20             | 28    | A11                    | 75    | DQ8             | 76    | A7              | 125   | V <sub>SS</sub> | 126   | NC                  |
| 29         | DQ21             | 30    | V <sub>DD</sub>        | 77    | DQ9             | 78    | NC, A15         | 127   | DM3             | 128   | NC                  |
| 31         | V <sub>SS</sub>  | 32    | A6                     | 79    | V <sub>SS</sub> | 80    | V <sub>DD</sub> | 129   | V <sub>SS</sub> | 130   | NC                  |
| 33         | DQ22             | 34    | A2                     | 81    | DQ10            | 82    | RESET#          | 131   | DQ28            | 132   | V <sub>SS</sub>     |
| 35         | DQ23             | 36    | CAS#                   | 83    | DQ11            | 84    | A8              | 133   | DQ29            | 134   | SDA                 |
| 37         | V <sub>SS</sub>  | 38    | V <sub>DD</sub>        | 85    | V <sub>SS</sub> | 86    | A4              | 135   | V <sub>SS</sub> | 136   | SA0                 |
| <b>KEY</b> |                  |       |                        | 87    | NC, DQS1#       | 88    | V <sub>DD</sub> | 137   | DQ30            | 138   | SA1                 |
| 39         | V <sub>SS</sub>  | 40    | NC, S2#                | 89    | DQS1            | 90    | A0              | 139   | DQ31            | 140   | SA2                 |
| 41         | DQ0              | 42    | V <sub>DD</sub>        | 91    | V <sub>SS</sub> | 92    | NC, BA2         | 141   | V <sub>SS</sub> | 142   | SCL                 |
| 43         | DQ1              | 44    | NC, ODT1               | 93    | DM1             | 94    | S0#             | 143   | NC, TEST        | 144   | V <sub>DD</sub> SPD |
| 45         | V <sub>SS</sub>  | 46    | V <sub>SS</sub>        | 95    | V <sub>SS</sub> | 96    | V <sub>DD</sub> |       |                 |       |                     |
| 47         | DQ2              | 48    | CK0                    | 97    | DQ12            | 98    | RAS#            |       |                 |       |                     |

**Note:** NC = No Connect.

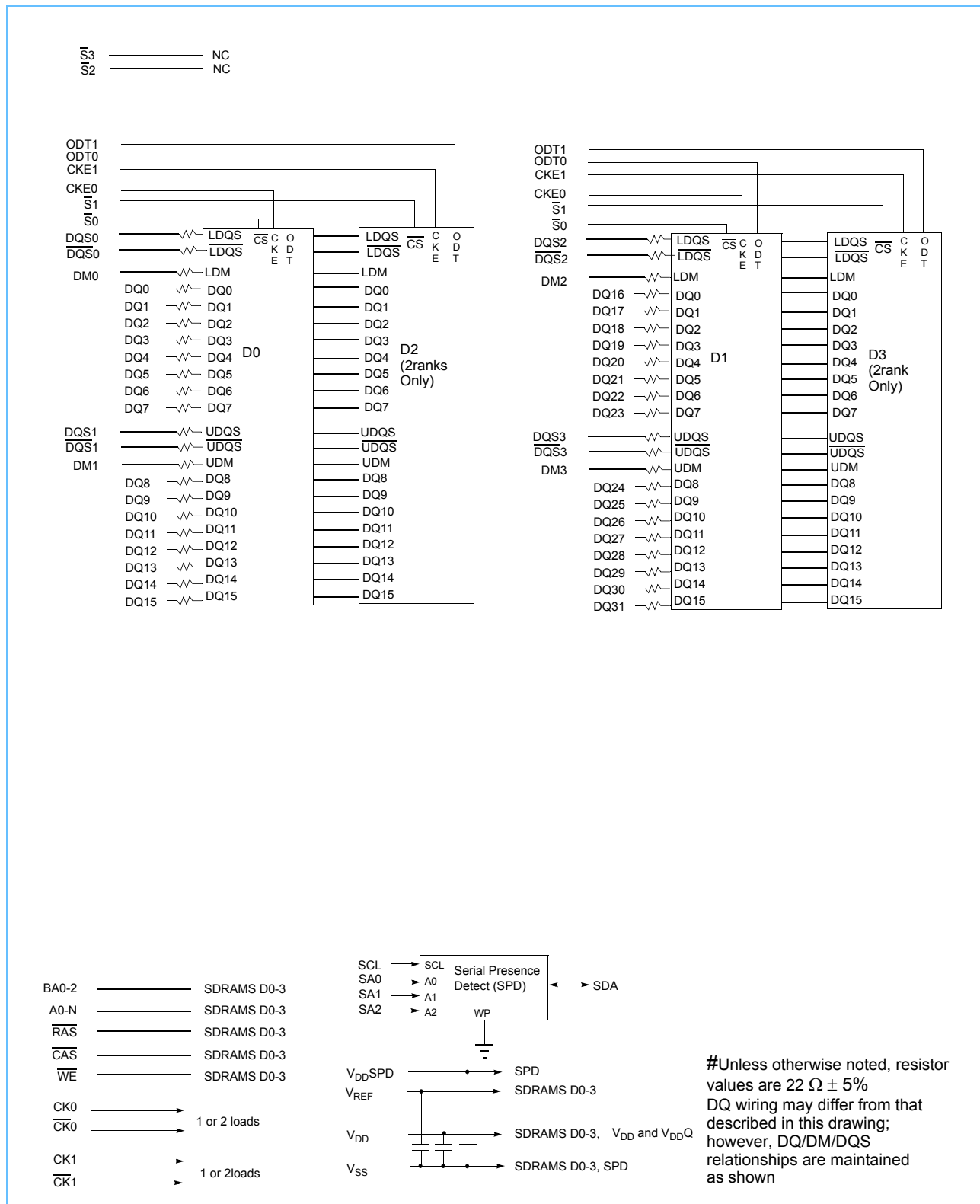
**Note:** NC,TEST(pin 143) is for bus analysis tool and is not connected on normal memory modules.

**Note:** RESET# not used on modules without PLL.

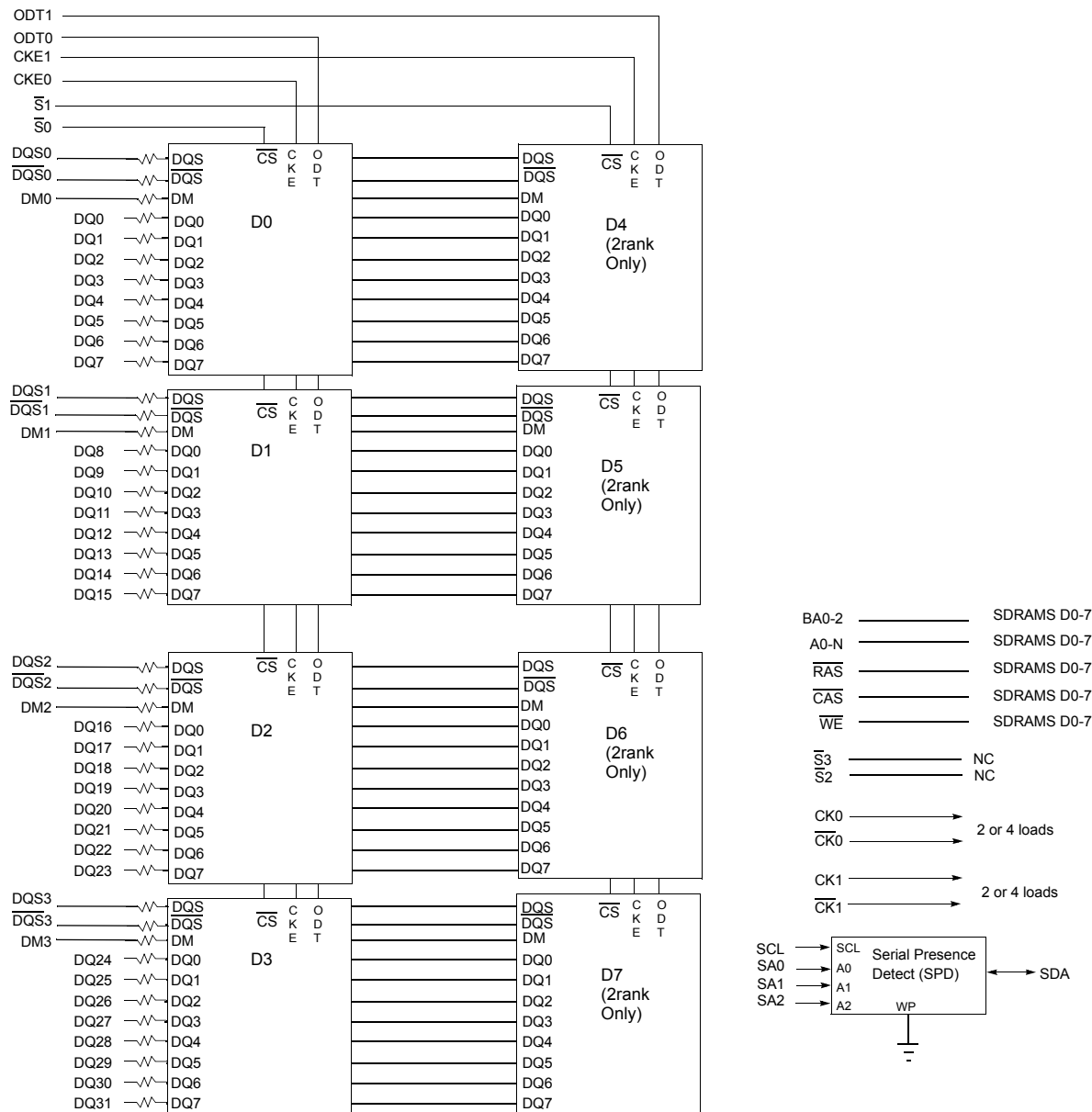
**Note:** For future compatibility, systems should ground undriven address and bank address inputs.

**Note:**

**Note:**

**Block Diagram: Raw Card Version A** (Populated as 1 or 2 rank of x16 SDRAMs)

Block Diagram: Raw Card Version B (Populated as 1 or 2 rank of x8 SDRAMs)



#Unless otherwise noted, resistor values are  $22\ \Omega \pm 5\%$   
DQ wiring may differ from that described in this drawing; however, DQ/DM/DQS relationships are maintained as shown

4. Component Details

32b-SO-DIMM Common ball pattern for x8 and x16 - 256Mb, 512Mb, 1Gb DDR SDRAM Planar Components (Top View)

