

## 4.20.17 - 214-Pin PC3-12800 DDR3 Unbuffered MicroDIMM Design Specification

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# **PC3-12800 DDR3 Unbuffered MicroDIMM Reference Design Specification**

Revision 0.34

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## 1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC3-12800 memory module, a 214-pin, 800MHz clock (16000 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate 3(DDR3) DRAM Micro Dual In-Line Memory Module (DDR3 SDRAM MicroDIMMs). It also defines a slower version, the PC3-10600, using 667MHz clock (1333 MT/s data rate) DDR3 SDRAMs, the PC3-8500, using 533MHz clock (1066 MT/s data rate) DDR3 SDRAMs, the PC3-6400, using 400MHz clock (800 MT/s data rate) DDR3 SDRAMs. These DDR3 SDRAM MicroDIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered MicroDIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 800MHz clock rate support. Other designs are acceptable, and all Unbuffered DDR3 MicroDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

### Product Family Attributes

| Attribute:                                                                      | Values:                                                        | Notes: |
|---------------------------------------------------------------------------------|----------------------------------------------------------------|--------|
| MicroDIMM Organization                                                          | x 64                                                           |        |
| MicroDIMM Dimensions (nominal)                                                  | 30 mm high, 54.0mm wide                                        |        |
| MicroDIMM Types Supported                                                       | Unbuffered                                                     |        |
| Pin Count                                                                       | 214                                                            |        |
| SDRAMs Supported                                                                | 512 Mb, 1 Gb, 2 Gb, 4 Gb                                       |        |
| Capacity                                                                        | 256 MB, 512 MB, 1 GB, 2GB                                      |        |
| Serial Presence Detect                                                          | Should be consistent with JEDEC latest Rev.                    |        |
| Voltage Options, Nominal                                                        | 1.5 V $V_{DD}$<br>1.5 V $V_{DDQ}$<br>3.0V to 3.6 V $V_{DDSPD}$ | 1      |
| Interface                                                                       | SSTL_15                                                        |        |
| Note 1: $V_{DDSPD}$ is not tied to $V_{DD}$ or $V_{DDQ}$ on the DDR3 MicroDIMM. |                                                                |        |

### Raw Card Summary

| Raw Card | Number of DDR3 SDRAMs | SDRAM Organization | Number of Ranks |
|----------|-----------------------|--------------------|-----------------|
| A        | 4                     | x16                | 1               |

## 2. Environmental Requirements

PC3-12800 DDR3 SDRAM Unbuffered MicroDIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

### Absolute Maximum Ratings

| Symbol    | Parameter                       | Rating   | Units | Notes |
|-----------|---------------------------------|----------|-------|-------|
| $T_{OPR}$ | Operating Temperature (ambient) | 0 to +65 | °C    | 1     |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 3. Architecture

### Pin Description

|                       |                                          |    |                        |                                                            |            |
|-----------------------|------------------------------------------|----|------------------------|------------------------------------------------------------|------------|
| CK[1:0]               | Clock Inputs, positive line              | 2  | DQS[7:0]               | Data strobes                                               | 8          |
| $\overline{CK}$ [1:0] | Clock inputs, negative line              | 2  | $\overline{DQS}$ [7:0] | Data strobes complement                                    | 8          |
| CKE[1:0]              | Clock Enables                            | 2  |                        |                                                            |            |
| $\overline{RAS}$      | Row Address Strobe                       | 1  | $\overline{EVENT}$     | Thermal sensor EVENT signal                                | 1          |
| $\overline{CAS}$      | Column Address Strobe                    | 1  | $\overline{RESET}$     | DDR3 SDRAM RESET signal                                    | 1          |
| $\overline{WE}$       | Write Enable                             | 1  | NC, TEST               | Logic Analyzer specific test pin (No connect on MicroDIMM) | 1          |
| $\overline{S}$ [1:0]  | Chip Selects                             | 2  |                        |                                                            |            |
| A[9:0], A11, A[15:13] | Address Inputs                           | 14 | $V_{DD}$               | Core and I/O Power                                         | 18         |
| A10/AP                | Address Input/Autoprecharge              | 1  | $V_{SS}$               | Ground                                                     | 56         |
| A12/ $\overline{BC}$  | Address Input/Burst Chop                 | 1  | $V_{REFDQ}$            | Input/Output Reference for Data                            | 1          |
|                       |                                          |    | $V_{REFCA}$            | Input/Output Reference for Commands and address            | 1          |
| BA[2:0]               | SDRAM Bank Address                       | 3  |                        |                                                            |            |
| ODT[1:0]              | On-die termination control               | 2  |                        |                                                            |            |
| SCL                   | Serial Presence Detect (SPD) Clock Input | 1  | $V_{tt}$               | Termination Voltage                                        | 2          |
| SDA                   | SPD Data Input/Output                    | 1  | $V_{DDSPD}$            | SPD Power                                                  | 1          |
| SA[1:0]               | SPD address                              | 2  |                        |                                                            |            |
|                       |                                          |    | NC                     | No connect                                                 | 8          |
| DQ[63:0]              | Data Input/Output                        | 64 |                        |                                                            |            |
| DM[7:0]               | Data Masks                               | 8  |                        |                                                            |            |
| <b>Total:</b>         |                                          |    |                        |                                                            | <b>214</b> |

## Input/Output Functional Description

| Symbol                                                                        | Type   | Polarity    | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------------------------------------------------------------------|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK0/ $\overline{\text{CK0}}$ ,<br>CK1/ $\overline{\text{CK1}}$                | Input  | Cross point | <b>Clock:</b> CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$ . Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| CKE[1:0]                                                                      | Input  | Active High | <b>Clock Enable:</b> CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$ , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. |
| $\overline{\text{S}}$ [1:0]                                                   | Input  | Active Low  | <b>Chip Select:</b> All commands are masked when $\overline{\text{S}}$ is registered HIGH. $\overline{\text{S}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{S}}$ is considered part of the command code.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ ,<br>$\overline{\text{WE}}$ | Input  | Active Low  | <b>Command Inputs:</b> $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{S}}$ ) define the command being entered.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| BA[2:0]                                                                       | Input  | —           | <b>Bank Address Inputs:</b> BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| ODT[1:0]                                                                      | Input  | Active High | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ , and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU/ $\overline{\text{DQSU}}$ , DQSL/ $\overline{\text{DQSL}}$ , DMU, and DML signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.                                                                                                                                                                                                                                                                                                                      |
| A0 -A15                                                                       | Input  | —           | <b>Address Inputs:</b> Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below). The address inputs also provide the op-code during (Extended) Mode Register Set commands.                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| A10/AP                                                                        | Input  |             | <b>Autoprecharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.                                                                                                                                                                                                                                                                                                                                              |
| A12/ $\overline{\text{BC}}$                                                   | Input  |             | <b>Burst Chop:</b> A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| DQ[63:0]                                                                      | In/Out | —           | Data Input/Output pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| DM[7:0]                                                                       | Input  | Active High | <b>Input Data Mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM is enabled by EMRS command.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| $\overline{\text{DQS}}$ [7:0],<br>DQS[7:0]                                    | In/Out | Cross point | <b>Data Strobe:</b> output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL, and DQSU are paired with differential signals $\overline{\text{DQS}}$ , $\overline{\text{DQSL}}$ , and $\overline{\text{DQSU}}$ , respectively, to provide differential pair signaling to the system during reads and writes.                                                                                                                                                                                                                                                                                                       |
| V <sub>DD</sub> , V <sub>DDSPD</sub> ,<br>V <sub>SS</sub>                     | Supply | —           | Power supplies for core, I/O, Serial Presence Detect, and ground for the module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

## Input/Output Functional Description

| Symbol                       | Type   | Polarity   | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|--------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{REFCA}$ ,<br>$V_{REFDQ}$ | Supply | ---        | Reference Voltage for Data, Commands and Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SDA                          | In/Out | —          | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to $V_{DD}$ to act as a pull up.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SCL                          | Input  | —          | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to $V_{DD}$ to act as a pull up.                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| SA[1:0]                      | Input  | —          | Address pins used to select the Serial Presence Detect base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| NC,TEST                      | In/Out | —          | The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (MicroDIMMs).                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| $\overline{RESET}$           | Input  | Active Low | $\overline{RESET}$ is an active low input to the DRAM compatible with a CMOS rail to rail signal with a DC high $\Rightarrow 0.8 * V_{DDQ}$ and DC low $\leq 0.2 * V_{DDQ}$ , i.e., 1.20V for high and 0.30V for low. $\overline{RESET}$ is referenced to VSS. No signal termination is required for $\overline{RESET}$ . It is expected that the $\overline{RESET}$ signal will be heavily loaded across multiple chips. A slow slew rate receiver design is recommended. It is also recommended that DRAM designs implement on-chip noise filtering to prevent false triggering. |
| $\overline{EVENT}$           | Output | Active Low | $\overline{EVENT}$ signal from the thermal sensor                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

## DDR3 SDRAM MicroDIMM Pinout

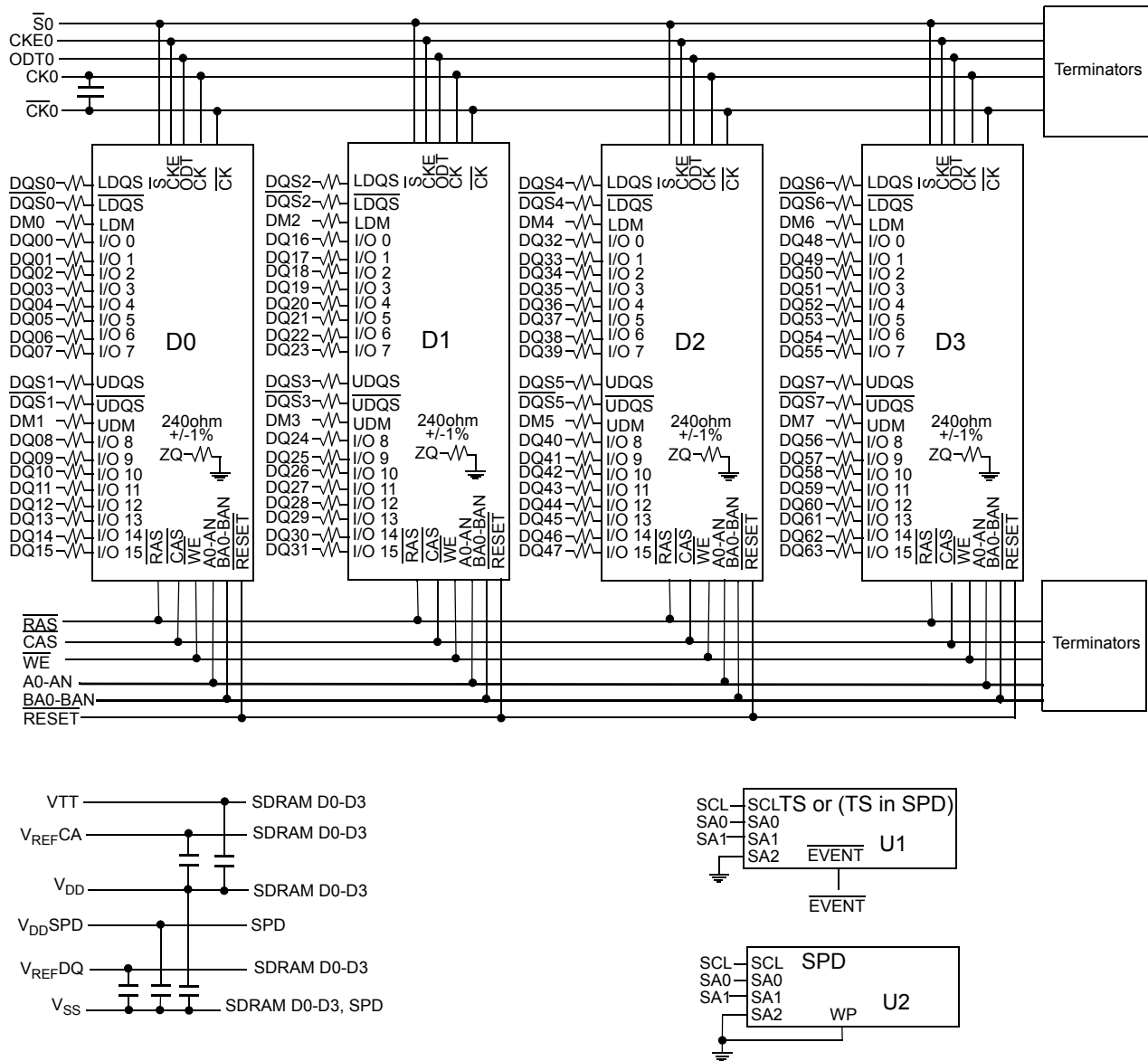
| Pin # | Lower Side               | Pin # | Upper Side               | Pin # | Lower Side                  | Pin # | Upper Side                | Pin # | Lower Side               | Pin # | Upper Side               | Pin # | Lower Side               | Pin # | Upper Side                |
|-------|--------------------------|-------|--------------------------|-------|-----------------------------|-------|---------------------------|-------|--------------------------|-------|--------------------------|-------|--------------------------|-------|---------------------------|
| 1     | V <sub>REFD</sub><br>Q   | 108   | V <sub>SS</sub>          | 28    | DM3                         | 135   | DQS2                      | 55    | V <sub>DD</sub>          | 162   | V <sub>DD</sub>          | 82    | DQ34                     | 189   | DQ47                      |
| 2     | V <sub>SS</sub>          | 109   | DQ4                      | 29    | V <sub>SS</sub>             | 136   | V <sub>SS</sub>           | 56    | A10/AP                   | 163   | A0                       | 83    | DQ35                     | 190   | V <sub>SS</sub>           |
| 3     | DQ12                     | 110   | DQ5                      | 30    | $\overline{\text{DQS3}}$    | 137   | DQ22                      | 57    | BA0                      | 164   | BA1                      | 84    | V <sub>SS</sub>          | 191   | DQ42                      |
| 4     | DQ13                     | 111   | V <sub>SS</sub>          | 31    | DQS3                        | 138   | DQ23                      | 58    | V <sub>DD</sub>          | 165   | V <sub>DD</sub>          | 85    | V <sub>SS</sub>          | 192   | DQ43                      |
| 5     | V <sub>SS</sub>          | 112   | DQ0                      | 32    | V <sub>SS</sub>             | 139   | V <sub>SS</sub>           | 59    | $\overline{\text{S0}}$   | 166   | $\overline{\text{RAS}}$  | 86    | V <sub>SS</sub>          | 193   | V <sub>SS</sub>           |
| 6     | DQ8                      | 113   | DQ1                      | 33    | DQ30                        | 140   | DQ18                      | 60    | $\overline{\text{CAS}}$  | 167   | $\overline{\text{WE}}$   | 87    | DQ52                     | 194   | DQ60                      |
| 7     | DQ9                      | 114   | V <sub>SS</sub>          | 34    | DQ31                        | 141   | DQ19                      | 61    | V <sub>DD</sub>          | 168   | V <sub>DD</sub>          | 88    | DQ53                     | 195   | DQ61                      |
| 8     | V <sub>SS</sub>          | 115   | DM0                      | 35    | V <sub>SS</sub>             | 142   | V <sub>SS</sub>           | 62    | A13 <sup>3</sup>         | 169   | ODT0                     | 89    | V <sub>SS</sub>          | 196   | V <sub>SS</sub>           |
| 9     | DM1                      | 116   | V <sub>SS</sub>          | 36    | DQ26                        | 143   | NC                        | 63    | ODT1                     | 170   | $\overline{\text{S1}}$   | 90    | DQ48                     | 197   | DQ56                      |
| 10    | V <sub>SS</sub>          | 117   | $\overline{\text{DQS0}}$ | 37    | DQ27                        | 144   | NC                        | 64    | V <sub>DD</sub>          | 171   | V <sub>DD</sub>          | 91    | DQ49                     | 198   | DQ57                      |
| 11    | $\overline{\text{DQS1}}$ | 118   | DQS0                     | 38    | V <sub>SS</sub>             | 145   | $\overline{\text{RESET}}$ | 65    | NC, TEST                 | 172   | NC                       | 92    | V <sub>SS</sub>          | 199   | V <sub>SS</sub>           |
| 12    | DQS1                     | 119   | V <sub>SS</sub>          | 39    | NC                          | 146   | NC                        | 66    | NC                       | 173   | V <sub>REFCA</sub>       | 93    | DM6                      | 200   | DM7                       |
| 13    | V <sub>SS</sub>          | 120   | DQ6                      | 40    | V <sub>DD</sub>             | 147   | V <sub>DD</sub>           | 67    | V <sub>SS</sub>          | 174   | NC                       | 94    | V <sub>SS</sub>          | 201   | V <sub>SS</sub>           |
| 14    | DQ14                     | 121   | DQ7                      | 41    | CKE0                        | 148   | CKE1                      | 68    | DQ36                     | 175   | NC                       | 95    | $\overline{\text{DQS6}}$ | 202   | $\overline{\text{DQS7}}$  |
| 15    | DQ15                     | 122   | V <sub>SS</sub>          | 42    | A14 <sup>3</sup>            | 149   | A15 <sup>3</sup>          | 69    | DQ37                     | 176   | V <sub>SS</sub>          | 96    | DQS6                     | 203   | DQS7                      |
| 16    | V <sub>SS</sub>          | 123   | DQ2                      | 43    | V <sub>DD</sub>             | 150   | V <sub>DD</sub>           | 70    | V <sub>SS</sub>          | 177   | DQ44                     | 97    | V <sub>SS</sub>          | 204   | V <sub>SS</sub>           |
| 17    | DQ10                     | 124   | DQ3                      | 44    | A12/ $\overline{\text{BC}}$ | 151   | BA2                       | 71    | DQ32                     | 178   | DQ45                     | 98    | DQ54                     | 205   | DQ62                      |
| 18    | DQ11                     | 125   | V <sub>SS</sub>          | 45    | A11                         | 152   | A9                        | 72    | DQ33                     | 179   | V <sub>SS</sub>          | 99    | DQ55                     | 206   | DQ63                      |
| 19    | V <sub>SS</sub>          | 126   | DQ20                     | 46    | V <sub>DD</sub>             | 153   | V <sub>DD</sub>           | 73    | V <sub>SS</sub>          | 180   | DQ40                     | 100   | V <sub>SS</sub>          | 207   | V <sub>SS</sub>           |
| 20    | V <sub>SS</sub>          | 127   | DQ21                     | 47    | A8                          | 154   | A7                        | 74    | DM4                      | 181   | DQ41                     | 101   | DQ50                     | 208   | DQ58                      |
| 21    | V <sub>SS</sub>          | 128   | V <sub>SS</sub>          | 48    | A5                          | 155   | A6                        | 75    | V <sub>SS</sub>          | 182   | V <sub>SS</sub>          | 102   | DQ51                     | 209   | DQ59                      |
| 22    | DQ28                     | 129   | DQ16                     | 49    | V <sub>DD</sub>             | 156   | V <sub>DD</sub>           | 76    | $\overline{\text{DQS4}}$ | 183   | DM5                      | 103   | V <sub>SS</sub>          | 210   | V <sub>SS</sub>           |
| 23    | DQ29                     | 130   | DQ17                     | 50    | A3                          | 157   | A4                        | 77    | DQS4                     | 184   | V <sub>SS</sub>          | 104   | SA0                      | 211   | $\overline{\text{EVENT}}$ |
| 24    | V <sub>SS</sub>          | 131   | V <sub>SS</sub>          | 51    | A2                          | 158   | A1                        | 78    | V <sub>SS</sub>          | 185   | $\overline{\text{DQS5}}$ | 105   | V <sub>DD</sub> SPD      | 212   | SDA                       |
| 25    | DQ24                     | 132   | DM2                      | 52    | V <sub>DD</sub>             | 159   | V <sub>DD</sub>           | 79    | DQ38                     | 186   | DQS5                     | 106   | SA1                      | 213   | SCL                       |
| 26    | DQ25                     | 133   | V <sub>SS</sub>          | 53    | CK1                         | 160   | CK0                       | 80    | DQ39                     | 187   | V <sub>SS</sub>          | 107   | VTT                      | 214   | VTT                       |
| 27    | V <sub>SS</sub>          | 134   | $\overline{\text{DQS2}}$ | 54    | $\overline{\text{CK1}}$     | 161   | $\overline{\text{CK0}}$   | 81    | V <sub>SS</sub>          | 188   | DQ46                     |       |                          |       |                           |

Note.

1. NC = No Connect; NU = Not Useable, RFU = Reserved Future Use.

2. TEST(pin 65) is reserved for bus analysis probes and is NC on normal memory modules.

3. This address might be connected to NC balls of the NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

**Block Diagram: Raw Card Version A** (Populated as 1rank of x16 SDRAMs)

## 4. Component Details

### x16 Ballout(MO-207 DU-Z)for 512Mb, 1Gb, 2Gb and 4Gb DDR3 SDRAMs (Top View)

| 1      | 2                         | 3                        |   | 7                               | 8      | 9    |
|--------|---------------------------|--------------------------|---|---------------------------------|--------|------|
| VDDQ   | DQU5                      | DQU7                     | A | DQU4                            | VDDQ   | VSS  |
| VSSQ   | VDD                       | VSS                      | B | $\overline{\text{DQS}}\text{U}$ | DQU6   | VSSQ |
| VDDQ   | DQU3                      | DQU1                     | C | DQSU                            | DQU2   | VDDQ |
| VSSQ   | VDDQ                      | DMU                      | D | DQU0                            | VSSQ   | VDD  |
| USS    | VSSQ                      | DQL0                     | E | DML                             | VSSQ   | VDDQ |
| VDDQ   | DQL2                      | DQSL                     | F | DQL1                            | DQL3   | VSSQ |
| VDDQ   | DQL6                      | $\overline{\text{DQSL}}$ | G | VDD                             | VSS    | USSQ |
| VREFDQ | VDDQ                      | DQL4                     | H | DQL7                            | DQL5   | VDDQ |
| NC     | VSS                       | $\overline{\text{RAS}}$  | J | CK                              | VSS    | NC   |
| ODT    | VDD                       | $\overline{\text{CAS}}$  | K | $\overline{\text{CK}}$          | VDD    | CKE  |
| NC     | $\overline{\text{CS}}$    | $\overline{\text{WE}}$   | L | A10/AP                          | ZQ     | NC   |
| VSS    | BA0                       | BA2                      | M | A15                             | VREFCA | VSS  |
| VDD    | A3                        | A0                       | N | A12/ $\overline{\text{BC}}$     | BA1    | VDD  |
| VSS    | A5                        | A2                       | P | A1                              | A4     | VSS  |
| VDD    | A7                        | A9                       | R | A11                             | A6     | VDD  |
| VSS    | $\overline{\text{RESET}}$ | A13                      | T | A14                             | A8     | VSS  |