

4.20.2 – 168 Pin, PC133 SDRAM Registered DIMM DESIGN SPECIFICATION

PC133 SDRAM Registered DIMM

Design Specification

Revision 1.4

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Product Description

This specification defines the electrical and mechanical requirements for 168-pin, 3.3 volt, 133MHz, 72-bit wide, Registered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs). These SDRAM DIMMs are used as main memory when installed in systems such as servers and workstations.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for 133MHz support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 168-pin 8-Byte Registered SDRAM DIMM product. (Refer to JEDEC standard 21-C, Section 4.5.7, at www.jedec.org).

Product Family Attributes

DIMM Organization	x 72 ECC
DIMM Dimensions (nominal)	5.25" x 1.5"/1.7" x .157"/.320"
	5.25" x 1.2" x .157"/.254"
Pin Count	168
SDRAMs Supported	64Mb, 128Mb, 256Mb, 512Mb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB
Serial PD	Consistent with JEDEC Rev. 1.2
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

Environmental Requirements

PC133 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functionality is not guaranteed.

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +55	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and the device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft.				

Architecture

Pin Description

CK(0:3)	Clock Inputs	DQ(0:63)	Data Input/Output
CKE(0:1)	Clock Enables	CB(0:7)	ECC Data Input/Output
RAS	Row Address Strobe	DQMB(0:7)	Data Mask
CAS	Column Address Strobe	V _{DD}	Power (3.3V)
WE	Write Enable	V _{SS}	Ground
$\overline{S}$ (0:3)	Chip Selects	NC	No Connect
A(0:9,11:12)	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0-BA1	SDRAM Bank Address	SA(0:2)	Serial Presence Detect Address Inputs
REGE	Register Enable	NC	No Connect
DU	Don't Use - leave as NC		

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK3	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock. CK0 drives the PLL. CK1, CK2 & CK3 are terminated.
CKE0,1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0} - \overline{S3}$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S0}$ and $\overline{S2}$; Bank 1 is selected by $\overline{S1}$ and $\overline{S3}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, 1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-12 A10/AP	Input	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A10 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	—	Data and Check Bit Input/Output pins.
DQMB0 - DQMB7	Input	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB has a latency of two clock cycles in Buffered mode or three clock cycles in Registered mode, and controls the output buffers like an output enable. In Write mode, DQMB has a zero clock latency in Buffered mode and a latency of one clock cycle in Registered mode. In this case, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.
V_{DD} , V_{SS}	Supply		Power and ground for the module.
REGE	Input	Active High (Register Mode Enable)	The Register Enable pin is used to permit the DIMM to operate in Buffered mode (inputs re-driven asynchronously) or Registered mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock).
SA0 - 2	Input	—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the SPD EEPROM.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus time to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull up.

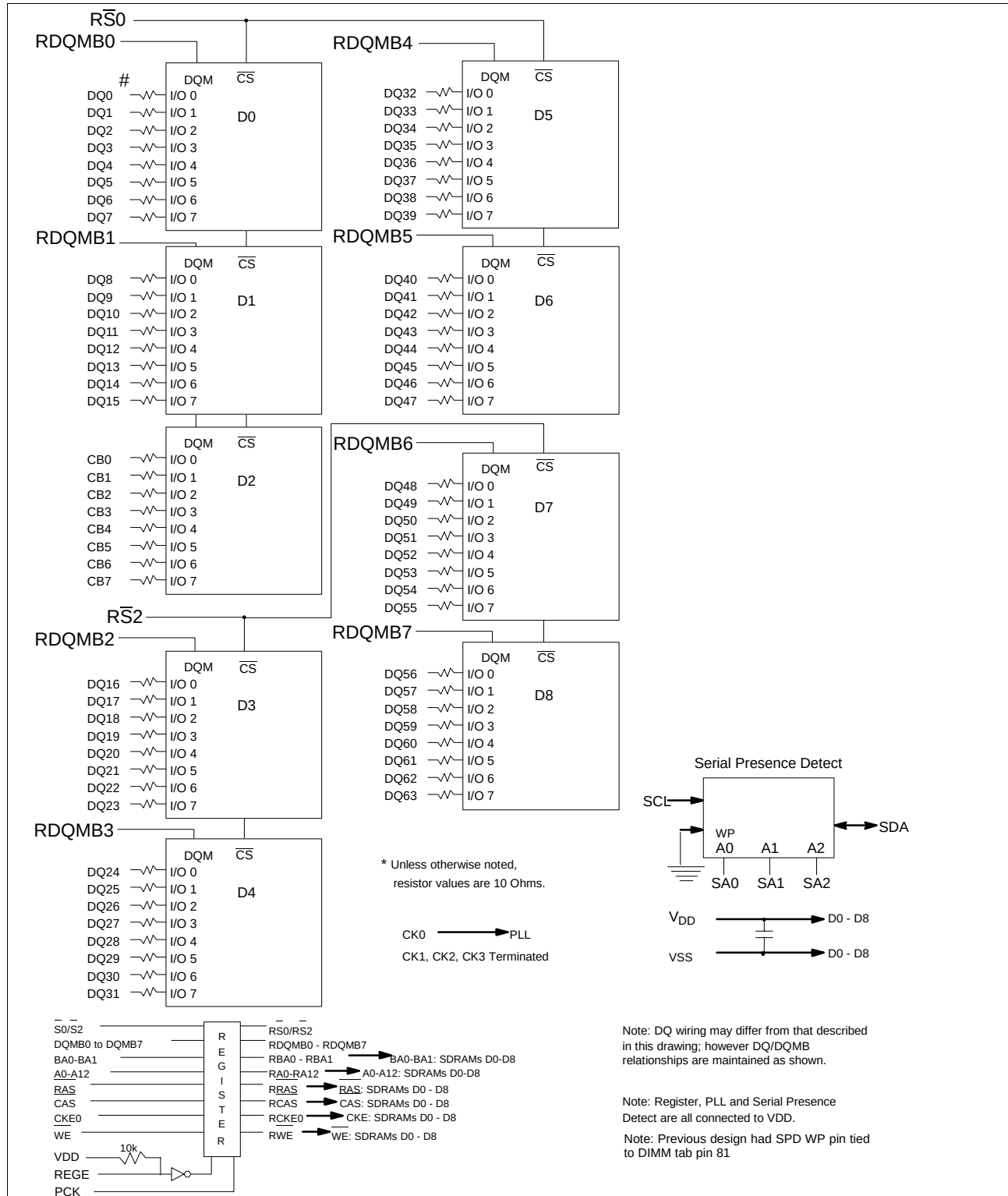
Registered SDRAM DIMM Pinout

Pin#	Front Side	Pin#	Back Side	Pin #	Front Side	Pin#	Back Side	Pin #	Front Side	Pin#	Back Side	Pin #	Front Side	Pin#	Back Side
1	V _{SS}	85	V _{SS}	22	CB1	106	CB5	43	V _{SS}	127	V _{SS}	64	V _{SS}	148	V _{SS}
2	DQ0	86	DQ32	23	V _{SS}	107	V _{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S}2$	129	$\overline{S}3$	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V _{DD}	110	V _{DD}	47	DQMB3	131	DQMB7	68	V _{SS}	152	V _{SS}
6	V _{DD}	90	V _{DD}	27	$\overline{WE}$	111	$\overline{CAS}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V _{DD}	133	V _{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S}0$	114	$\overline{S}1$	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	RAS	52	CB2	136	CB6	73	V _{DD}	157	V _{DD}
11	DQ8	95	DQ40	32	V _{SS}	116	V _{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V _{SS}	96	V _{SS}	33	A0	117	A1	54	V _{SS}	138	V _{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V _{SS}	162	V _{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V _{DD}	143	V _{DD}	80	NC	164	NC
18	V _{DD}	102	V _{DD}	39	BA1	123	A11	60	DQ20	144	DQ52	81	DU	165	SA0
19	DQ14	103	DQ46	40	V _{DD}	124	V _{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V _{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	A12	63	CKE1,NC	147	REGE	84	V _{DD}	168	V _{DD}

Note: All pin assignments are consistent with all 8-byte unbuffered versions.

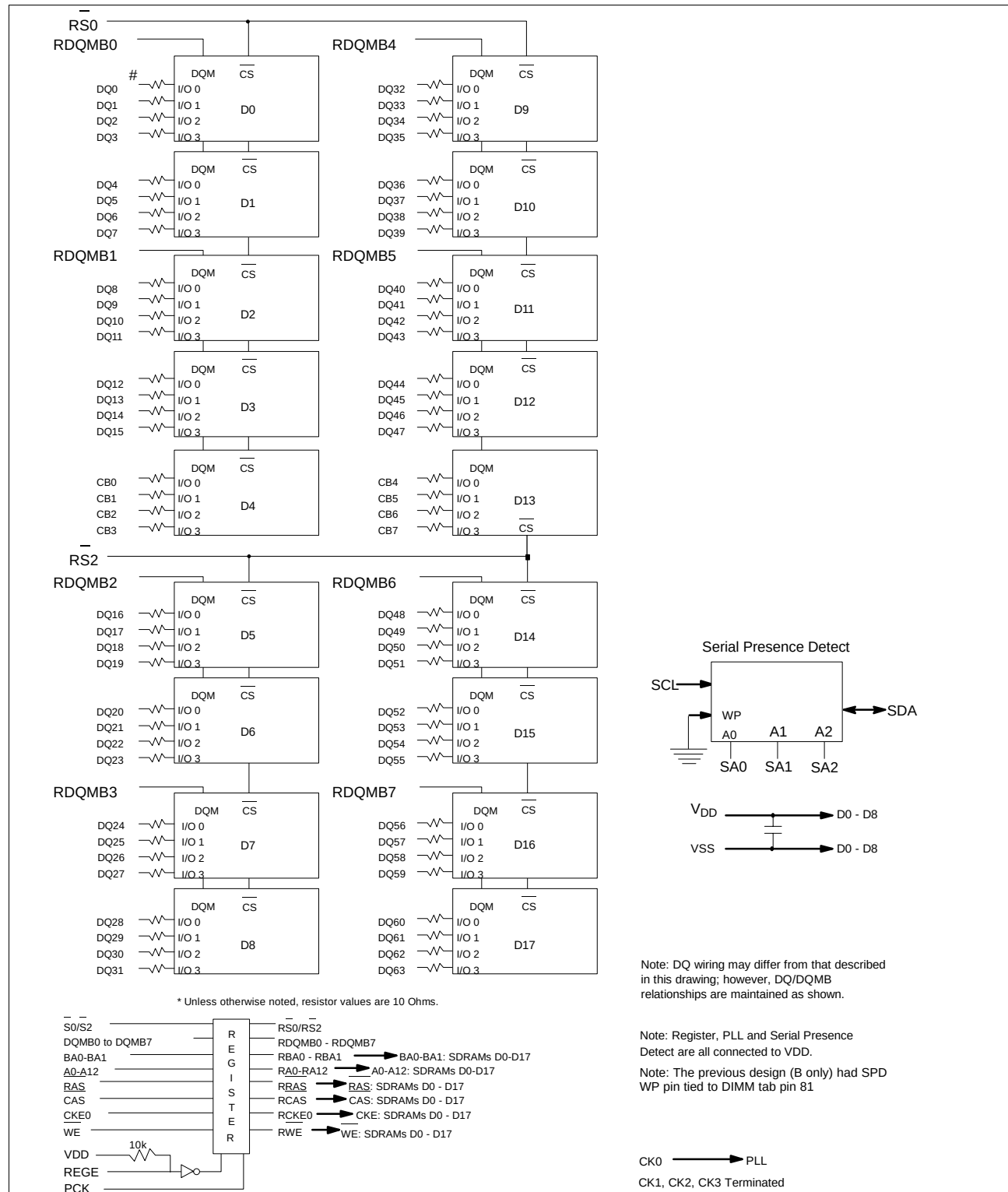
Block Diagram: Raw Card Version A

(Populated as 1 physical bank of x8 SDRAMs)



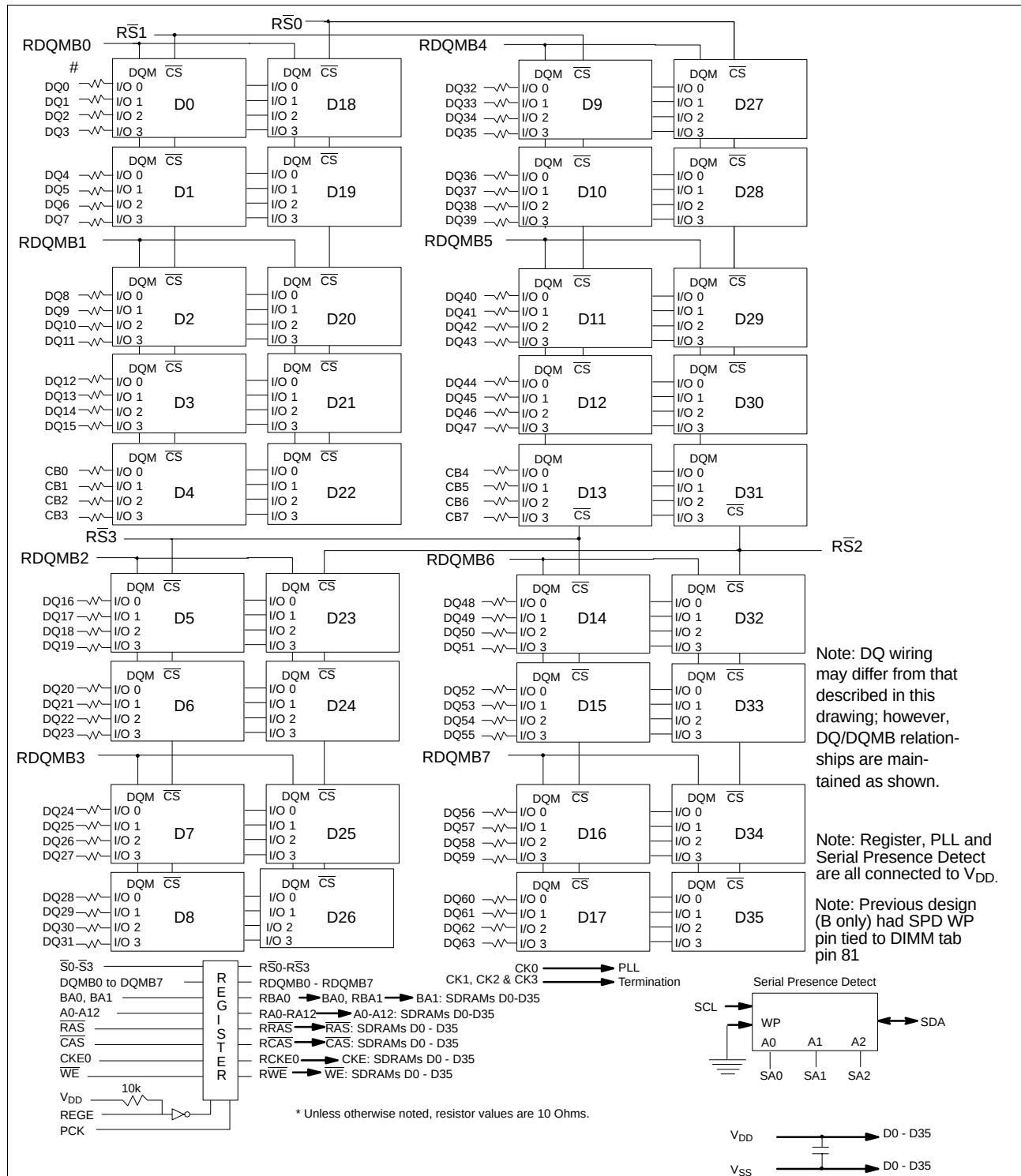
Block Diagram: Raw Card Version B & G

(Populated as 1 physical bank of x4 SDRAMs)



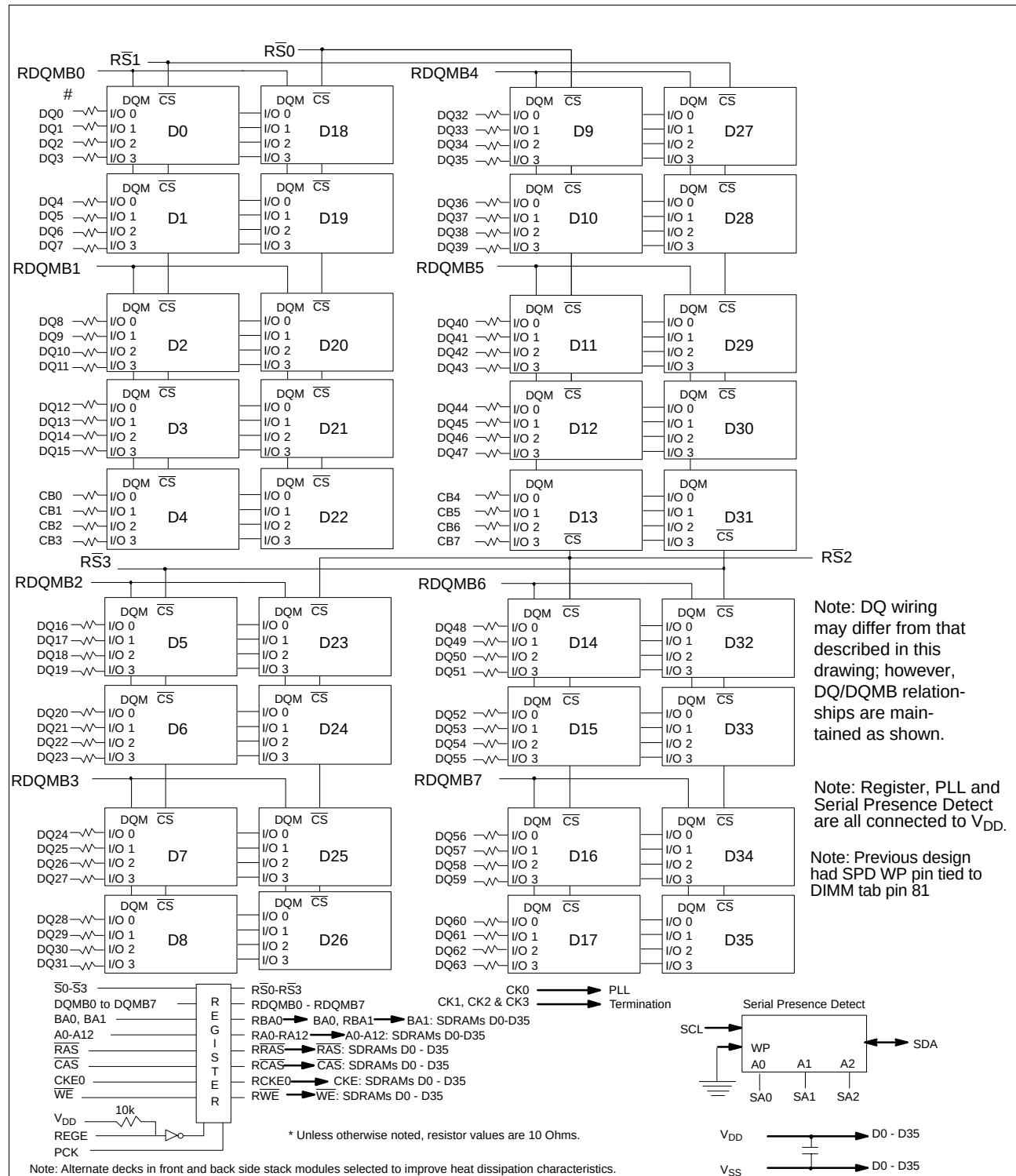
Block Diagram: Raw Card Version B & G

(Populated as 2 physical banks of x4 SDRAMs)



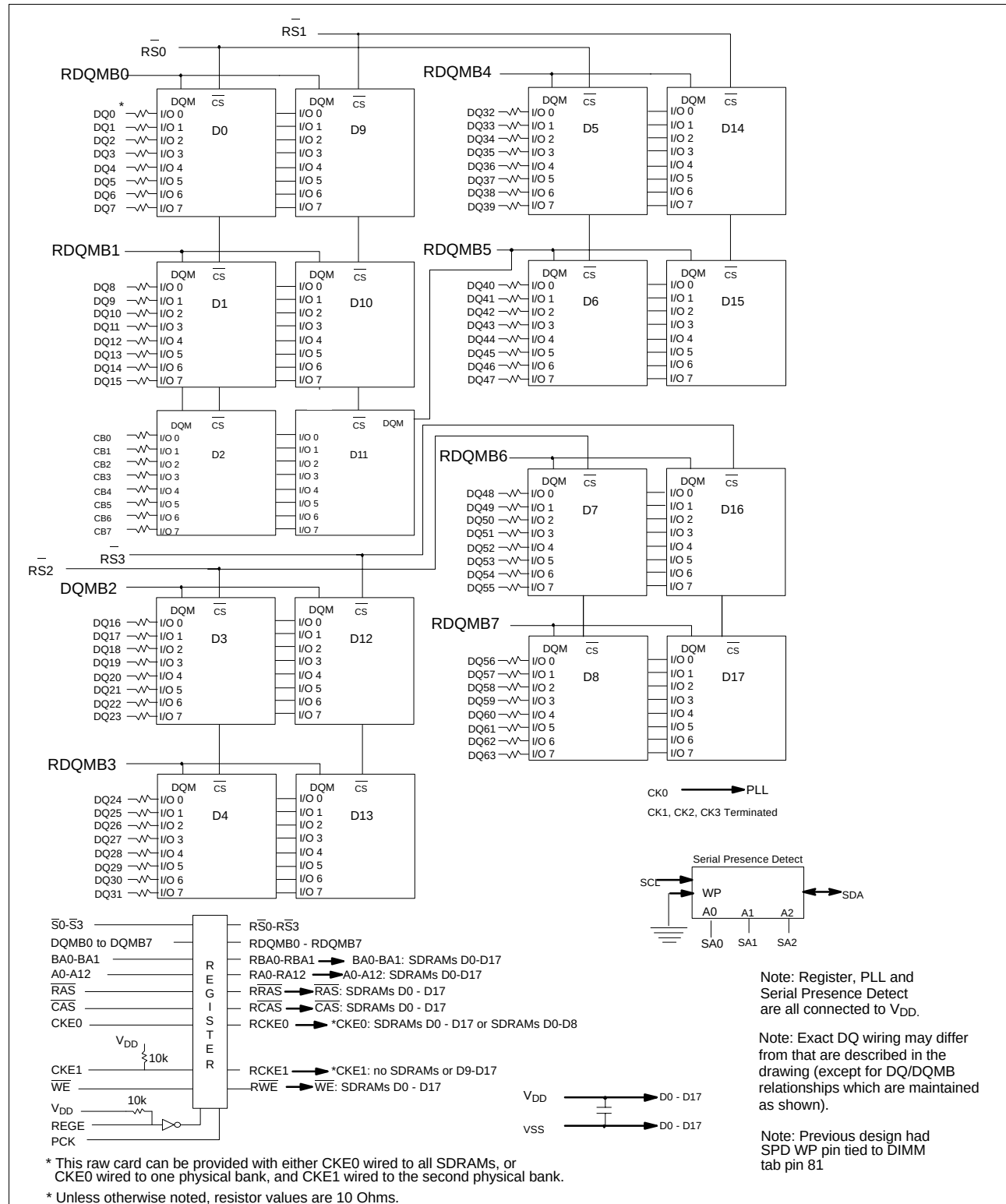
Block Diagram: Raw Card Versions C & D

(Populated as 2 physical banks of x4 SDRAMs)



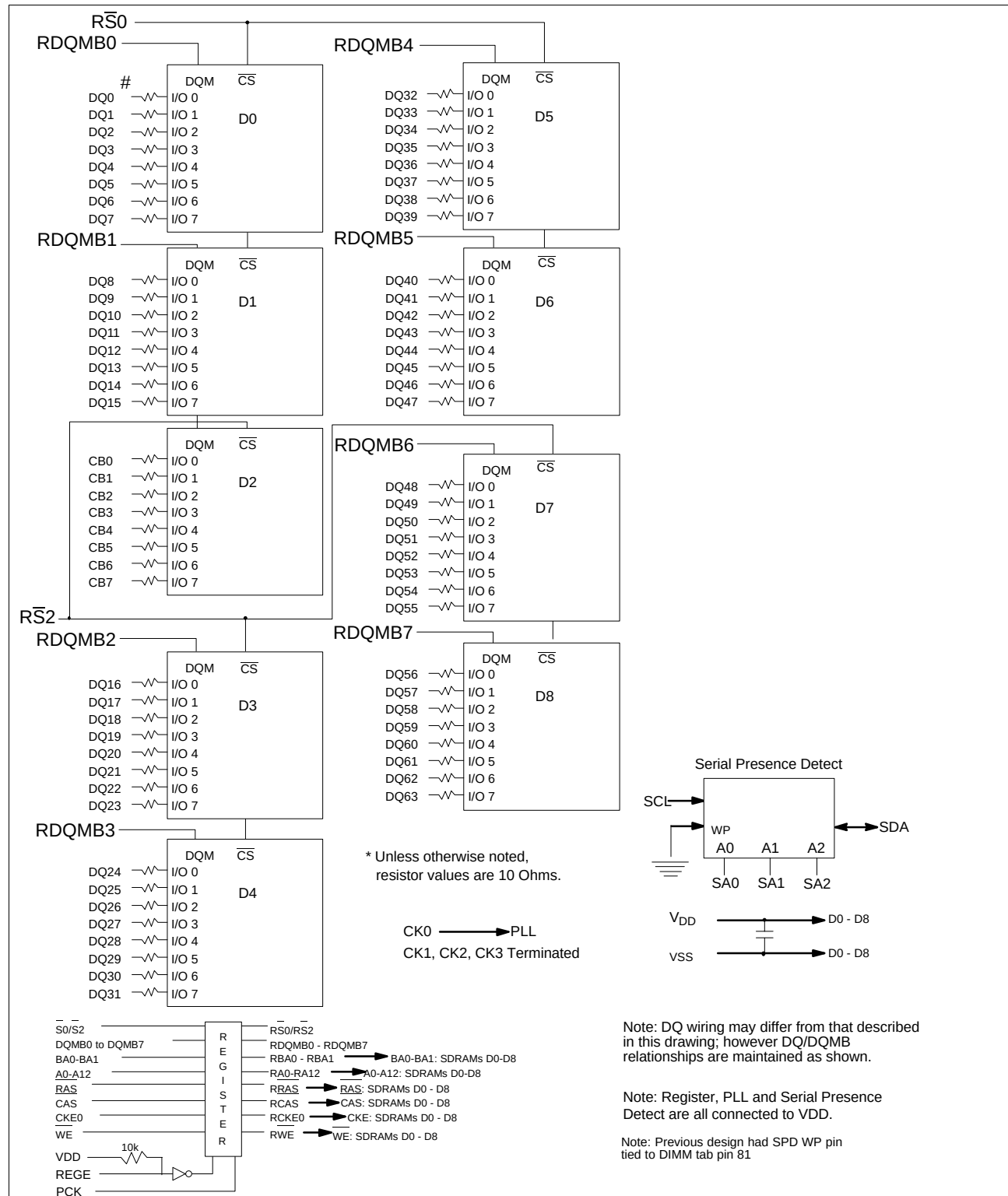
Block Diagram: Raw Card Versions E

(Populated as 2 physical banks of x8 SDRAMs)



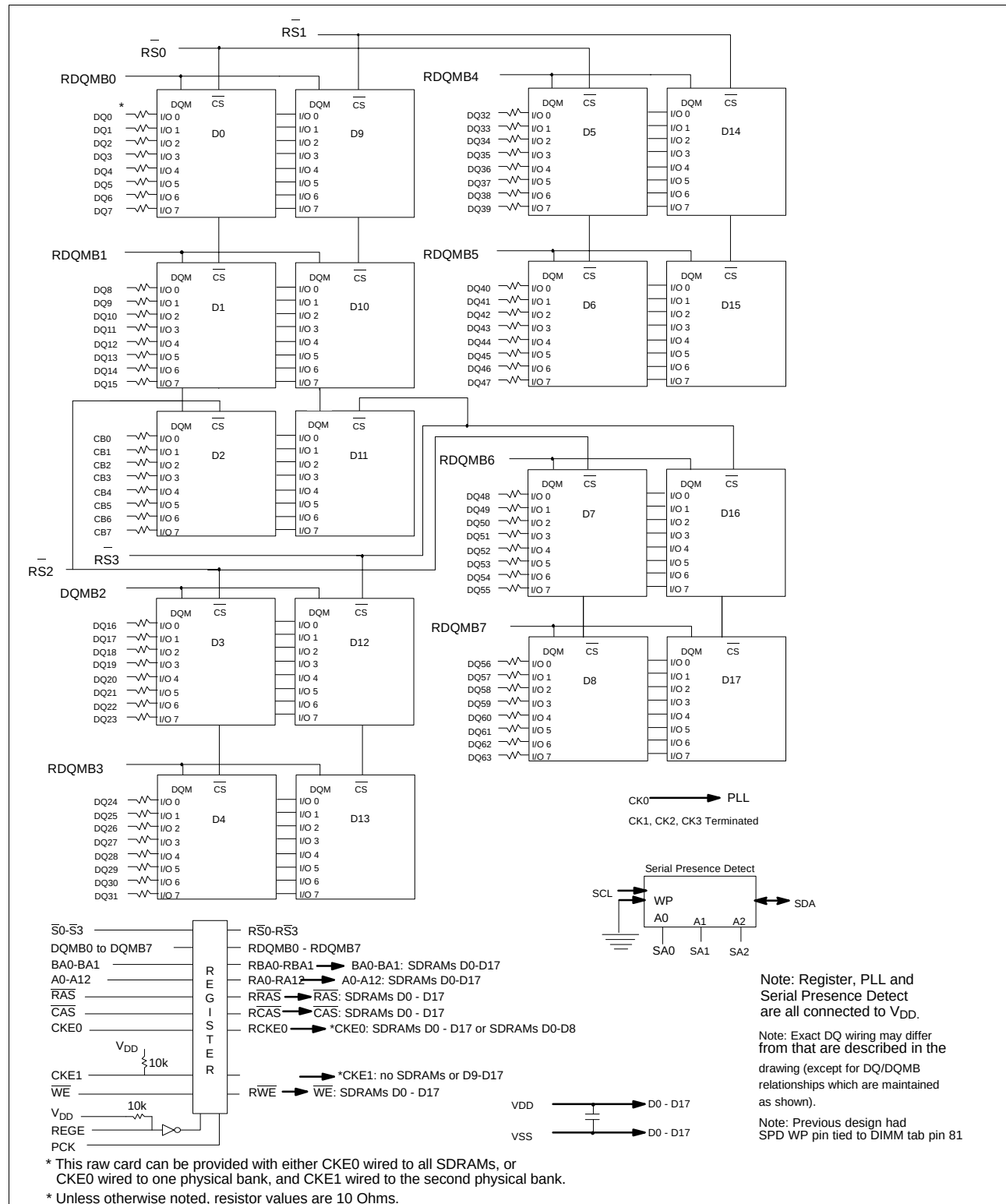
Block Diagram: Raw Card Version F

(Populated as 1 physical bank of x8 SDRAMs)

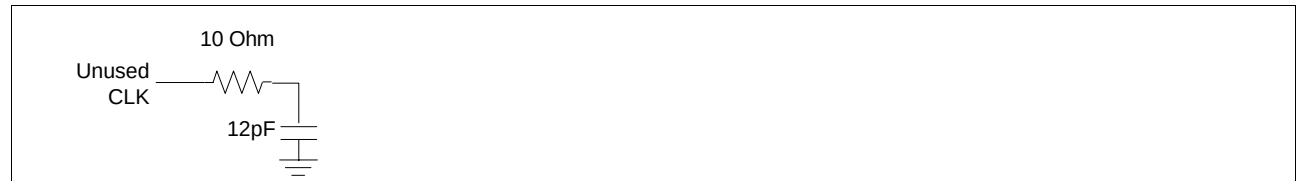


Block Diagram: Raw Card Version F

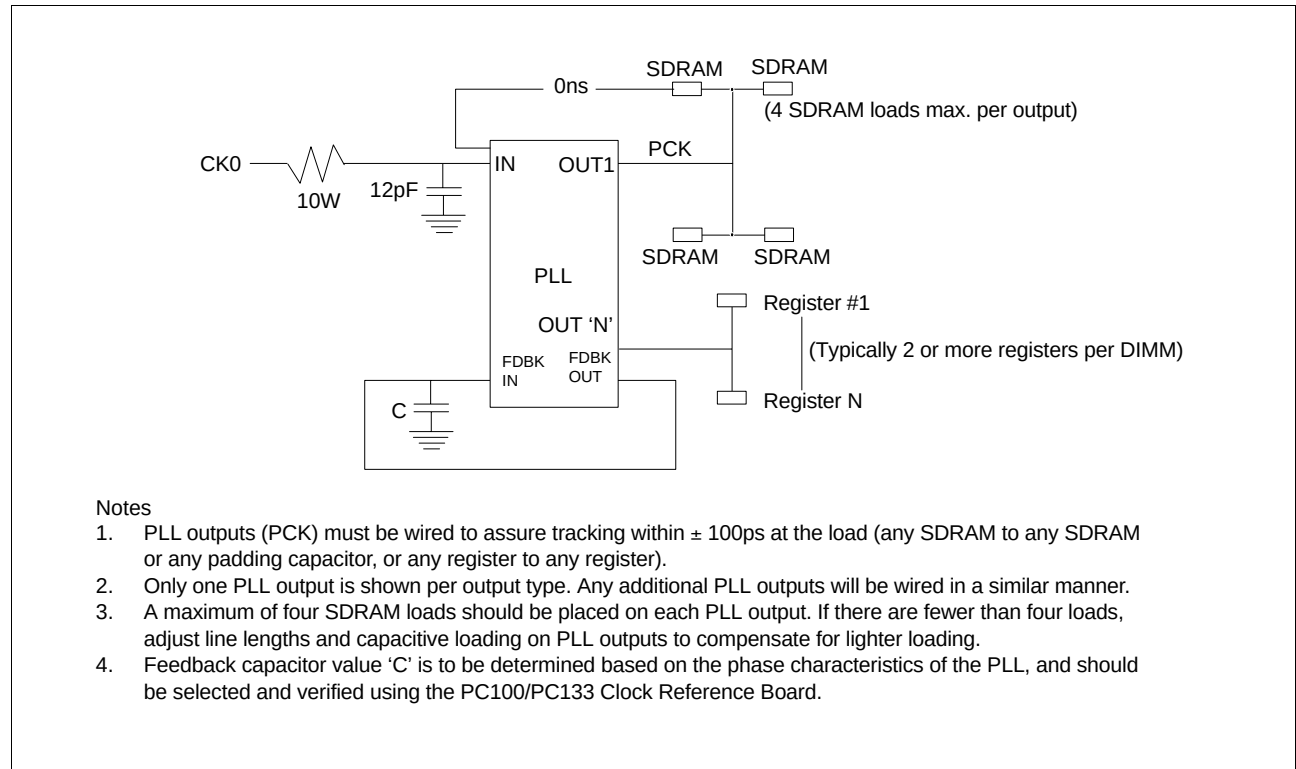
(Populated as 2 physical banks of x8 SDRAMs)



Termination for Unused Clock Signals (CK1-CK3)



Clock Net Wiring (CK0)



Register Functional Assignments

Raw Card Version A (Two Registers)				Raw Card Version F (Two Registers)				Raw Card Versions B, C, D and G (Three Registers)					
Register 1		Register 2		Register 1		Register 2		Register 1		Register 2		Register 3	
In	Out	In	Out	In	Out	In	Out	In	Out	In	Out	In	Out
A0	RA0	DQMB2	RDQMB2	A0	RA0	DQMB2	RDQMB2	A0	RA0A	A0	RA0B	DQMB0	RDQMB0
A1	RA1	DQMB3	RDQMB3	A1	RA1	DQMB3	RDQMB3	A1	RA1A	A1	RA1B	DQMB1	RDQMB1
A2	RA2	DQMB6	RDQMB6	A2	RA2	DQMB6	RDQMB6	A2	RA2A	A2	RA2B	DQMB2	RDQMB2
A3	RA3	DQMB7	RDQMB7	A3	RA3	DQMB7	RDQMB7	A3	RA3A	A3	RA3B	DQMB3	RDQMB3
A4	RA4	$\overline{S}2$	$\overline{R}S2$	A4	RA4	$\overline{S}2$	$\overline{R}S2$	A4	RA4A	A4	RA4B	DQMB4	RDQMB4
A5	RA5	CKE0	RCKE0	A5	RA5	CKE0	RCKE0	A5	RA5A	A5	RA5B	DQMB5	RDQMB5
A6	RA6	BA0	RBA0	A6	RA6	BA0	RBA0	A6	RA6A	A6	RA6B	DQMB6	RDQMB6
A7	RA7	BA1	RBA1	A7	RA7	BA1	RBA1	A7	RA7A	A7	RA7B	DQMB7	RDQMB7
A8	RA8	A10	RA10	S1	$\overline{R}S1$	A10	RA10	A8	RA8A	A8	RA8B	$\overline{S}0$	$\overline{R}S0$
A9	RA9	A11	RA11	A9	RA9	A11	RA11	A9	RA9A	A9	RA9B	$\overline{S}1$	$\overline{R}S1$
$\overline{S}0$	$\overline{R}S0$	A12 ¹	RA12	$\overline{S}0$	$\overline{R}S0$	A12 ¹	RA12	A10	RA10A	A10	RA10B	$\overline{S}2$	$\overline{R}S2$
DQMB0	RDQMB0			DQMB0	RDQMB0	A8	RA8	A11	RA11A	A11	RA11B	$\overline{S}3$	$\overline{R}S3$
DQMB1	RDQMB1			DQMB1	RDQMB1	S3	$\overline{R}S3$	BA0	RBA0A	BA0	RBA0B	WE	$\overline{R}WEA$
DQMB4	RDQMB4			DQMB4	RDQMB4	CKE1	RCKE1	BA1	RBA1A	BA1	RBA1B	WE	$\overline{R}WEB$
DQMB5	RDQMB5			DQMB5	RDQMB5			CAS	$\overline{R}CA\overline{S}A$	CAS	$\overline{R}CA\overline{S}B$	A12 ¹	RA12A
CAS	$\overline{R}CA\overline{S}$			CAS	$\overline{R}CA\overline{S}$			RAS	$\overline{R}RA\overline{S}A$	RAS	$\overline{R}RA\overline{S}B$	A12 ¹	RA12B
RAS	$\overline{R}RA\overline{S}$			RAS	$\overline{R}RA\overline{S}$			CKE0	CKE0A				
WE	$\overline{R}WE$			WE	$\overline{R}WE$			CKE0	CKE0B				

1. Only used with 256Mb and 512Mb SDRAMs.

Register Functional Assignments (continued)

Raw Card Version E (Three Registers)					
Register 1		Register 2		Register 3	
In	Out	In	Out	In	Out
A0	RA0A	A0	RA0B	DQMB0	RDQMB0
A1	RA1A	A1	RA1B	DQMB1	RDQMB1
A2	RA2A	A2	RA2B	DQMB2	RDQMB2
A3	RA3A	A3	RA3B	DQMB3	RDQMB3
A4	RA4A	A4	RA4B	DQMB4	RDQMB4
A5	RA5A	A5	RA5B	DQMB5	RDQMB5
A6	RA6A	A6	RA6B	DQMB6	RDQMB6
A7	RA7A	A7	RA7B	DQMB7	RDQMB7
A8	RA8A	A8	RA8B	S0	RS0
A9	RA9A	A9	RA9B	S1	RS1
A10	RA10A	A10	RA10B	S2	RS2
A11	RA11A	A11	RA11B	S3	RS3
BA0	RBA0A	BA0	RBA0B	WE	RWEA
BA1	RBA1A	BA1	RBA1B	$\overline{WE}$	RWEB
RAS	$\overline{RRASA}$	RAS	$\overline{RRASB}$	A12 ¹	RA12A
CAS	$\overline{RCASA}$	CAS	$\overline{RCASB}$	A12 ¹	RA12B
				CKE0	RCKE0
				CKE1 ²	RCKE1

- Only used with 256Mb and 512Mb SDRAMs.
- R/C E can be produced with either CKE0 wired to all SDRAMs (this pin would not be used) or CKE0 can be wired to one physical bank and CKE1 to the second physical bank.

Component Details

Pin Assignments for 64Mb and 128Mb SDRAM Planar Components

(Top View)

V _{DD}	V _{DD}	1	54	V _{SS}	V _{SS}
DQ0	NC	2	53	NC	DQ7
V _{DDQ}	V _{DDQ}	3	52	V _{SSQ}	V _{SSQ}
NC	NC	4	51	NC	NC
DQ1	DQ0	5	50	DQ3	DQ6
V _{SSQ}	V _{SSQ}	6	49	V _{DDQ}	V _{DDQ}
NC	NC	7	48	NC	NC
DQ2	NC	8	47	NC	DQ5
V _{DDQ}	V _{DDQ}	9	46	V _{SSQ}	V _{SSQ}
NC	NC	10	45	NC	NC
DQ3	DQ1	11	44	DQ2	DQ4
V _{SSQ}	V _{SSQ}	12	43	V _{DDQ}	V _{DDQ}
NC	NC	13	42	NC	NC
V _{DD}	V _{DD}	14	41	V _{SS}	V _{SS}
NC	NC	15	40	NC	NC
$\overline{WE}$	$\overline{WE}$	16	39	DQM	DQM
$\overline{CAS}$	$\overline{CAS}$	17	38	CK	CK
$\overline{RAS}$	$\overline{RAS}$	18	37	CKE	CKE
$\overline{CS}$	$\overline{CS}$	19	36	NC	NC
BA0	BA0	20	35	A11	A11
BA1	BA1	21	34	A9	A9
A10/AP	A10/AP	22	33	A8	A8
A0	A0	23	32	A7	A7
A1	A1	24	31	A6	A6
A2	A2	25	30	A5	A5
A3	A3	26	29	A4	A4
V _{DD}	V _{DD}	27	28	V _{SS}	V _{SS}

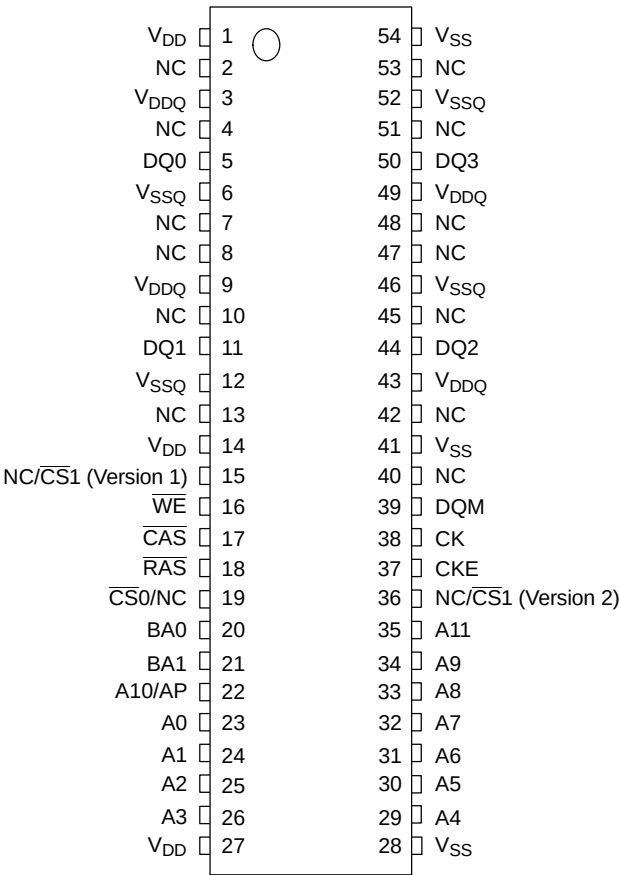
54-pin Plastic TSOP(II) 400 mil

4Mbit x 4 I/O x 4 Bank
8Mbit x 4 I/O x 4 Bank

2Mbit x 8 I/O x 4 Bank
4Mbit x 8 I/O x 4 Bank

Note: Raw Card Versions 'A' and 'B' support the use of the above SDRAM pin assignments.
These pin assignments are consistent with the JEDEC standard package definition.

Pin Assignments for 64Mb and 128Mb 54 pin SDRAM 2-High Stack Package
(Dual CS Pin)
(Top View)



54-pin Plastic TSOP(II) or TSOJ(II) 400 mil
(4Mbit x 4 I/O x 4 Bank) x 2 High
(8Mbit x 4 I/O x 4 Bank) x 2 High

Version 1: Consistent with Staktek™ 2-High stacked package. Raw Card Versions B and G support the use of this pin assignment.
Version 2: Consistent with IBM Microelectronics and JEDEC standard 2 High stacked package. Raw Card Version 'C' supports the use of this pin assignment.

* CS0 selects the lower DRAM in the stack.
* CS1 selects the upper DRAM in the stack.

Pin Assignments for 256Mb and 512Mb 54 pin SDRAM Planar Components (Top View)

V _{DD}	V _{DD}	1	54	V _{SS}	V _{SS}
DQ0	NC	2	53	NC	DQ7
V _{DDQ}	V _{DDQ}	3	52	V _{SSQ}	V _{SSQ}
NC	NC	4	51	NC	NC
DQ1	DQ0	5	50	DQ3	DQ6
V _{SSQ}	V _{SSQ}	6	49	V _{DDQ}	V _{DDQ}
NC	NC	7	48	NC	NC
DQ2	NC	8	47	NC	DQ5
V _{DDQ}	V _{DDQ}	9	46	V _{SSQ}	V _{SSQ}
NC	NC	10	45	NC	NC
DQ3	DQ1	11	44	DQ2	DQ4
V _{SSQ}	V _{SSQ}	12	43	V _{DDQ}	V _{DDQ}
NC	NC	13	42	NC	NC
V _{DD}	V _{DD}	14	41	V _{SS}	V _{SS}
NC	NC	15	40	NC	NC
WE	WE	16	39	DQM	DQM
CAS	CAS	17	38	CK	CK
RAS	RAS	18	37	CKE	CKE
CS	CS	19	36	A12	A12
BS0	BS0	20	35	A11	A11
BS1	BS1	21	34	A9	A9
A10/AP	A10/AP	22	33	A8	A8
A0	A0	23	32	A7	A7
A1	A1	24	31	A6	A6
A2	A2	25	30	A5	A5
A3	A3	26	29	A4	A4
V _{DD}	V _{DD}	27	28	V _{SS}	V _{SS}

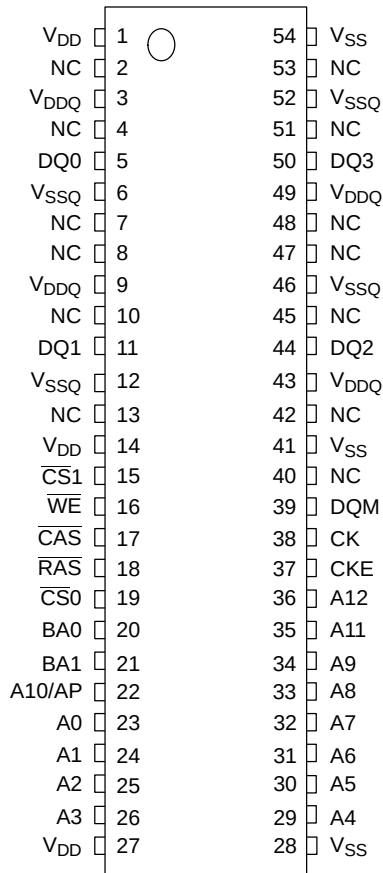
54-pin Plastic TSOP(II) 400mil

16Mbit x 4 I/O x 4 Bank
32Mbit x 4 I/O x 4 Bank

8Mbit x 8 I/O x 4 Bank
16Mbit x 8 I/O x 4 Bank

Note: Raw card versions B and G support use of the above SDRAM pin assignment. This assignment is consistent with the JEDEC standard package

Pin Assignments for 256Mb and 512Mb 54 pin SDRAM 2-High Stack Package
(Dual CS Pins)
(Top View)



54-pin Plastic TSOP(II) or TSOJ(II) 400 mil

(16Mbit x 4 I/O x 4 Bank) x 2-High
(32Mbit x 4 I/O x 4 Bank) x 2-High

Note: Raw Card Versions B and G support the use of the above SDRAM pin assignment. This pin assignment is consistent with the Staktek™ 2 High stacked package.

- * $\overline{\text{CS}}0$ selects the lower DRAM in the stack.
- * $\overline{\text{CS}}1$ selects the upper DRAM in the stack.

Pin Assignments for 512Mb 54 pin SDRAM 2-High Stack Package (Dual CS Pins, Dual CKE Pins)

(Top View)

V _{DD}	1	54	V _{SS}
DQ0	2	53	DQ7
V _{DDQ}	3	52	V _{SSQ}
NC	4	51	NC
DQ	5	50	DQ6
V _{SSQ}	6	49	V _{DDQ}
NC	7	48	NC
DQ2	8	47	DQ5
V _{DDQ}	9	46	V _{SSQ}
NC	10	45	NC
DQ3	11	44	DQ4
V _{SSQ}	12	43	V _{DDQ}
NC	13	42	NC
V _{DD}	14	41	V _{SS}
$\overline{\text{CS}}1$	15	40	CKE1
$\overline{\text{WE}}$	16	39	DQM
$\overline{\text{CAS}}$	17	38	CK
$\overline{\text{RAS}}$	18	37	CKE0
$\overline{\text{CS}}0$	19	36	A12
BA0	20	35	A11
BA1	21	34	A9
A10/AP	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
V _{DD}	27	28	V _{SS}

54-pin Plastic TSOP(II)

(8Mbit x 8 I/O x 4 Bank) x 2-High

Note: Raw Card Version 'F' supports the use of the above SDRAM pin assignment. This pin assignment is consistent with the Staktek™ 2-High stacked package.

- * $\overline{\text{CS}}0$ selects the lower DRAM in the stack.
- * $\overline{\text{CS}}1$ selects the upper DRAM in the stack.