4.20.20- 240-Pin DDR3 SDRAM Registered DIMM Design Specification

PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900 /PC3-17000 DDR3 SDRAM Registered DIMM Design Specification

Revision 0.91

February 2012

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Contents

1. Product Description **4**
Product Family Attributes 4

2. Environmental Requirements **5**

3. Pinout and Description **6**
Pin Description 6
Input/Output Functional Description 7
DDR3 240-pin DIMM Pinout 9
Pinout Comparison 10

4. Component Details **11**
Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM 12
PCB Pad Array Options for SDRAM Placements 16
Pin Assignments for Registering Clock Driver 22
Critical Registering Clock Driver Specifications (Reference Only) 23
Pin Assignments for Serial Presence Detect 25

5. DDR3 Registered DIMM Wiring Details **26**
Signal Groups 26
General Net Structure Routing Guidelines 26
Test Point 28
Explanation of Net Structure Diagrams 29

6. Timing Budget **30**
Example of DDR3 Timing Budget 31

7. On DIMM Thermal Sensor **32**

8. Register Clock Driver (RCD) Feedback Topology **33**

9. Serial Presence Detect Definition **34**

10. DDR3 DIMM Label Format **37**

11. DIMM Mechanical Specifications **39**

12. Design File Naming Convention **40**

Annex A – Raw Card A **A1**

Annex B – Raw Card B **B1**

Annex C – Raw Card C **C1**

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Annex D – Raw Card D..... D1

Annex E – Raw Card E..... .... E1

Annex F– Raw Card F..... F1

Annex G – Raw Card G..... G1

Annex H – Raw Card H..... H1

Annex J – Raw Card J J1

Annex K – Raw Card K..... K1

Annex L – Raw Card L..... L1

Annex M – Raw Card M..... M1

Annex N – Raw Card N..... N1

Annex V – Raw Card V..... V1

Annex W – Raw Card W..... W1

Annex Y – Raw Card Y..... Y1

Annex AB – Raw Card AB..... AB1

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

PC3 refers to DIMMs designed to operate at 1.5V nominal. PC3L refers to DIMMs with components that can support 1.35V nominal. PC3U refers to DIMMs with components that can support 1.25V nominal.

PC3(L,U)-6400, PC3(L,U)-8500, PC3(L,U)-10600, PC3(L,U)-12800, PC3-14900, PC3-17000 refers to the JEDEC standard DIMM naming convention in which PC3(L,U)-6400, PC3(L,U)-8500, PC3(L,U)-10600, PC(L,U)-12800, PC3-14900 and PC3-17000 indicates a DIMM running at 400, 533, 667, 800, 931 and 1063 MHz clock speed and offering 6400, 8500, 10600, 12800, 14900 and 17000 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC3(L,U)-6400, PC3(L,U)-8500, PC3(L,U)-10600, PC3(L,U)-12800, PC3-14900 and PC3-17000 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

DDR3 and DDR3L and DDR3U (PC3 and PC3L and PC3U) have different requirements. Many of the initial designs were only simulated and tested based on 1.5V requirements. Speed grades and voltages for each reference design are defined in each appendix. DDR3 refers to 1.5V operation only. For the design to be 1.35V capable the appendix must specifically include DDR3L. For the design to be 1.25V capable the appendix must specifically include DDR3U.

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.0 mm x 133.35 mm x 4.00 mm / MO-269, Variation AB 30.0 mm x 133.35 mm x 6.75 mm / MO-269, Variation BB 30.0 mm x 133.35 mm x 7.55 mm / MO-269, Variation CB 18.75 mm x 133.35 mm x 4.00 mm / MO-269, Variation DB 18.75 mm x 133.35 mm x 6.75 mm / MO-269, Variation EB 18.75 mm x 133.35 mm x 7.55 mm / MO-269, Variation FB
Pin count	240
SDRAMs supported	512 Mb, 1 Gb, 2 Gb, 4 Gb, 8Gb
Capacity	512 MB, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, 32 GB
Serial PD	Consistent with JC 45
Voltage options	1.25 volts or 1.35 volts or 1.5 volts (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.25 volt or 1.35 volt or 1.5 volt signal switching based on reference voltage at VDD/2. See DRAM specification for more detail.

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Environmental Requirements

DDR3 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Pinout and Description

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
CK0_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CK1_t	Clock Input, positive line	1	CB[7:0]	Data check bits Input/Output	8
CK1_c	Clock Input, negative line	1	DQS[8:0]_t	Data strobes	9
CKE[1:0]	Clock Enables	2	DQS[8:0]_c	Data strobes, negative line	9
RAS_n	Row Address Strobe	1	DM[8:0]/ DQS[17:9]_t, TDQS[17:9]_t	Data Masks / Data strobes, Termination data strobes	9
CAS_n	Column Address Strobe	1	DQS[17:9]_c TDQS[17:9]_c	Data strobes, negative line, Termination data strobes	9
WE_n	Write Enable	1	EVENT_n	Reserved for optional hardware temperature sensing	1
S_n[3:0]	Chip Selects	4	TEST	Memory bus test tool (Not Connected and Not Usable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	RESET_n	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V_{DD}	Power Supply	22
A12/BC_n	Address Input/Burst chop	1	V_{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V_{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V_{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V_{DDSPD}	SPD Power	1
Par_In	Parity bit for the Address and Control bus	1			
Err_Out_n	Parity error found on the Address and Control bus	1			

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
CK0_c	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1_t	IN	Positive Line	Terminated but not used on RDIMMs.
CK1_c	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2]_n operate similarly to S[1:0]_n for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V_{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V_{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[15:13, 12/BC_n,11, 10/AP,[9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for ''BL on the fly'' during CAS_n command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V_{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[17:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Registered DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
TDQS[17:9]_t TDQS[17:9]_c	OUT		TDQS_t/TDQS_c is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1,DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11=0 in MR1, DM/TDQS_t will provide the data mask function and TDQS_c is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part. No pull-up resister is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN		The RESET_n pin is connected to the RESET_n pin on the register and to the RESET_n pin on the DRAM.
Par_In	IN		Parity bit for the Address and Command bus. (“1 “: Odd, “0 “: Even)
Err_Out_n	OUT (open drain)		Parity error detected on the Address and-Command bus. A resistor may be connected from Err_Out_n bus line to V_{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

DDR3 240-pin RDIMM and UDIMM Pinout

Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{REFDQ}	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DM3, DQS12_t, TDQS12_t	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC,DQS12_c, TDQS12_c	63	NC, CK1_t	183	V_{DD}	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	V_{SS}	34	DQS3_t	154	V_{SS}	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	V_{SS}
5	V_{SS}	125	DM0,DQS9_t, TDQS9_t	35	V_{SS}	155	DQ30	65	V_{DD}	185	CK0_c	95	V_{SS}	215	DQ46
6	DQS0_c	126	NC,DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	V_{DD}	186	V_{DD}	96	DQ42	216	DQ47
7	DQS0_t	127	V_{SS}	37	DQ27	157	V_{SS}	67	V_{REFCA}	187	EVENT_n, NC	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4,NC	68	Par_In, NC	188	A0	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V_{DD}	189	V_{DD}	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1,NC	160	V_{SS}	70	A10 / AP	190	BA1	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	NC, DM8, DQS17_t, TDQS17_t,	71	BA0	191	V_{DD}	101	V_{SS}	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC,DQS17_c, TDQS17_c	72	V_{DD}	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	V_{SS}	43	DQS8_t	163	V_{SS}	73	WE_n	193	S0_n	103	DQS6_t	223	V_{SS}
14	V_{SS}	134	DM1, DQS10_t, TDQS10_t	44	V_{SS}	164	CB6,NC	74	CAS_n	194	V_{DD}	104	V_{SS}	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2,NC	165	CB7,NC	75	V_{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	V_{SS}	46	CB3,NC	166	V_{SS}	76	S1_n, NC	196	A13	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC(TEST)	77	ODT1, NC	197	V_{DD}	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	V_{DD}	198	S3_n, NC	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}	KEY				79	S2_n, NC	199	V_{SS}	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	49	VTT, NC	169	CKE1, NC	80	V_{SS}	200	DQ36	110	V_{SS}	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	V_{DD}	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	V_{SS}	51	V_{DD}	171	A15	82	DQ33	202	V_{SS}	112	DQS7_t	232	V_{SS}
23	V_{SS}	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V_{SS}	203	DM4, DQS13_t, TDQS13_t	113	V_{SS}	233	DQ62
24	DQS2_c	144	NC, DQS11_c TDQS11_c,	53	Err_Out_n NC	173	V_{DD}	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V_{SS}	54	V_{DD}	174	A12 / BC_n	85	DQS4_t	205	V_{SS}	115	DQ59	235	V_{SS}
26	V_{SS}	146	DQ22	55	A11	175	A9	86	V_{SS}	206	DQ38	116	V_{SS}	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	V_{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V_{SS}	57	V_{DD}	177	A8	88	DQ35	208	V_{SS}	118	SCL	238	SDA
29	V_{SS}	149	DQ28	58	A5	178	A6	89	V_{SS}	209	DQ44	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	V_{TT}	240	V_{TT}
				60	V_{DD}	180	A3								

See Notes on following page for differences of RDIMMs and UDIMMs

Documents Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Pinout Comparison Based on Module Type

Pin #	RDIMM		UDIMM	
	Signal	Notes	Signal	Notes
48, 49	VTT	Additional connection for Termination Voltage for Address/Command/Control/Clock nets.	NC	Not used on UDIMMs
120, 240	VTT	Termination Voltage for Address/Command/Control/Clock nets.	VTT	Termination Voltage for Address/Command/Control/Clock nets.
53	Err_Out_n	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
63	CK1_t	CK1_t and CK1_c are terminated but not used on RDIMMs	CK1_t	Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated
64	CK1_c		CK1_c	
68	Par_In	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
76	S1_n	Connected to the register on all RDIMMs	S1_n	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs
77	ODT1, NC	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs
79	S2_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs	NC	Not used on UDIMMs
167	NC	TEST input used only on bus analysis probes	NC	TEST input used only on bus analysis probes
169	CKE1	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	CKE1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs
171	A15	Connected to the register on all RDIMMs	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs
172	A14		A14	
196	A13		A13	
198	S3_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single-or dual-rank RDIMMs	NC	Not used on UDIMMs
39, 40, 45, 46, 158, 159, 164, 165	CBn	Used on all RDIMMs; (n = 0...7)	NC, CBn	Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs
125, 134, 143, 152, 161, 203, 212, 221, 230	DQSn_t, TDQSn_t	Connected to DQS_t on x4 SDRAMs, TDQS_t on x8 SDRAMs on RDIMMs; (n = 9...17)	DMn	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8)
126, 135, 144, 153, 162, 204, 213, 222, 231	DQSn_c, TDQSn_c	Connected to DQS_c on x4 DRAMs, TDQS_c on x8 SDRAMs on RDIMMs; (n=9...17)	NC	Not used on UDIMMs
187	EVENT_n NC	Connected to optional thermal sensing component. NC on Modules without a thermal sensing component.	EVENT_n NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.
NC = no internal connection				

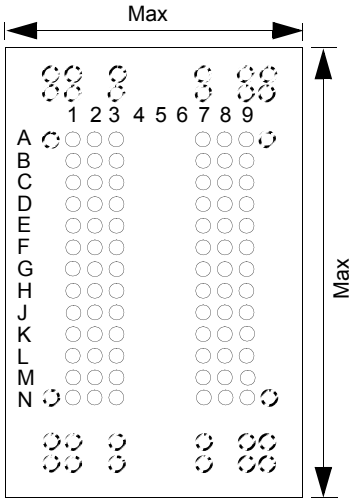
Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

Component Details

Supported SDRAM Components Maximum size for 512Mb to 8Gb; DDR3 SDRAM
This table is for reference only. Please see appropriate raw card appendix for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Package Type	MO-207 variation	# of DRAM balls supported
A	12.5 mm x 21.0 mm	Planar	DW-z	106
B	12.0 mm x 21.0 mm	Planar	DW-z	106
C	11.9 mm x 21.0 mm	Planar	DW-z	106
D	12.4 mm x 21.0 mm	Stacked	DW-z	106
E	8.5 mm x 13.0 mm ... 10.0 mm x 11.5 mm[1]	Planar	DW-z	82
F	9.0 mm x 13.0 mm ... 10.0 mm x 11.5 mm[1]	Stacked	DT-z	78
G	11.0 mm x 19.0 mm ... 11.9 x 19.0 mm[1]	Stacked	DW-z	106
H	10.0 mm x 13.0 mm	Planar	DT-z	78
J	10.2 mm x 11.5 mm	Planar	DT-z	78
K	21.1 mm x 18.05 mm	Planar	DW-z	106
L	11.0 mm x 13.0 mm	Planar	DW-z	82
M	11.0 mm x 13.0 mm	Planar	DW-z	82
N	11.0 mm x 13.0 mm	Stacked	DW-z	82
V	11.0 mm x 13.0 mm	Stacked	DW-z	82
W	10.5 mm x 11.5 mm	Stacked	DT-z	78
Y	10.0 mm x 11.5 mm	Planar	DT-z	78
AB	11.0 mm x 11.5 mm	Stacked	DT-z	78

Note: 1. SDRAM width depends on placement of de-coupling capacitors between SDRAMs.



Documents
Document Sharing Hub
Full document details: JEDEC MODULE4.20.20 2012

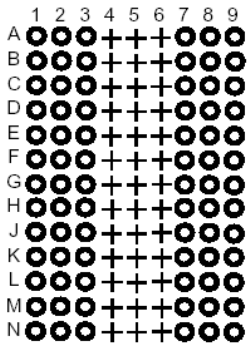
Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs (Top view)

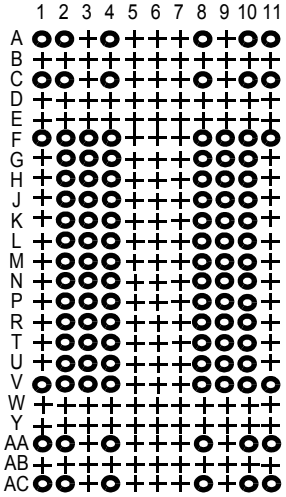
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



Populated ball
Ball not populated

MO-207 Variation DW-z
with support balls



Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 17).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

Documents
Document Sharing Hub

Full document details: JEDEC MODULE4.20.20 2012