

Annex D - Raw Card D

DDR3 Registered Dimm Design File

Applicable Design File	Applicable BOM
PC3-8500-RDIMM-V0_30_RC_D_REV0_71_20080331.brd	PC3-8500-RDIMM-V0_30_RC_D_REV0_7_20080331-BOM.xls
Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.	

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
2GB	256M x 72	512Mbit	128M x 4	36	2	13/11/3	AB/BB
4GB	512M x 72	1Gbit	256M x 4	36	2	14/11/3	AB/BB
8GB	1G x 72	2Gbit	512M x 4	36	2	15/11/3	AB/BB
16GB	2G x 72	4Gbit	1G x 4	36	2	16/11/3	AB/BB
32GB	4G x 72	8Gbit	2G x 4	36	2	16/12/3	AB/BB
Note: Some heat spreaders may not be covered within these variations.							

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
12.4 x 21.0 mm	8	106 Ball stacked FBGA	stacked, single row	DW-z
Note1: DRAM body center to DRAM body center is 12.8 mm				
Note2: DRAM width limited to 10.9 mm if passive placements between DRAMs is required.				

Supported Speeds

PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
X	X			

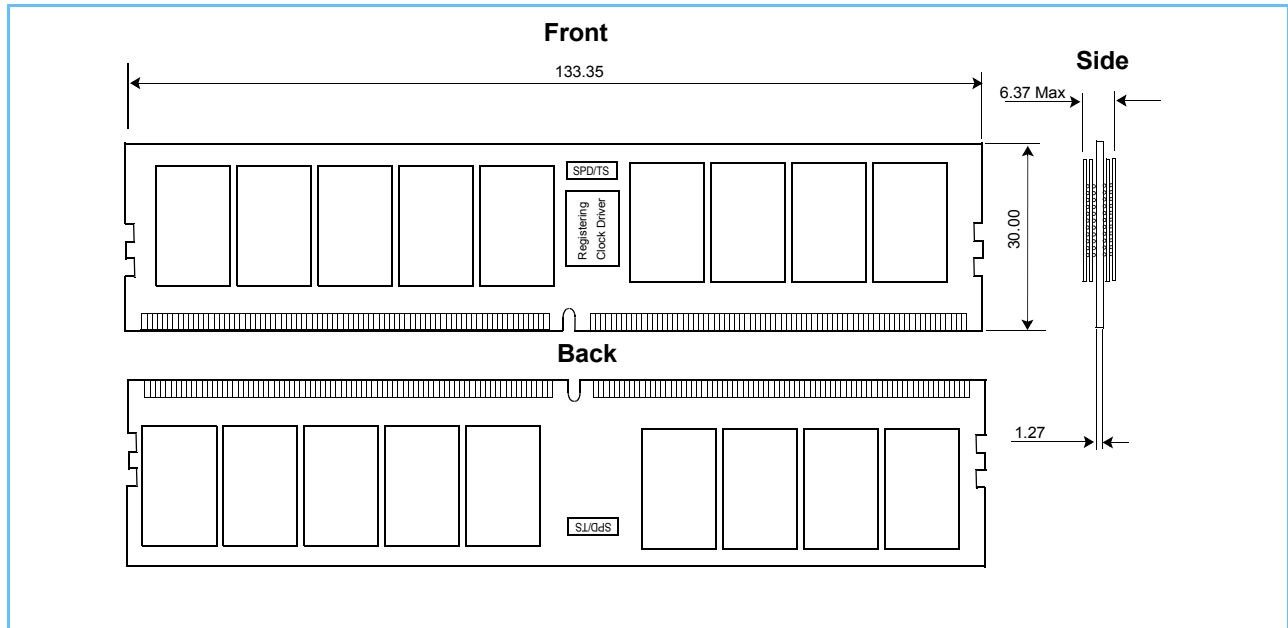
Note: X will reflect passed committee ballot at the time when specification is issued at BOD ballot

Design Rules and Deviations

This card uses 0.076 mm traces on internal layers with a nominal impedance of 56Ω.
This card uses blind vias.

General Layout

x72 DIMM, populated as two physical ranks of stacked x4 DDR3 SDRAMs



Note 1: All dimension are typical unless otherwise stated. (Millimeters)

Note 2: Thermal sensor is placed within the Thermal Sensor Placement Area as defined in MO-269.

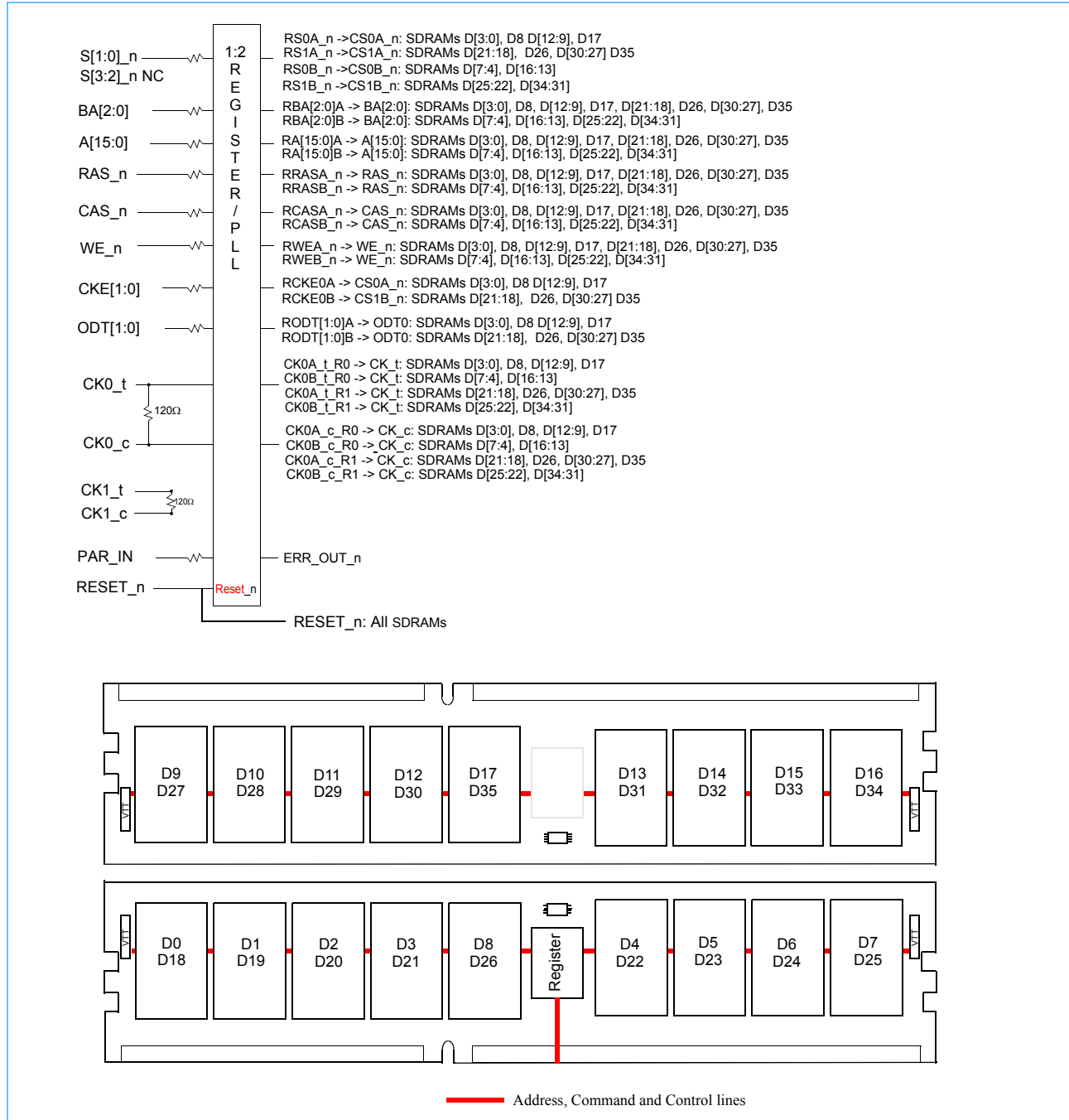
Note 3: Registering clock driver is placed within the Register Placement Area as defined in MO-269

Note 4: Implementation and dimensions shown without heat spreader.

Note 5: In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heat spreader attached.

Block Diagram

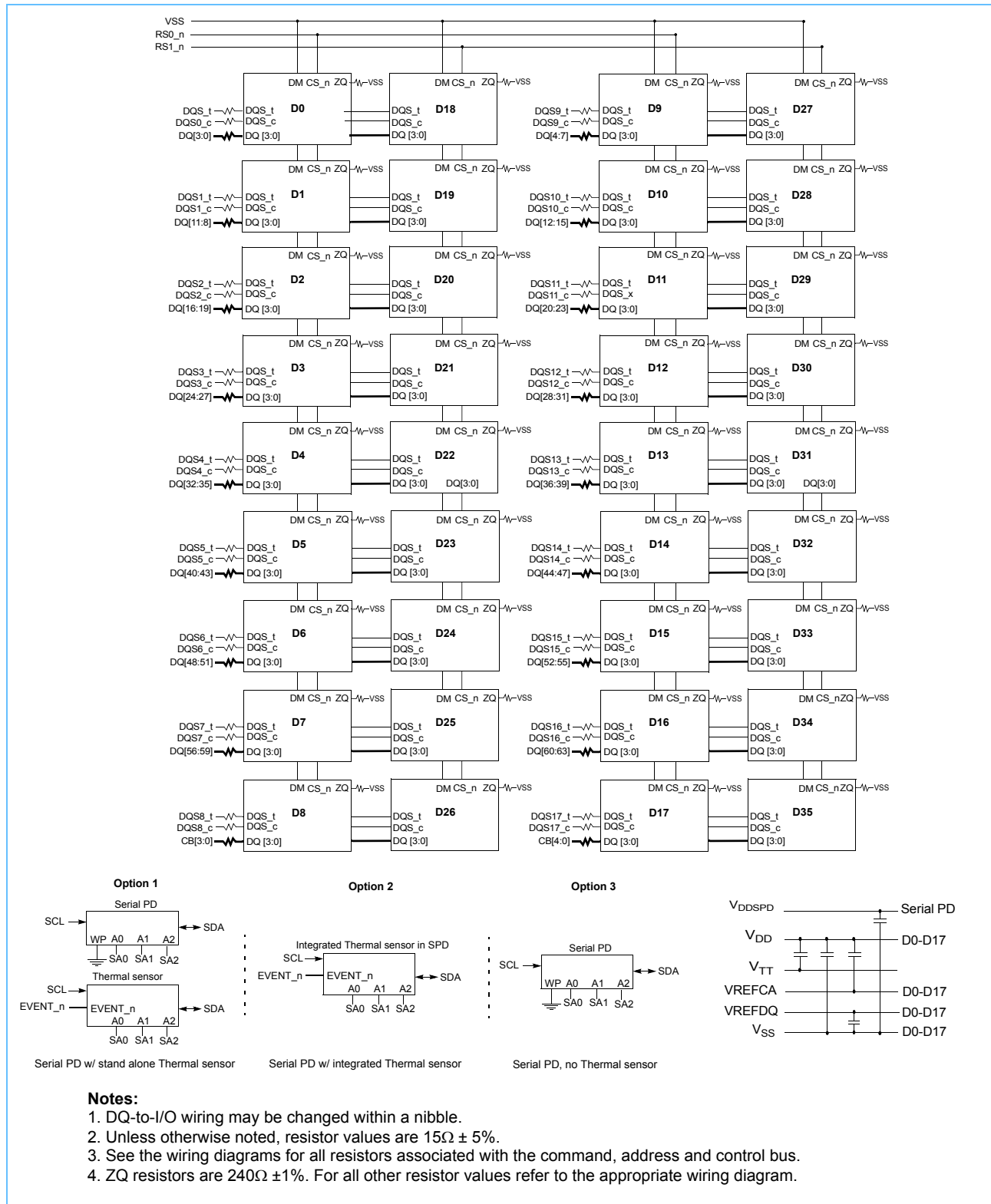
x72 DIMM, populated as two physical ranks of stacked x4 DDR3 SDRAMs (Part 1 of 2)



1. CK0_t, CK0_c terminated with $120\Omega \pm 5\%$ resistor.
2. CK1_t, CK1_c terminated with $120\Omega \pm 5\%$ resistor, but not connected to any DRAM.
3. All resistors are 22Ω unless otherwise stated.

Functional Block Diagram

x72 DIMM, populated as two physical ranks of stacked x4 DDR3 SDRAMs (Part 2 of 2)



Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specifications

DRAMs per output	Register Type	Register Speed Grade PC3-6400	Register Speed Grade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
20 / 16	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

Register Control Bit Settings

Types of Control Bits

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only.

They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match-module implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.

Register Control Word Setting for Raw Card D

Register Control Word	Bit	Function	Type	Register Settings
RC0	DBA1	B outputs disabled	Card	0
	DBA0	A outputs disabled	Card	0
	DA4	Float outputs	A/S	0 or 1
	DA3	Output Inversion	Card	0
RC1	DBA1	Disable Y3_t/Y3_c clock	Card	0
	DBA0	Disable Y2_t/Y2_c clock	Card	0
	DA4	Disable Y1_t/Y1_c clock	Card	0
	DA3	Disable Y0_t/Y0_c clock	Card	0
RC2	DBA1	Frequency Band Select	Test	0
	DBA0	Input Bus Termination	A/S	0 or 1
	DA4	1T/3T Output timing	A/S	0 or 1
	DA3	Address- and command-nets prelaunch (Control Signals QxCKE, QxCS, QxODT do not apply)	Card	0
RC3	DBA1	Driver Characteristics: Command/Address Driver-B Outputs	Card	1
	DBA0		Card	0
	DA4	Driver Characteristics: Command/Address Driver-A Outputs	Card	1
	DA3		Card	0
RC4	DBA1	Driver Characteristics: Control Driver-B Outputs	Card	1
	DBA0		Card	0
	DA4	Driver Characteristics: Control Driver-A Outputs	Card	1
	DA3		Card	0
RC5	DBA1	Driver Characteristics: Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers	Card	1
	DBA0		Card	0
	DA4	Driver Characteristics: Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers	Card	1
	DA3		Card	0
RC6	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0