

Annex E - Raw Card E

DDR3 Registered Dimm Design File

RC	Applicable Design File	Applicable BOM
E0	PC3-RDIMM_RC_E0_REV051_20071002.brd	PC3-RDIMM_RC_E0_REV051_20071002_BOM.pdf
E1	PC3-RDIMM_RC_E1_REV070_20080721.brd	PC3-RDIMM_RC_E1_REV070_20080721_BOM.pdf
E2	PC3-RDIMM_V089_RC_E2_20101217.brd	PC3-RDIMM_V089_RC_E2_20101217_BOM.pdf

NOTE "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
2GB	128Mx72	512Mbit	128Mx4	36	2	13/11/3	AB*
4GB	256Mx72	1Gbit	256Mx4	36	2	14/11/3	AB*
8GB	512Mx72	2Gbit	512Mx4	36	2	15/11/3	AB*
16GB	1Gx72	4Gbit	1Gx4	36	2	16/11/3	AB*
32GB	2Gx72	8Gbit	2Gx4	36	2	16/12/3	AB*

NOTE *without heatspreader; variations with heatspreader are TBD

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
8.5 x 13.0 ... 10.0 x 11.5 *	8	106 Ball FBGA	x4 planar, double row	DW-z

NOTE *with (Width + Length < 21.5 mm), depending on placement of de-coupling capacitors between SDRAMs

Supported Speeds

Registration	Voltage	PC3-6400	PC3-8500	PC3-10600	PC3-12800	PC3-14900	PC3-17000	Notes
E0	DDR3	X	X	X				1,2
	DDR3L							1,2
E1	DDR3	X	X	X	X			1,2
	DDR3L	X	X	X	X			1,2
E2	DDR3	X	X	X	X	X		1,2
	DDR3L	X	X	X	X			1,2
	DDR3U	X	X	X				1,2

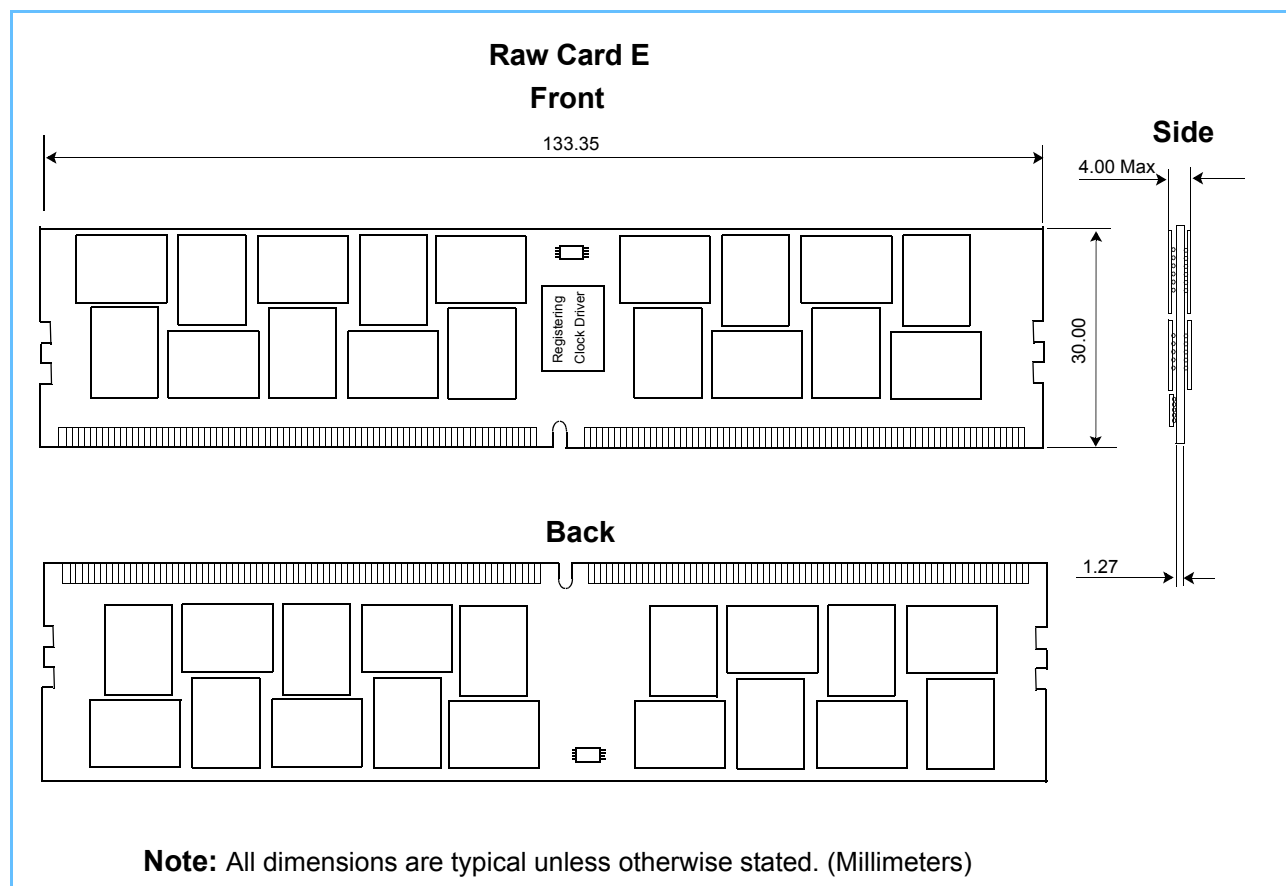
NOTE 1 X will reflect passed committee ballot at the time when specification is the issued at BOD ballot.

NOTE 2 P means the proposed speed for committee ballot.

Design Rules and Deviations

0.2 mm Via drill size used in Register breakout area.

General Layout



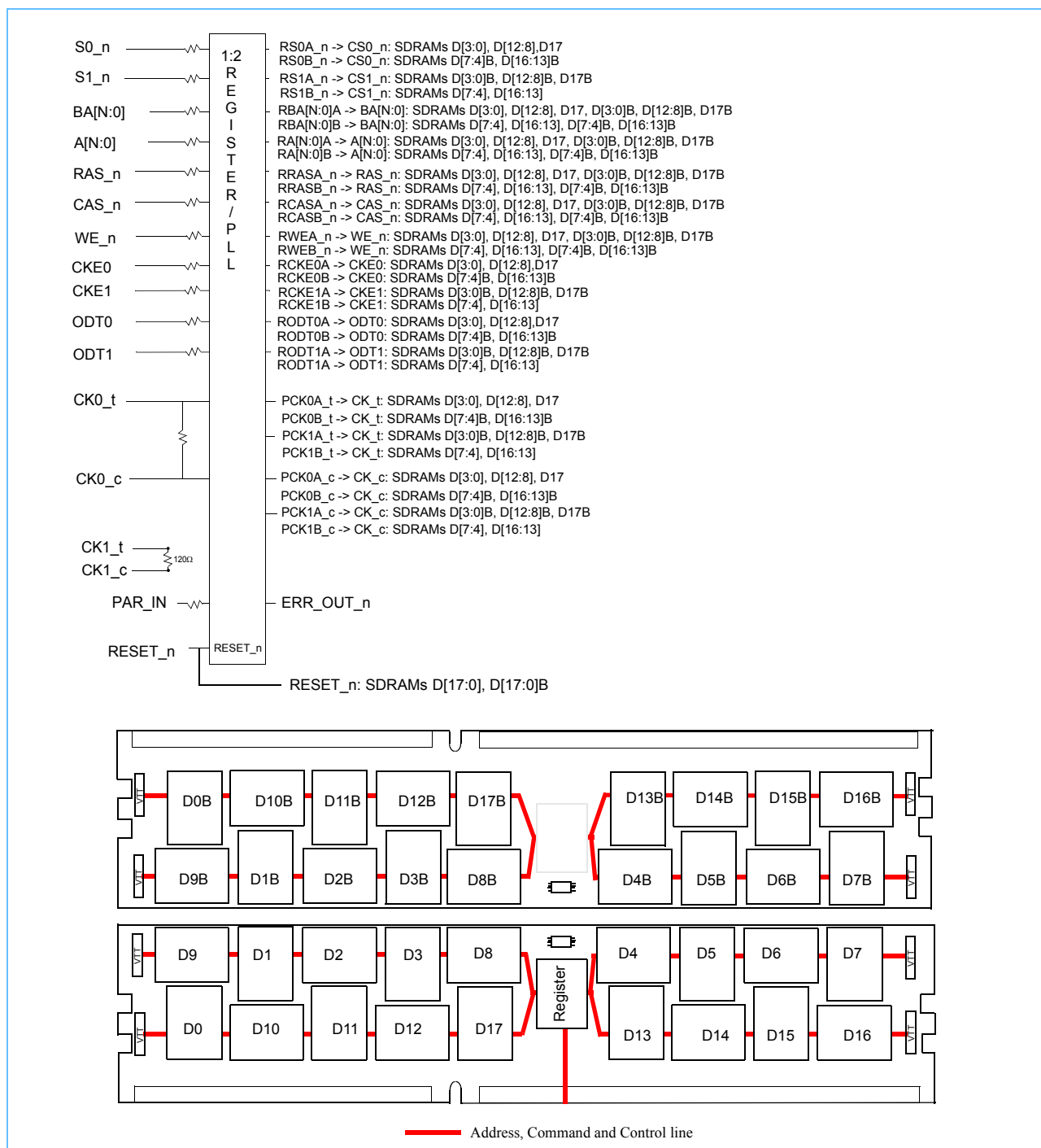
NOTE 1 Implementation and dimensions without heatspreader.

NOTE 2 Thermal sensor is placed within the Thermal Sensor Placement Area as defined in MO-269.

NOTE 3 In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heatspreader attached.

Functional Block Diagram

(x72 DIMM, populated as two physical ranks of x4 DDR3 SDRAMs, part 1 of 3)



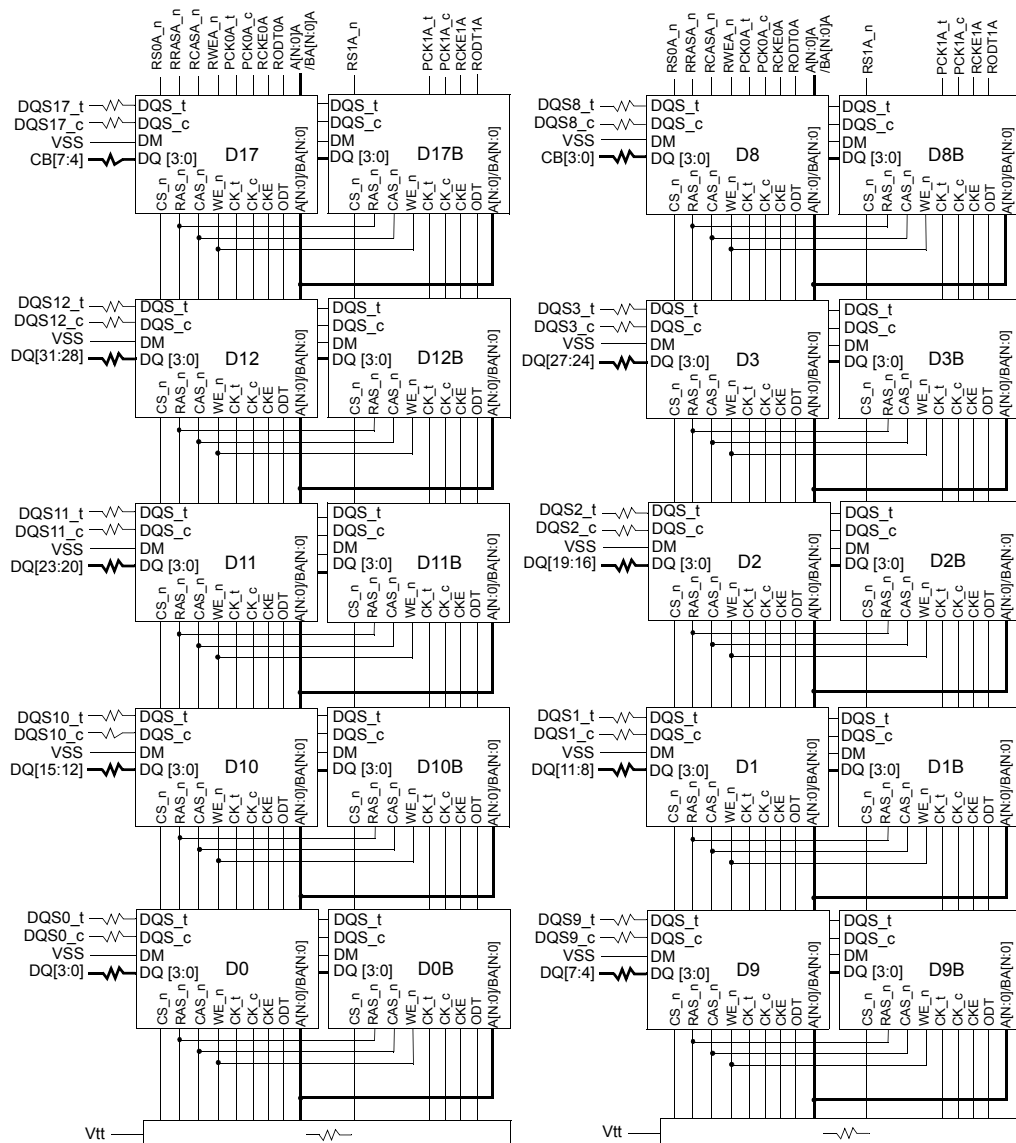
NOTE 1 S[3:2]_n are NC

NOTE 2 CK0_t and CK0_c are differentially terminated with single 120Ω ±5% resistor.

NOTE 3 CK1_t and CK1_c are differentially terminated with single 120Ω ±5% resistor but is not used.

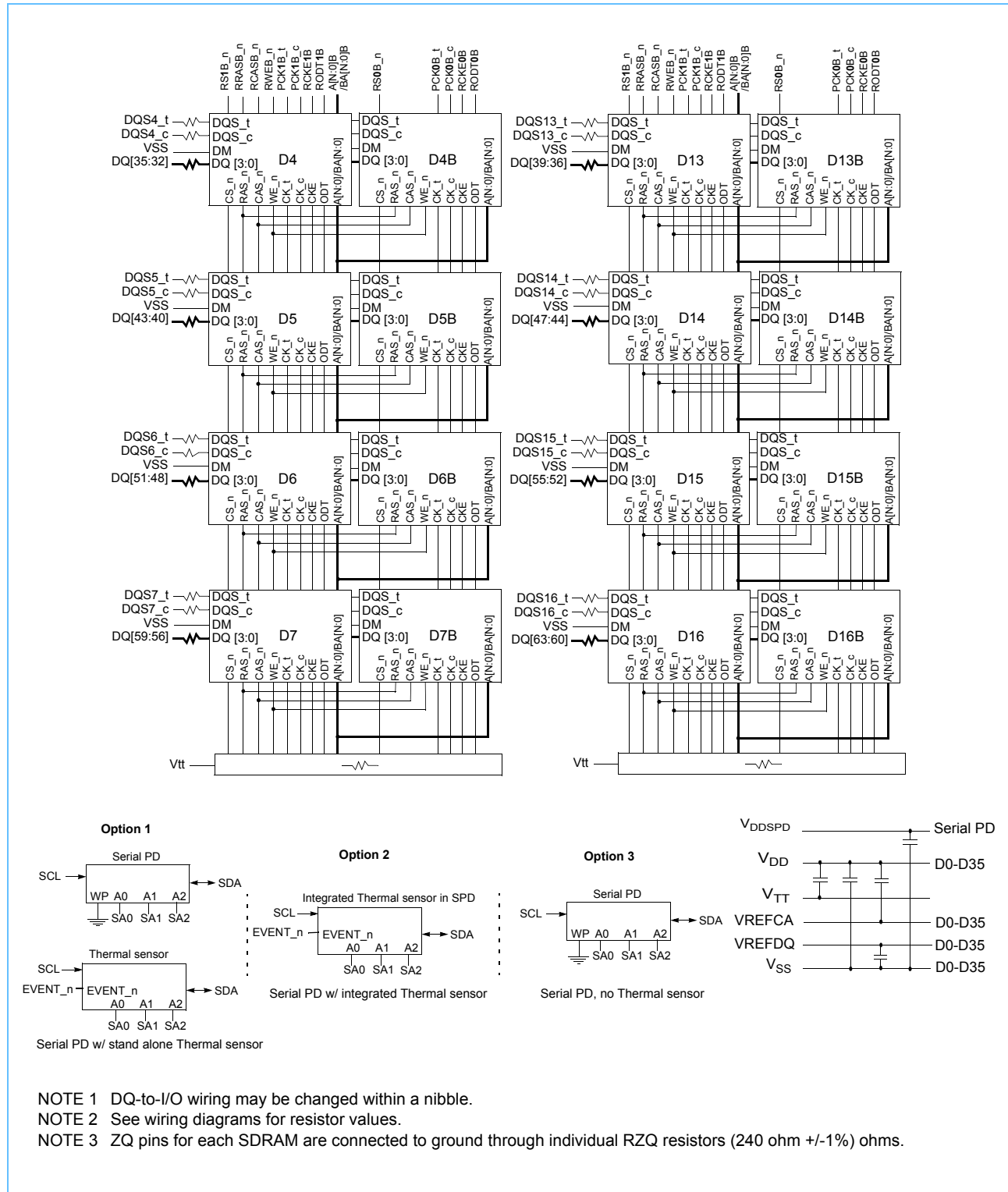
Functional Block Diagram

(x72 DIMM, populated as two physical ranks of x4 DDR3 SDRAMs, part 2 of 3)



Functional Block Diagram

(x72 DIMM, populated as two physical ranks of x4 DDR3 SDRAMs, part 3 of 3)



Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specification.

DRAMs per output	Register Type	RegisterSpeedGrade PC3-6400	RegisterSpeedGrade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
20/ 16	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only.

They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to matchmodule implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.