

Appendix H - Raw Card H

DDR3 Registered DIMM Design File

Revision	Applicable Design File	Applicable BOM
0.82	PC3-6400-4R-RDIMM_RC_H0_REV080_20080619.brd	PC3-6400-4R-RDIMM_RC_H0_REV080_20080619_BOM.pdf

Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
2GB	256Mx72	512Mbit	64Mx8	36	4	13/10/3	AB*
4GB	512Mx72	1Gbit	128Mx8	36	4	14/10/3	AB*
8GB	1Gx72	2Gbit	256Mx8	36	4	15/10/3	AB*
16GB	2Gx72	4Gbit	512Mx8	36	4	16/10/3	AB*
32GB	4Gx72	8Gbit	1Gx8	36	4	16/11/3	AB*

*Note: without heatspreader; variations with heatspreader are TBD

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
10.0 x 13.0	8	78 Ball FBGA	x8 planar, double row	DW-z

Supported Speeds

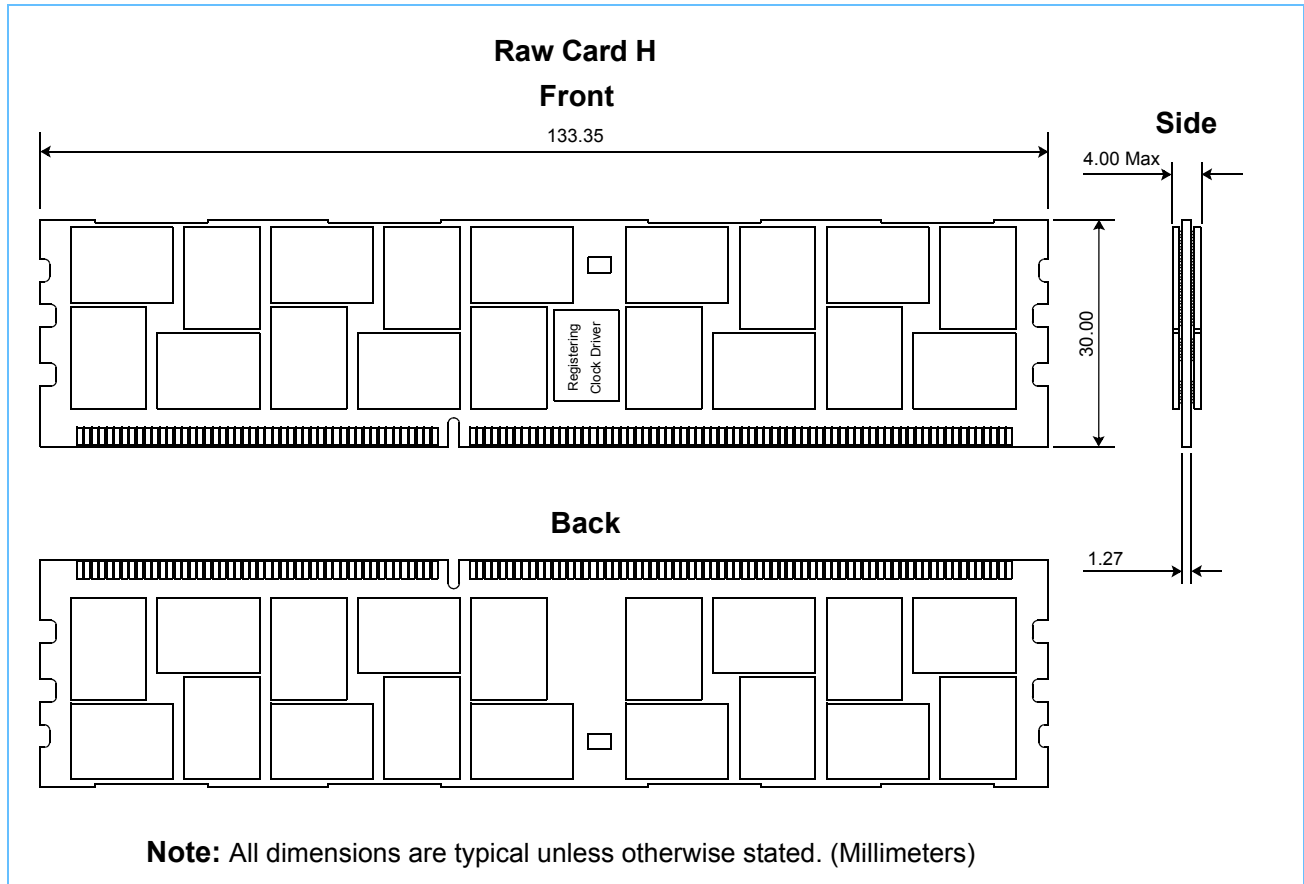
PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
X	X			

Note: X will reflect passed committee ballot at the time when specification is issued at BOD ballot.

Design Rules and Deviations

Via drill size is 0.20 mm, Copper pour to any copper feature is 0.15 mm on all signal layers, Signal line to pad is 0.10 mm, Via pad size is 0.40 mm, Via to Via is 0.14 mm, Drill to Drill is 0.34mm, Data nets are dual referenced between V_{DD} and V_{SS} .

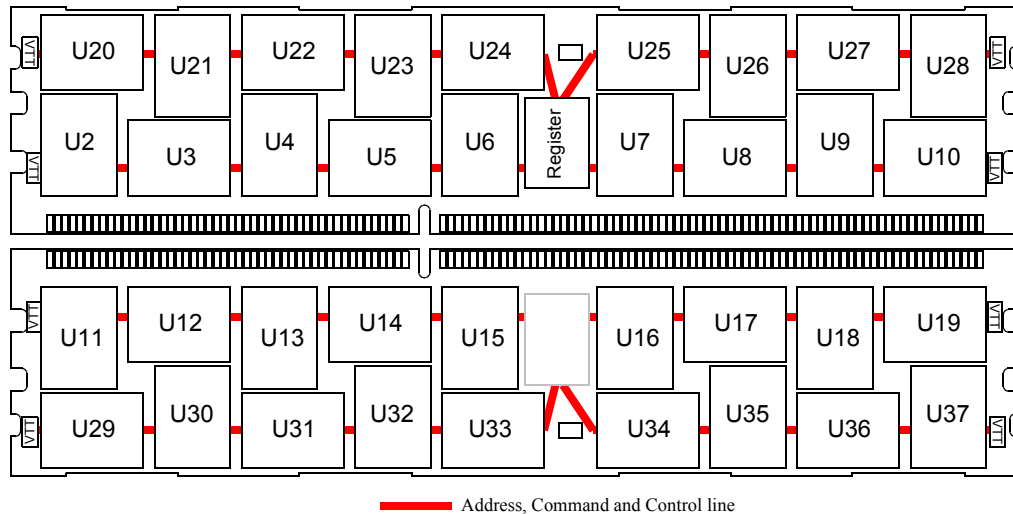
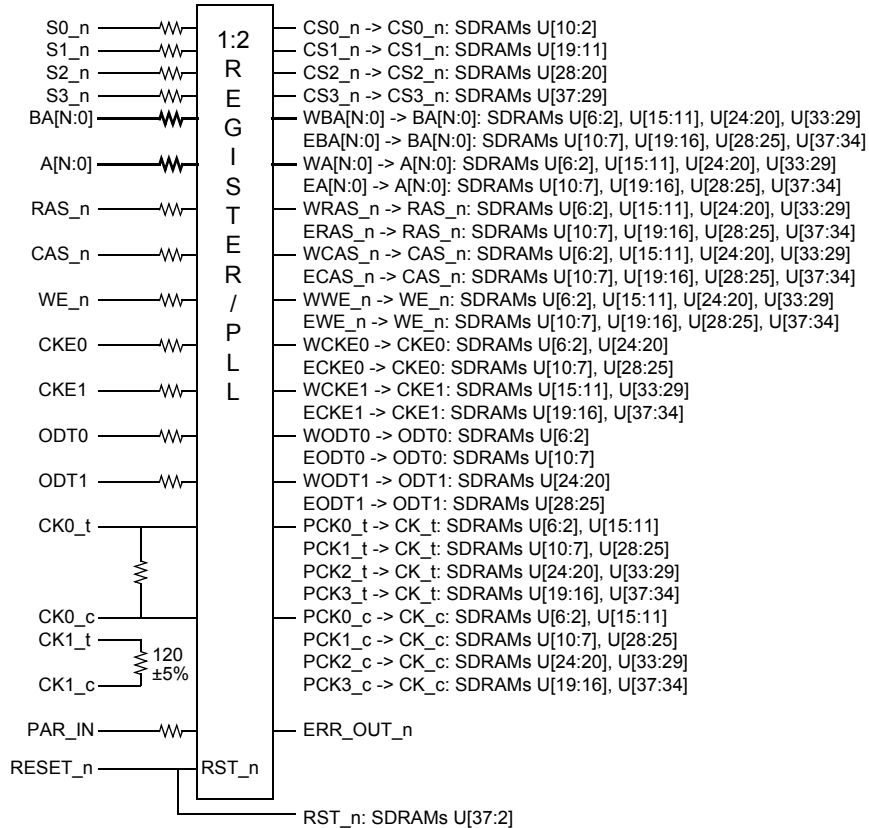
General Layout:



Note: Thermal sensor placement complies with MO-269. Restricted register placement is only required to support the Full DIMM Heat Spreader for stacked DRAM designs. This raw card design uses only monolithic DRAMs so register placement is not required to comply.

Functional Block Diagram (Part 1 of 3)

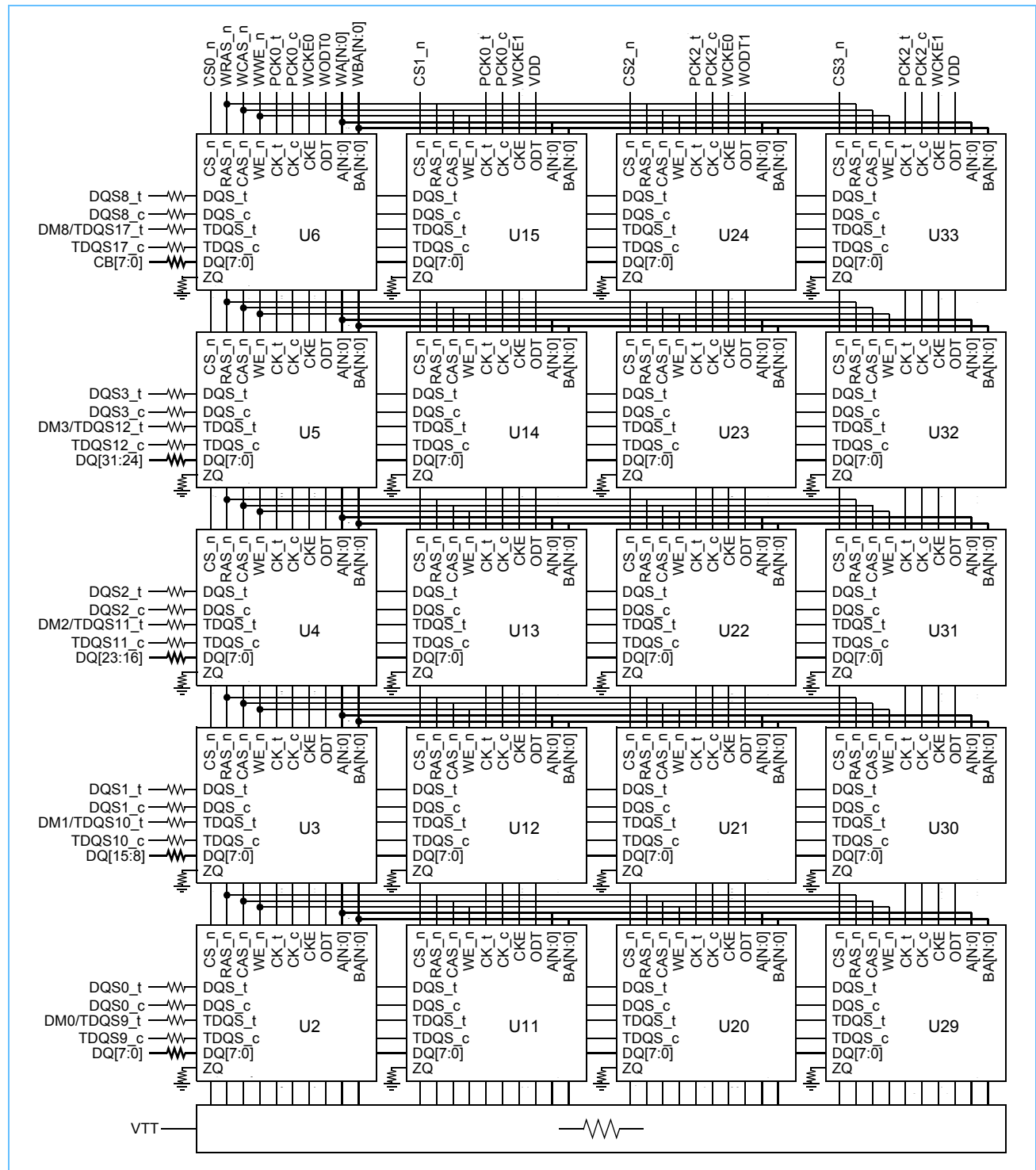
(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs)



1. PCK_t and PCK_c are differentially terminated with single resistor (See net topology diagram).

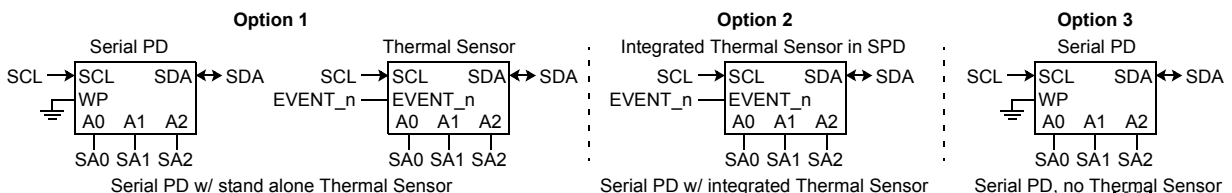
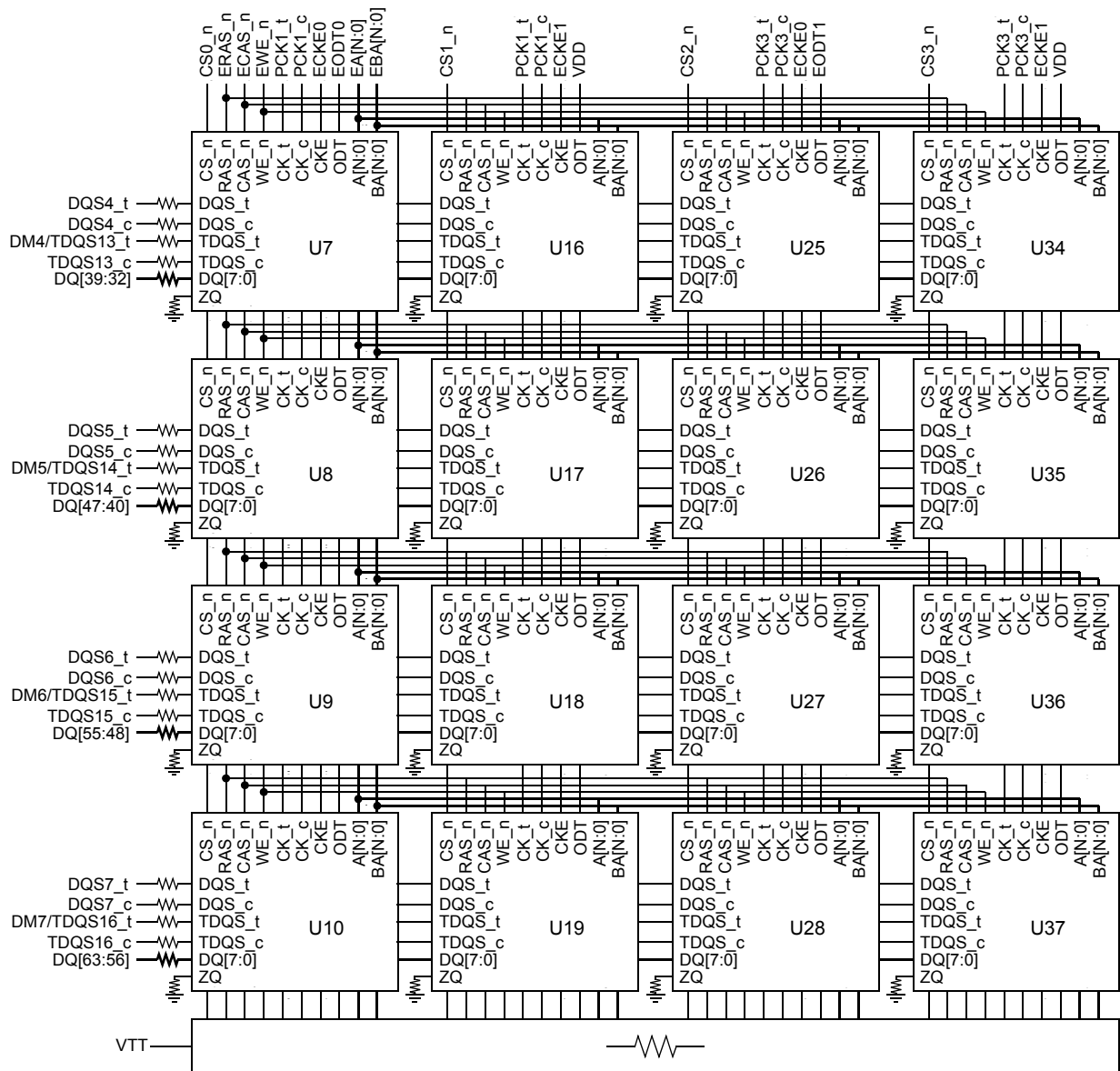
Functional Block Diagram (Part 2 of 3)

(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs)



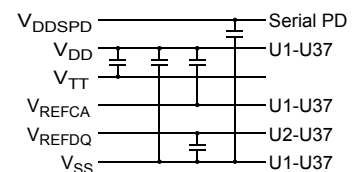
Functional Block Diagram (part 3 of 3)

(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. See wiring diagrams for resistor values.
3. ZQ pins of each SDRAM are connected to individual RZQ resistors (240 +/-1%) ohms.



Register Component Specifications

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specification.

DRAMs per output	Register Type	Register Speed Grade PC3-6400	Register Speed Grade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
20/16	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	TBD	1

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These register control bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These register control bits are used by Register, DIMM or System vendors for test and characterization purposes only. They must be programmed to zero for normal operation

3. Card type specific (Card):

These register control bits must be programmed to a certain value based on the raw card. The values are given in the table. These bits will be defined and balloted during the raw card development. DIMM is only guaranteed to work with those bits set appropriately.

4. Application specific bits (A/S):

These register control bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.

Register Control Word	Bit	Function	Type	Register Settings
				Raw Card H
RC0	DBA1	B outputs disabled	Card	0
	DBA0	A outputs disabled	Card	0
	DA4	Float outputs	A/S	“0” or “1”
	DA3	Output Inversion	Card	0
RC1	DBA1	Disable Y3_t/Y3_c clock	Card	0
	DBA0	Disable Y2_t/Y2_c clock	Card	0
	DA4	Disable Y1_t/Y1_c clock	Card	0
	DA3	Disable Y0_t/Y0_c clock	Card	0
RC2	DBA1	Frequency Band Select	Test	0
	DBA0	Input Bus Termination	A/S	“0” or “1”
	DA4	1T/3T Output timing	A/S	“0” or “1”
	DA3	Address and Command nets prelaunch (Control Signals QxCKE, QxCS, QxODT do not apply)	Card	0

Register Control Word	Bit	Function	Type	Register Settings
				Raw Card H
RC3	DBA1	Driver Characteristics: Command/Address Driver-B Outputs	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Command/Address Driver-A Outputs	Card	0
	DA3		Card	1
RC4	DBA1	Driver Characteristics: Control Driver-B Outputs	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Control Driver-A Outputs	Card	0
	DA3		Card	1
RC5	DBA1	Driver Characteristics: Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers	Card	0
	DA3		Card	1
RC6	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC7	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC8	DBA1	Extended IBT Settings	Card	0
	DBA0		A/S	"0" or "1"
	DA4		A/S	"0" or "1"
	DA3		A/S	"0" or "1"
RC9	DBA1	CKE Power Down Mode Enable	A/S	"0" or "1"
	DBA0	CKE Power Down Mode	A/S	"0" or "1"
	DA4	Reserved for Future Use	RFU	0
	DA3	Reduced Drive Mode	A/S	"0" or "1"
RC10	DBA1	RDIMM Operating Speed	A/S	"0" or "1"
	DBA0		A/S	"0" or "1"
	DA4		A/S	"0" or "1"
	DA3		A/S	"0" or "1"

Register Control Word	Bit	Function	Type	Register Settings
				Raw Card H
RC11 ... RC15	DBA1	Reserved for Future Use	RFU	0
	DBA0		RFU	0
	DA4		RFU	0
	DA3		RFU	0