

Annex K - Raw Card K0 and K1

DDR3 Registered Dimm Design File

Row Card	Applicable Design File	Applicable BOM
K0	PC3-RDIMM_V80_RC_K0_20080424.brd	PC3-RDIMM-V80_RC_K0_20080424-Bom.pdf
K1	PC3-RDIMM_V090_RC_K1_20101220.brd	PC3-RDIMM_V090_RC_K1_20101220-Bom.pdf

NOTE: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
512MB	64Mx72	512Mbit	64Mx8	9	1	13/10/3	DB
1GB	128Mx72	1Gbit	128Mx8	9	1	14/10/3	DB
2GB	256Mx72	2Gbit	256Mx8	9	1	15/10/3	DB
4GB	512Mx72	4Gbit	512Mx8	9	1	16/10/3	DB
8GB	1Gx72	8Gbit	1Gx8	9	1	16/11/3	DB

SDRAM Configuration

RC	Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
K0	12.1 mm x 18.05 mm ¹	8	106 Ball FBGA ²	Planar	DW-z
K1	11 mm x 13 mm	8	78 Ball FBGA	Planar	DW-z

NOTE 1 Maximum DRAM size can be increased to 12.55 x 18.05 if heat spreader is not used.

NOTE 2 Only 82 pads are present on the reference design due to DRAM outline limitation.

Supported Speeds

RC	SPEED	PC3-6400	PC3-8500	PC3-10600	PC3-12800	PC3-14900	Notes
K0	DDR3	X	X	X			1
K1	DDR3	X	X	X	X	X	1
K1	DDR3L	X	X	X	X		1

NOTE 1 X will reflect passed committee ballot at the time when specification is issued at BOD ballot

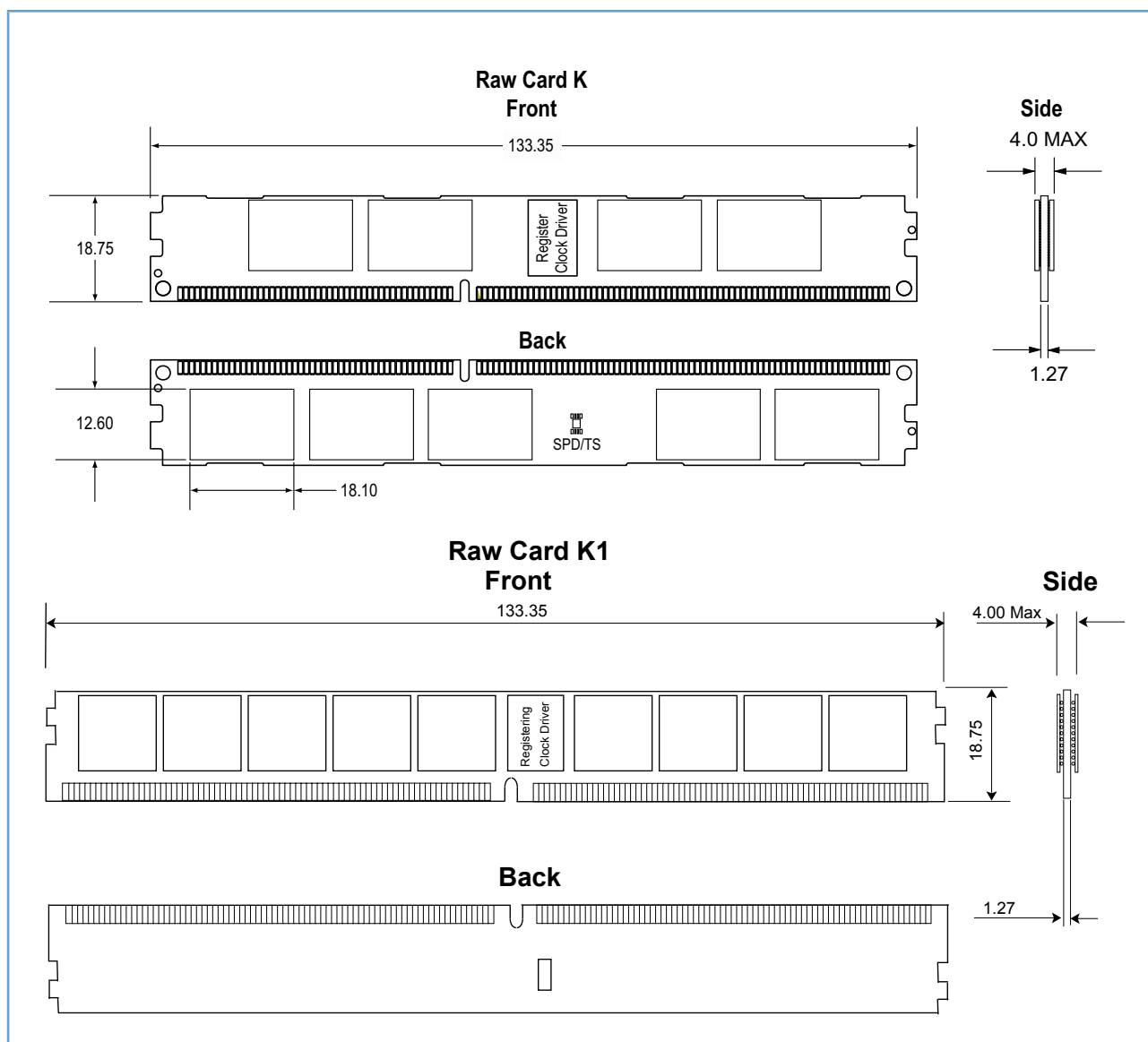
NOTE 2 P is proposed.

Design Rules and Deviations

None

General Layout for K0

x72 DIMM, populated as one physical ranks of x8 DDR3 SDRAMs



NOTE 1 All dimensions are typical unless otherwise stated.

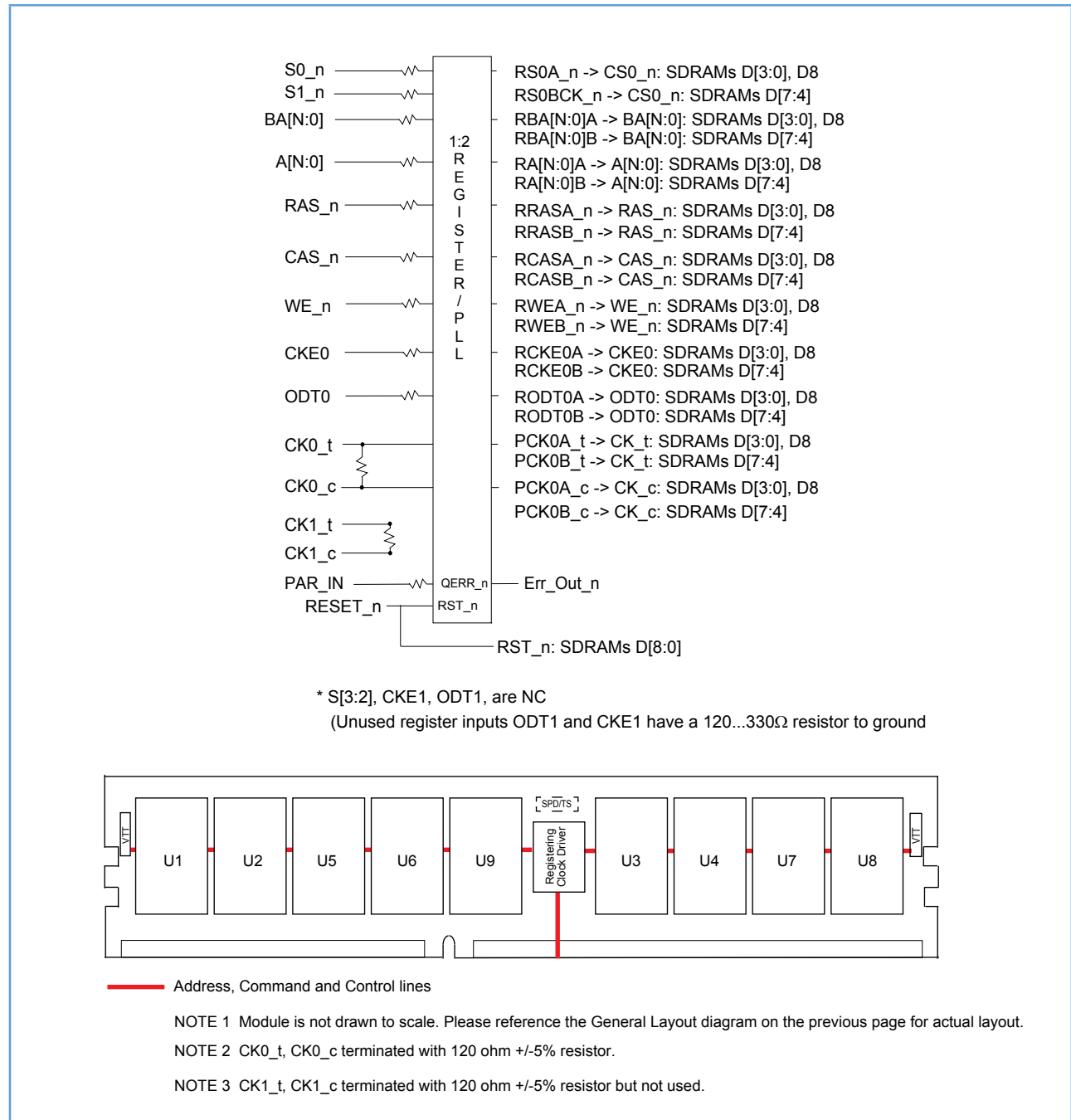
NOTE 2 Thermal sensor placement complies with MO-269 (Item# JC11.14-120). Restricted register placement is only required to support the Full DIMM Heat Spreader for stacked DRAM designs. This raw card design uses only monolithic DRAMs so register placement is not required to comply.

NOTE 3 Implementation and dimensions are without heat spreader.

NOTE 4 In the event that a heat spreader is added to the module, module thickness would increase. Please refer to MO-269 (Item# JC11.14-120) for dimensions of specific variations with heat spreader attached.

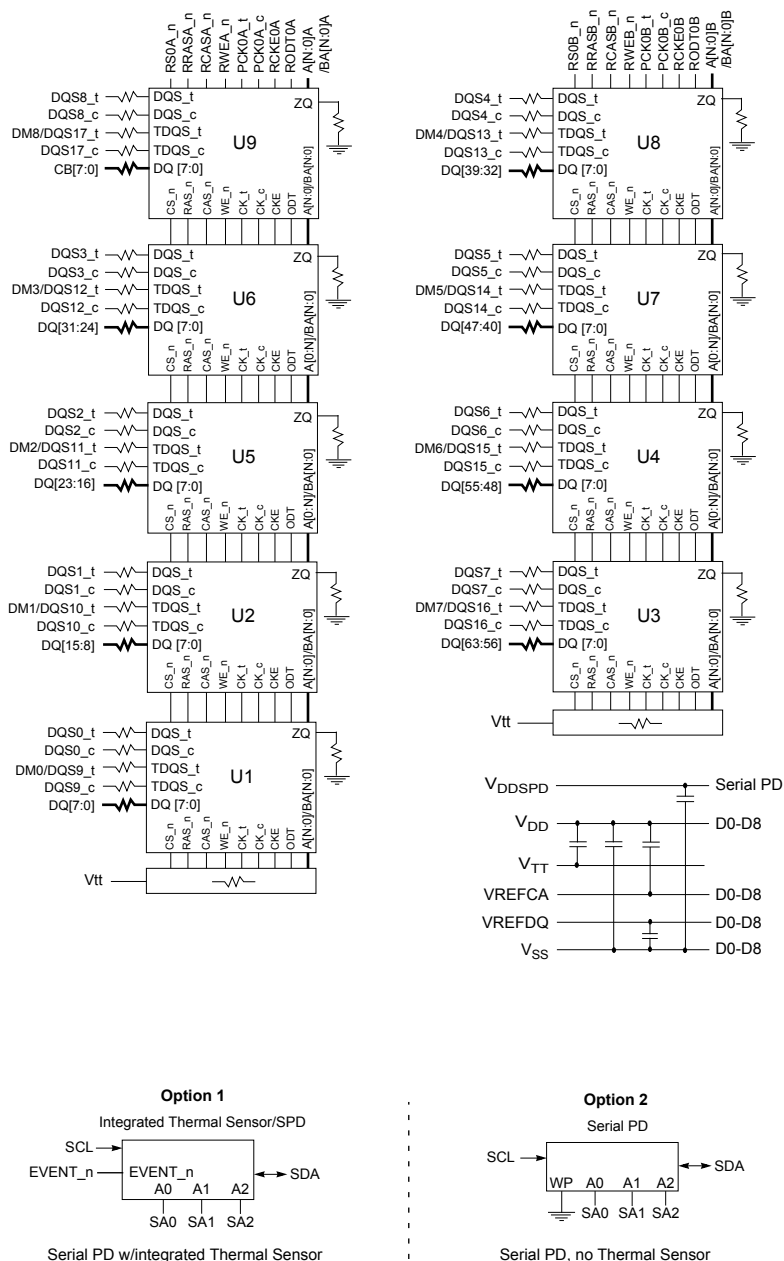
Block Diagram

x72 DIMM, populated as one physical rank of x8 DDR3 SDRAMs (Part 1 of 2)



Block Diagram

x72 DIMM, populated as one physical rank of x8 DDR3 SDRAMs (Part 2 of 2)



NOTE 1 DQ-to-I/O wiring may be changed within a byte.

NOTE 2 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

NOTE 3 The connection of the Serial PD to EVENT_n (Option 1) or to ground (Option 2) is realized by resistor options.

Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specifications

DRAMs per output	Register Type	Register Speed Grade PC3-6400	Register Speed Grade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Register Speed Grade PC3-14900	Quantity
5/4	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined. The respective SPD bits will be programmed to “0”.

2. Test bits (Test):

These bits are used by Register, DIMM or System vendors for test and characterization purposes only. They must be programmed to zero for normal operation. The respective SPD bits will be programmed to “0”.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match-module implementation must be verified by simulation and testing.

4. Application specific bits (A/S):

These bits are freely programmable by the user based on the actual system configuration in which this DIMM is used. The respective SPD bits will be programmed to “0” unless specified otherwise in the Register Control Word Settings table.

Register Control Word Settings for Raw Card K, and K1

Register Control Word	Bit	Function	Type	Register Setting
RC0	DBA1	B outputs disabled	Card	0
	DBA0	A outputs disabled	Card	0
	DA4	Float outputs	A/S	0 or 1
	DA3	Output Inversion	Card	0
RC1	DBA1	Disable Y3_t/Y3_c clock	Card	1
	DBA0	Disable Y2_t/Y2_c clock	Card	1
	DA4	Disable Y1_t/Y1_c clock	Card	0
	DA3	Disable Y0_t/Y0_c clock	Card	0
RC2	DBA1	Frequency Band Select	Test	0
	DBA0	Input Bus Termination	A/S	0 or 1
	DA4	1T/3T Output timing	A/S	0 or 1
	DA3	Address- and command-nets prelaunch (Control Signals QxCKE, QxCs, QxODT do not apply)	Card	0

Register Control Word	Bit	Function	Type	Register Setting
RC3	DBA1	Driver Characteristics: Command/Address Driver-B Outputs	Card	0
	DBA0		Card	0
	DA4	Driver Characteristics: Command/Address Driver-A Outputs	Card	0
	DA3		Card	0
RC4	DBA1	Driver Characteristics: Control Driver-B Outputs	Card	0
	DBA0		Card	0
	DA4	Driver Characteristics: Control Driver-A Outputs	Card	0
	DA3		Card	0
RC5	DBA1	Driver Characteristics: Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers	Card	0
	DBA0		Card	0
	DA4	Driver Characteristics: Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers	Card	0
	DA3		Card	0
RC6	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC7	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC8	DBA1	Extended IBT settings	Card	0
	DBA0		A/S	0 or 1
	DA4		A/S	0 or 1
	DA3		A/S	0 or 1
RC9	DBA1	CKE Power Down Mode Enable	A/S	0 or 1
	DBA0	CKE Power Down Mode	A/S	0 or 1
	DA4	Reserved for Future Use	RFU	0
	DA3	Reduced Drive Mode	A/S	0 or 1
RC10 ... RC15	DBA1	Reserved for Future Use	RFU	0
	DBA0		RFU	0
	DA4		RFU	0
	DA3		RFU	0