

## Appendix U - Raw Card U

### DDR3 Registered DIMM Design File

| Raw Card | Applicable Design File            | Applicable BOM                    |
|----------|-----------------------------------|-----------------------------------|
| U0       | PC3-RDIMM_V050_RC-U0_20111107.brd | PC3-RDIMM_V050_RC-U0_20111107_BOM |

Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only, in these cases the design files will not be updated.

### Module Configuration

| DIMM     |              | SDRAM   |              | # of SDRAMs | # of Physical Ranks | # of Address bits row/col/Bank | MO-269 variation |
|----------|--------------|---------|--------------|-------------|---------------------|--------------------------------|------------------|
| Capacity | Organization | Density | Organization |             |                     |                                |                  |
| 16GB     | 2Gx72        | 2Gbit   | 512Mx4       | 72          | 4                   | 14/11/3                        | DB               |
| 32GB     | 4Gx72        | 4Gbit   | 1Gx4         | 72          | 4                   | 15/11/3                        | DB               |
| 64GB     | 8Gx72        | 8Gbit   | 2Gx4         | 72          | 4                   | 16/11/3                        | DB               |
| 128GB    | 16Gx72       | 16Gbit  | 4Gx4         | 72          | 4                   | 16/12/3                        | DB               |

Note: Some heat spreaders may not be covered within these variations.

### SDRAM Configuration

| Supported DRAM Outline (Width x Length) max. | # of Banks in SDRAM | SDRAM Package Type   | Package Type             | MO-207 variation |
|----------------------------------------------|---------------------|----------------------|--------------------------|------------------|
| 11.0 x 12.5 mm                               | 8                   | 78 Ball stacked FBGA | quad stacked, single row | DW-z             |

### Supported Speeds

|       | PC3-6400 | PC3-8500 | PC3-10600 | PC3-12800 | Notes |
|-------|----------|----------|-----------|-----------|-------|
| DDR3  | X        | X        |           |           |       |
| DDR3L | X        | X        |           |           |       |

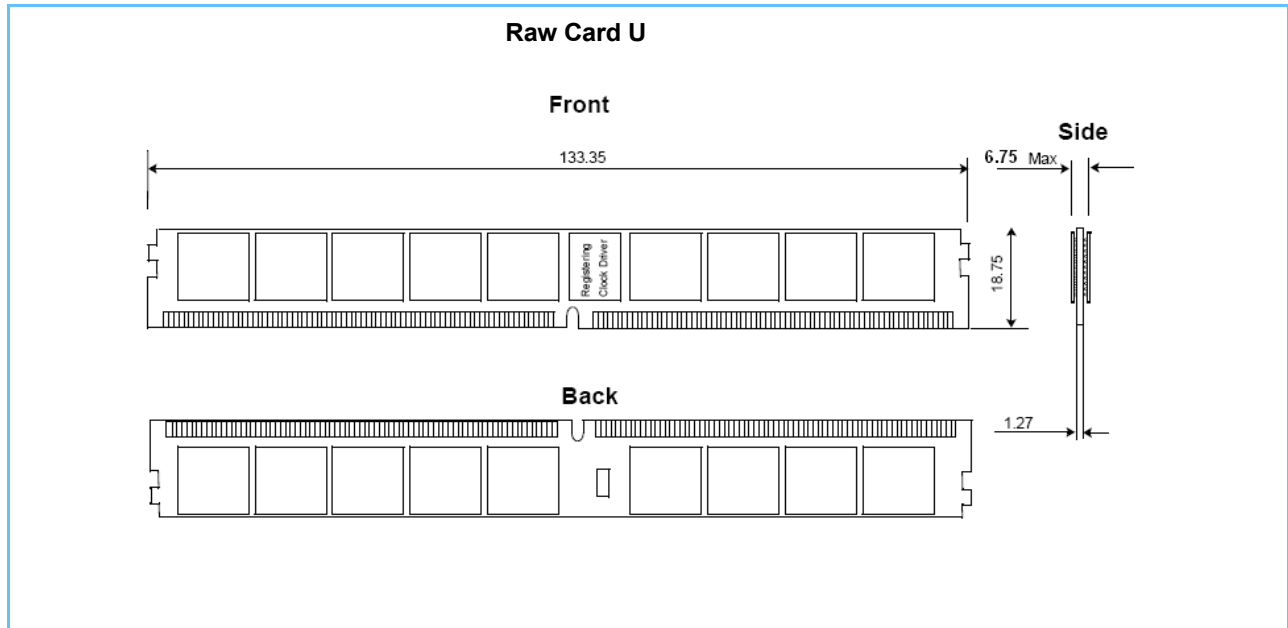
Note: P reflects speed grades proposed for this ballot. X reflects speed grades from previous ballots. JEDEC office to change P to X before publication

### Design Rules and Deviations

1. This card uses blind vias.
2. Uses 0.100 mm and 0.075 mm wide traces for inner layers.

## General Layout

x72 DIMM, populated as four physical ranks of stacked x4 DDR3 SDRAMs



**Note1** : All dimensions are typical unless otherwise stated. (Millimeters)

**Note2** : Serial PD with thermal sensor is within the thermal sensor placement area as defined in MO-269.

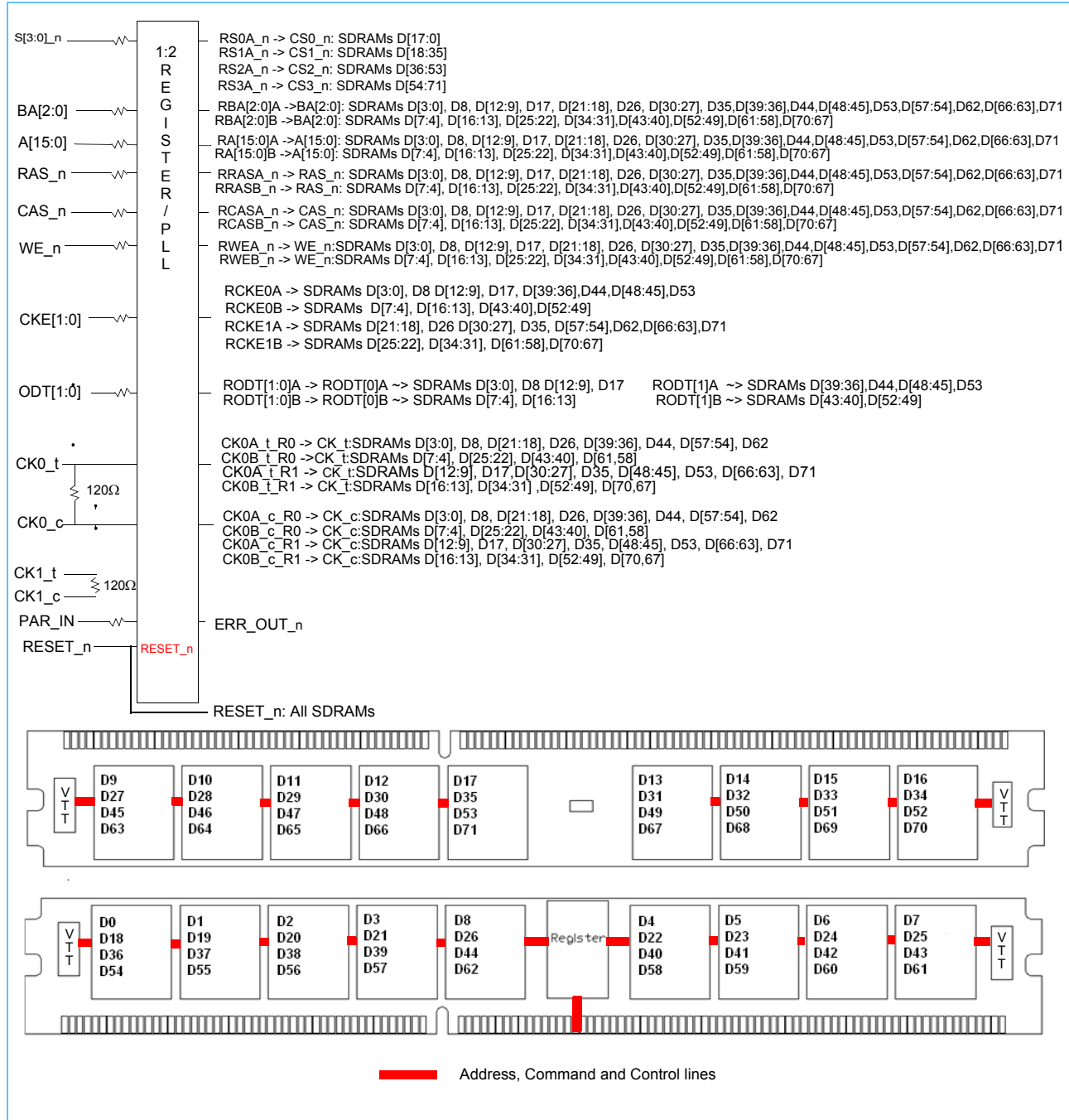
**Note3** : Registering clock driver is placed within the Register Placement Area as defined in MO-269.

**Note4** : Implementation and dimensions are without heat spreader.

**Note5** : In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heat spreader attached.

## Block Diagram

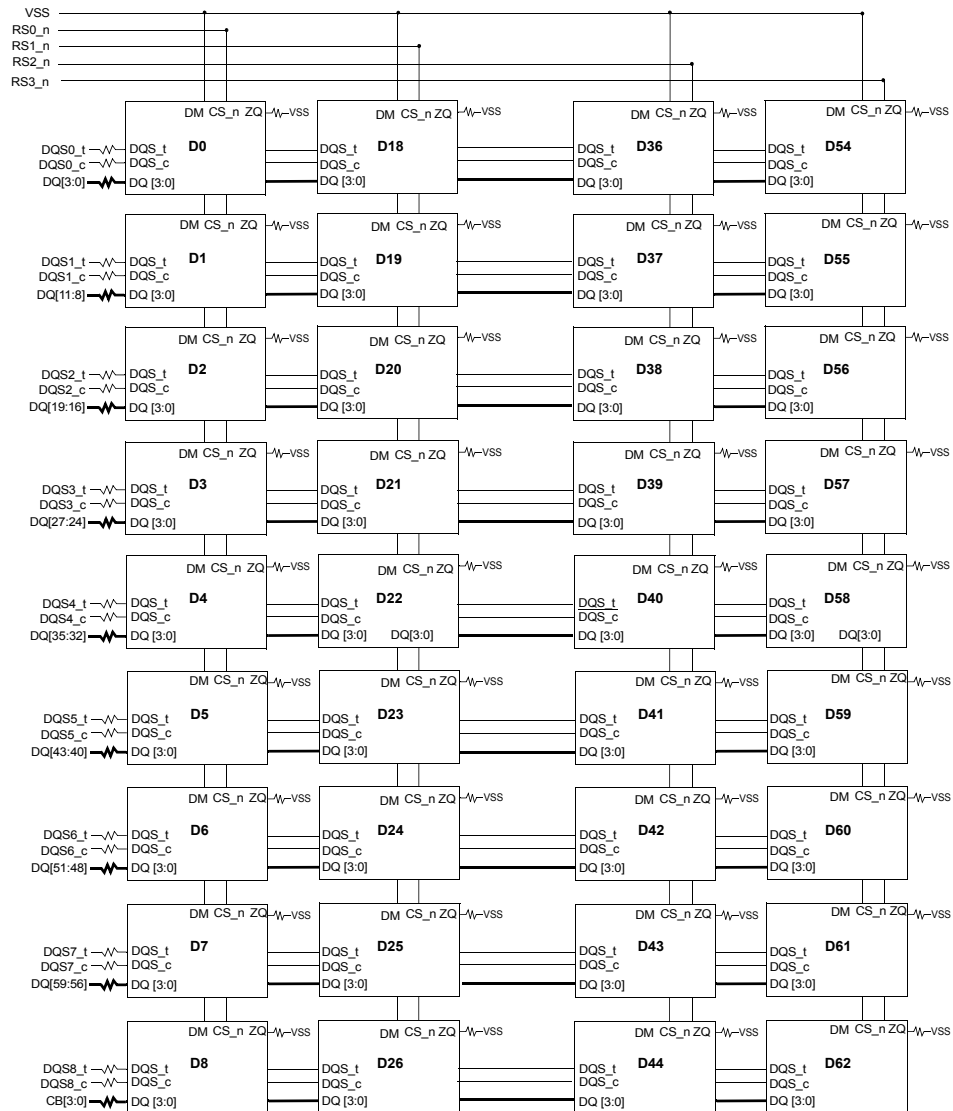
x72 DIMM, populated as four physical ranks of stacked x4 DDR3 SDRAMs (part 1 of 3)



1. CK0\_t and CK0\_c are differentially terminated with a single 120Ω ±5% resistor.
2. CK1\_t and CK1\_c are differentially terminated with a single 120Ω ±5% resistor, but not is used.
3. The module drawing on this page is not drawn to scale.
4. All resistors are 22Ω unless otherwise stated.

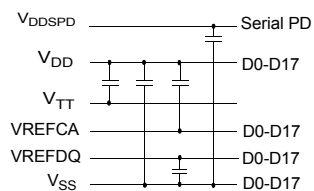
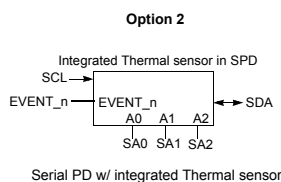
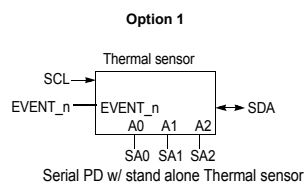
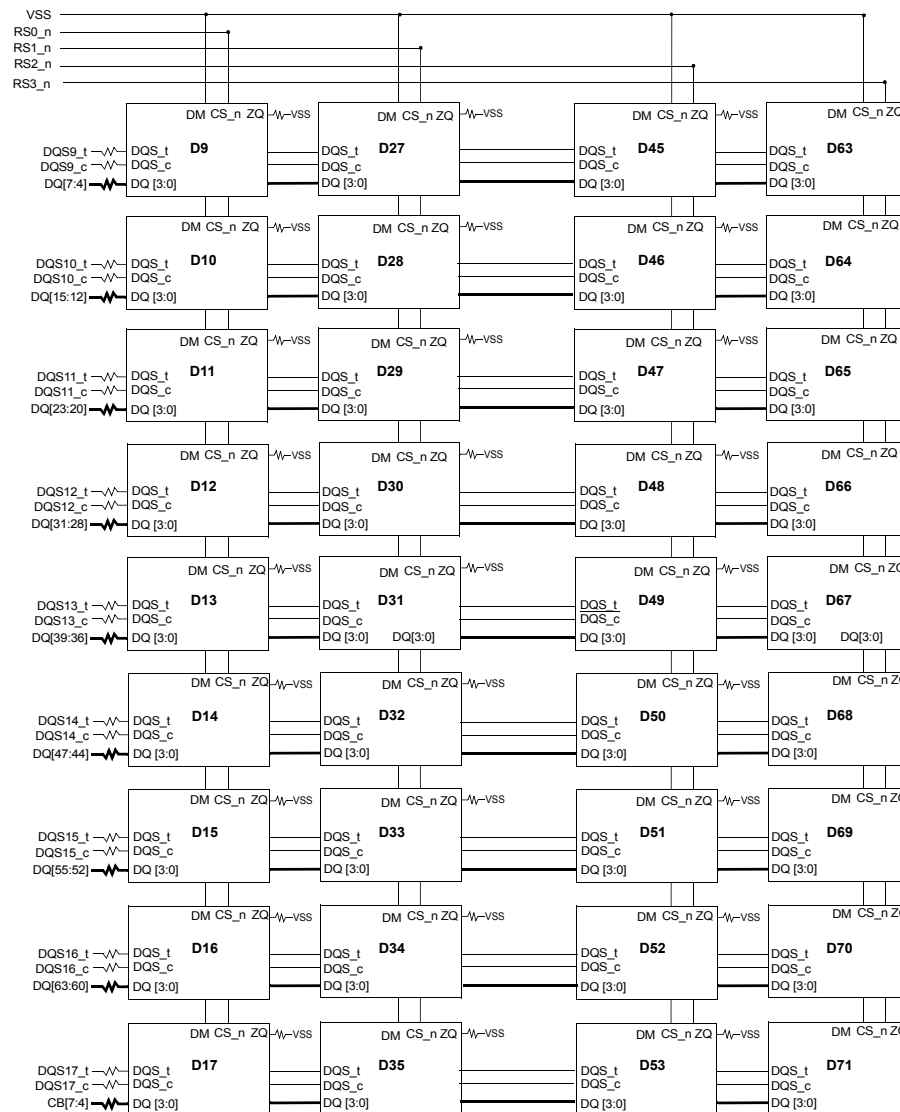
## Block Diagram

x72 DIMM, populated as four physical ranks of stacked x4 DDR3 SDRAMs (part 2 of 3)



## Block Diagram

x72 DIMM, populated as four physical ranks of stacked x4 DDR3 SDRAMs (part 3 of 3)



### Notes:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are  $15\Omega \pm 5\%$ .
3. See the wiring diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.

## Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

### Component Specifications

| DRAMs per output | Register Type   | RegisterSpeedGrade<br>PC3-6400 | RegisterSpeedGrade<br>PC3-8500 | Register Speed Grade<br>PC3-10600 | Register Speed Grade<br>PC3-12800 | Quantity |
|------------------|-----------------|--------------------------------|--------------------------------|-----------------------------------|-----------------------------------|----------|
| 40 / 32          | 1:2 28-bit 1.5V | SSTE32882                      | SSTE32882                      | SSTE32882                         | SSTE32882                         | 1        |

### Register Control Bit Settings

#### Types of Control Bits:

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only. They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match-module implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.

## Register Control Word Setting for Raw Card U

| Register Control Word | Bit  | Function                                                                                | Type | Register Setting |
|-----------------------|------|-----------------------------------------------------------------------------------------|------|------------------|
| RC0                   | DBA1 | B outputs disabled                                                                      | Card | 0                |
|                       | DBA0 | A outputs disabled                                                                      | Card | 0                |
|                       | DA4  | Float outputs                                                                           | A/S  | 0 or 1           |
|                       | DA3  | Output Inversion                                                                        | Card | 0                |
| RC1                   | DBA1 | Disable Y3_t/Y3_c clock                                                                 | Card | 0                |
|                       | DBA0 | Disable Y2_t/Y2_c clock                                                                 | Card | 0                |
|                       | DA4  | Disable Y1_t/Y1_c clock                                                                 | Card | 0                |
|                       | DA3  | Disable Y0_t/Y0_c clock                                                                 | Card | 0                |
| RC2                   | DBA1 | Frequency Band Select                                                                   | Test | 0                |
|                       | DBA0 | Input Bus Termination                                                                   | A/S  | 0 or 1           |
|                       | DA4  | 1T/3T Output timing                                                                     | A/S  | 0 or 1           |
|                       | DA3  | Address- and command-nets prelaunch (Control Signals QxCCKE, QxCSS, QxODT do not apply) | Card | 0                |
| RC3                   | DBA1 | Driver Characteristics:<br>Command/Address<br>Driver-B Outputs                          | Card | 1                |
|                       | DBA0 |                                                                                         | Card | 0                |
|                       | DA4  | Driver Characteristics:<br>Command/Address<br>Driver-A Outputs                          | Card | 1                |
|                       | DA3  |                                                                                         | Card | 0                |
| RC4                   | DBA1 | Driver Characteristics:<br>Control Driver-B<br>Outputs                                  | Card | 0                |
|                       | DBA0 |                                                                                         | Card | 1                |
|                       | DA4  | Driver Characteristics:<br>Control Driver-A<br>Outputs                                  | Card | 0                |
|                       | DA3  |                                                                                         | Card | 1                |
| RC5                   | DBA1 | Driver Characteristics:<br>Clock Y0_t, Y0_c, Y2_t, and Y2_c<br>Output Drivers           | Card | 0                |
|                       | DBA0 |                                                                                         | Card | 1                |
|                       | DA4  | Driver Characteristics:<br>Clock Y1_t, Y1_c, Y3_t, and Y3_c<br>Output Drivers           | Card | 0                |
|                       | DA3  |                                                                                         | Card | 1                |
| RC6                   | DBA1 | Reserved, free to use by register vendor                                                | Test | 0                |
|                       | DBA0 |                                                                                         | Test | 0                |
|                       | DA4  |                                                                                         | Test | 0                |
|                       | DA3  |                                                                                         | Test | 0                |