

Appendix W - Raw Card W

DDR3 Registered DIMM Design File

Specification Revision	Applicable Design File	Applicable BOM
1.10	PC3-RDIMM_V110_RC-W_20081125.brd	PC3-RDIMM_RC-W_RV110_RC-W_20081125_bom.xls

Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
4GB	512Mx72	512Mbit	128Mx4	72	4	13/11/3	AB
8GB	1Gx72	1Gbit	256Mx4	72	4	14/11/3	AB
16GB	2Gx72	2Gbit	512Mx4	72	4	15/11/3	AB
32GB	4Gx72	4Gbit	1Gx4	72	4	16/11/3	AB
64GB	8GX72	8Gbit	2Gx4	72	4	16/12/3	AB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	SDRAM Organization	MO-207 variation
10.0 mm x 11.5 mm	8	78 Ball stacked FBGA	x4, stacked, double row	DT-z

Supported Speeds

PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
X	X			

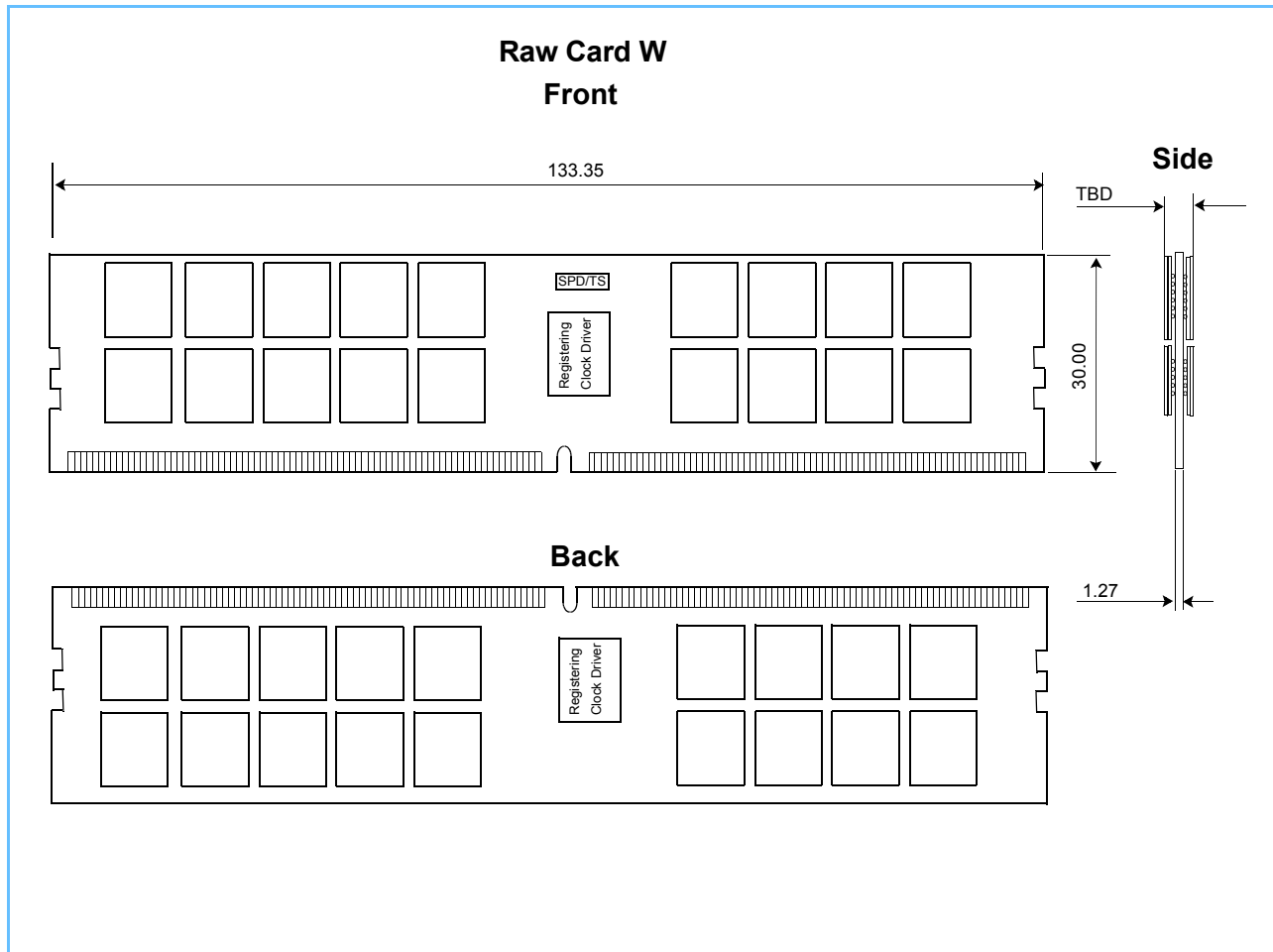
Note: X will reflect passed committee ballot at the time when specification is issued at BOD ballot

Design Rules and Deviations

1. 0201 capacitors and resistors are used in this design.
2. Blind vias are used in this design.
3. Trace widths of .0762 and .080, and .0857 internal; .089 outer routing layers.
4. Impedance of outer layers is ~ 83 ohm; inner layer 54 ohm (L2 & L9); 60 ohm L5 & L6.

General Layout

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs)



Note 1: All dimensions are typical unless otherwise stated. (Millimeters)

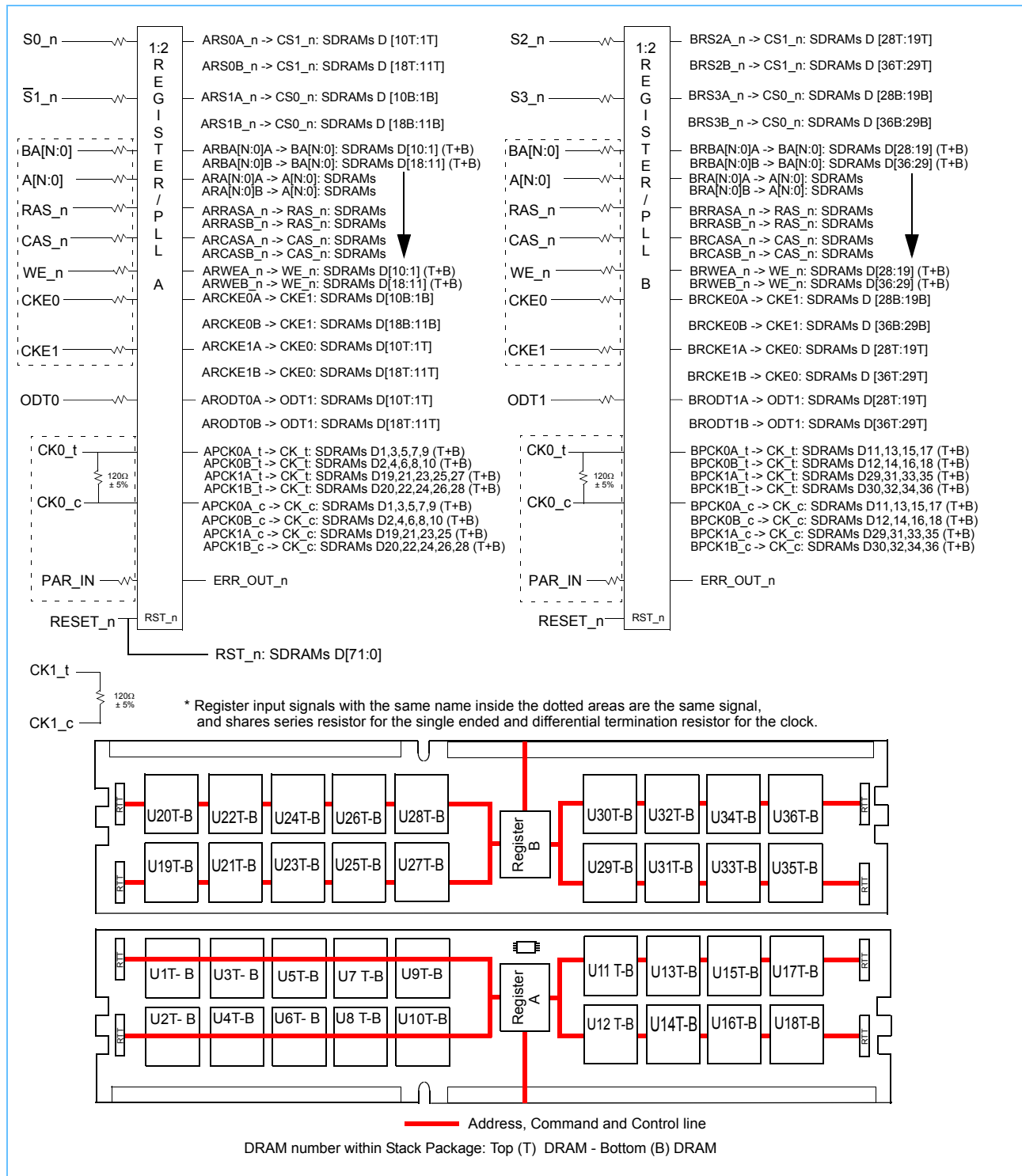
Note 2: Thermal sensor is placed within the thermal sensor placement area as defined in MO-269.

Note 3: Registering clock driver is placed within the Register Placement Area as defined in MO-269.

Note 4: Implementation and dimensions shown without heat spreader.

Note 5: In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heat spreader attached.

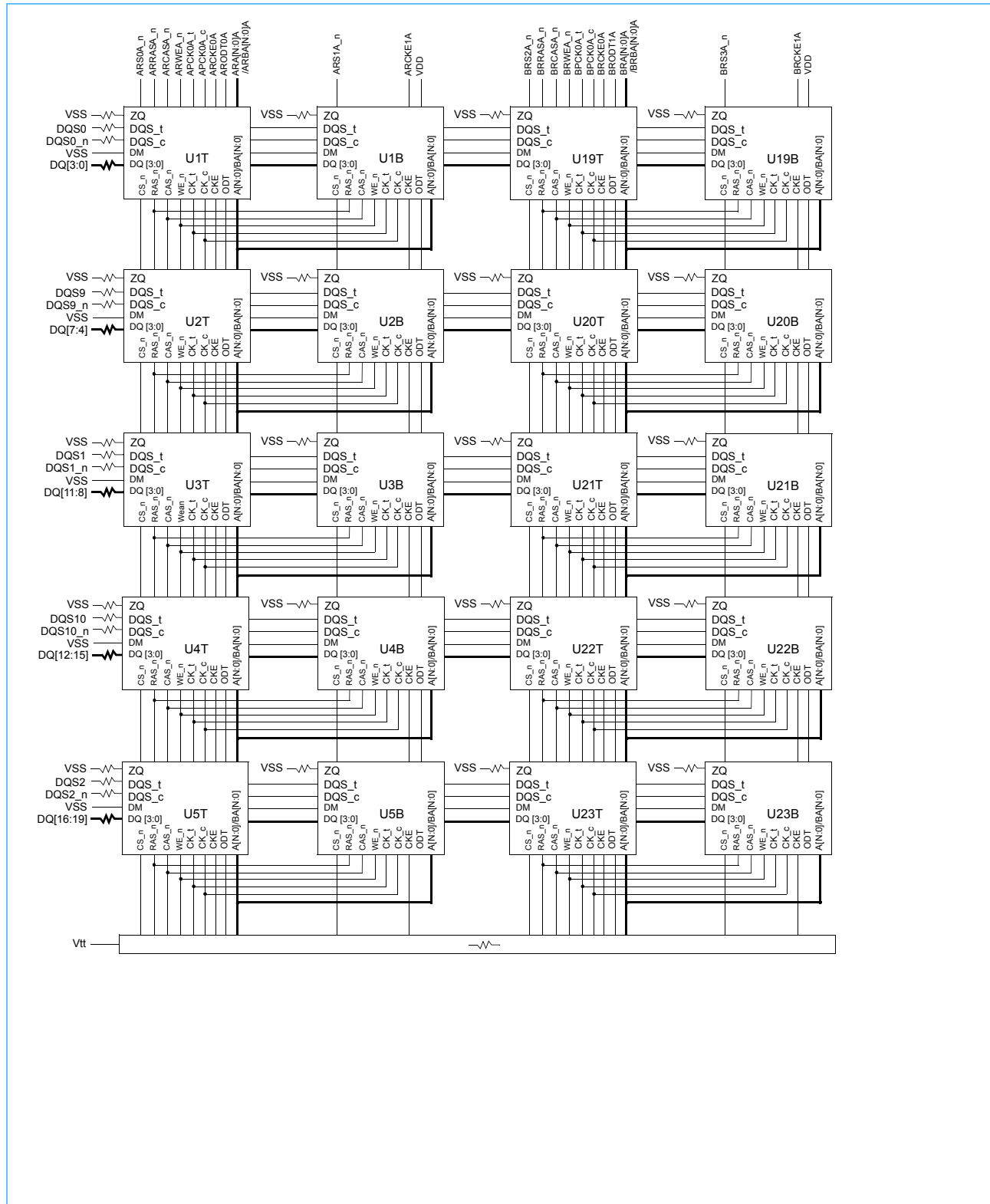
x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 1 of 5)



1. CK0_t and CK0_c are differentially terminated with a single $120\Omega \pm 5\%$ resistor.
2. CK1_t and CK1_c are differentially terminated with a single $120\Omega \pm 5\%$ resistor, but is not used.
3. Unused register inputs ODT1 for Register A and ODT0 for Register B are tied to ground.
4. The module drawing on this page is not drawn to scale.

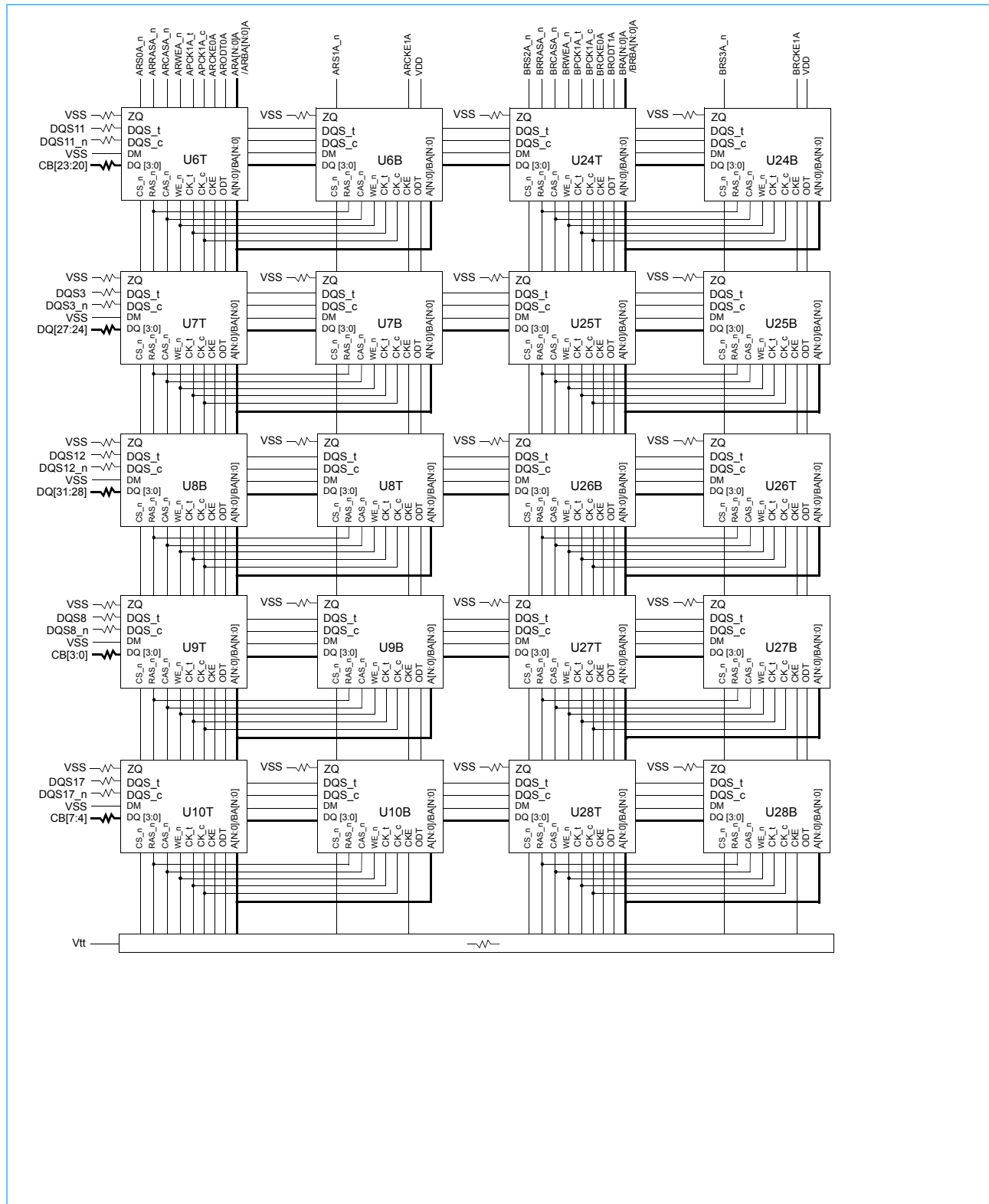
Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 2 of 5)



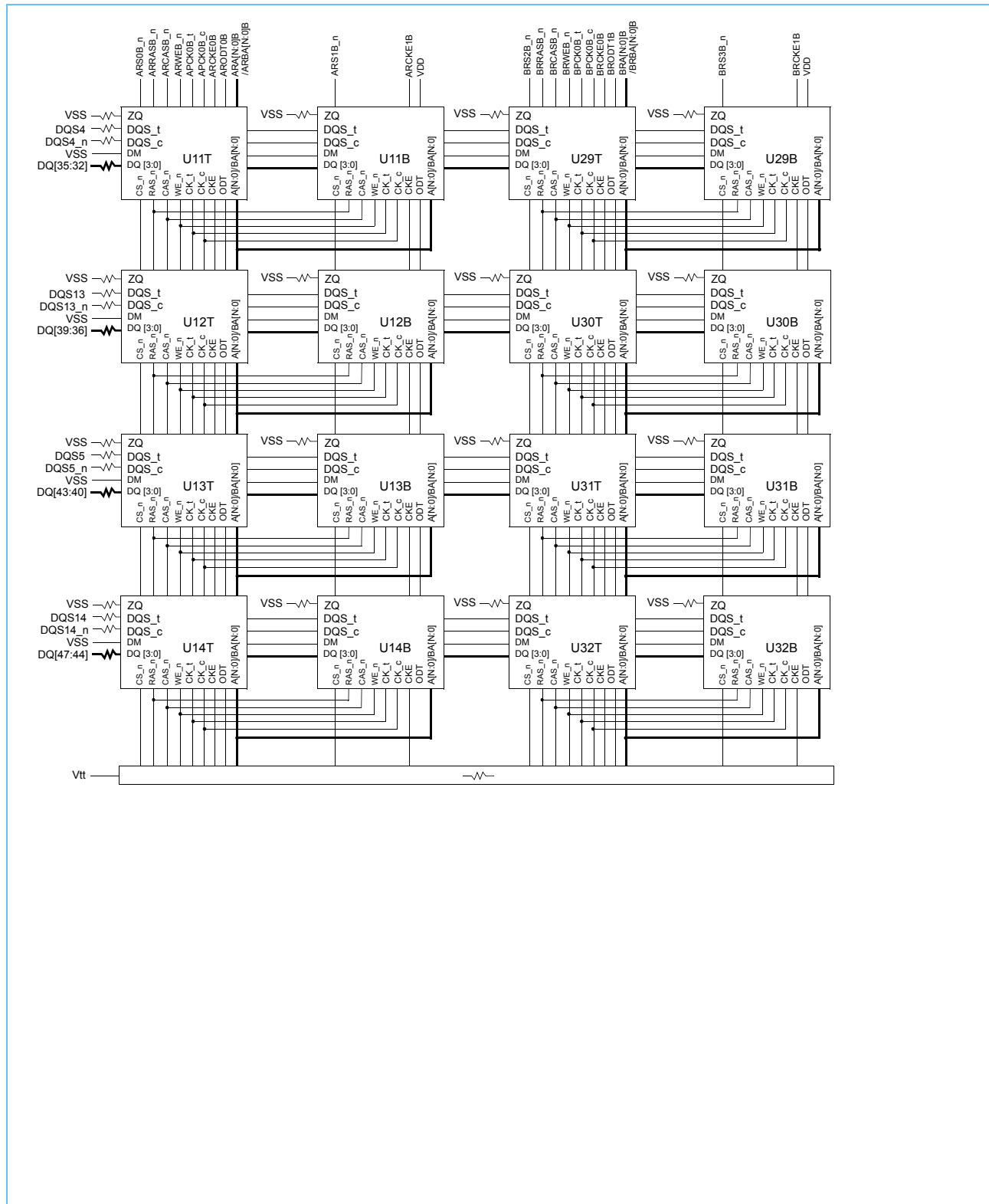
Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 3 of 5)



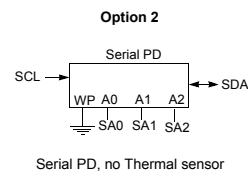
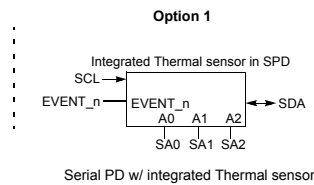
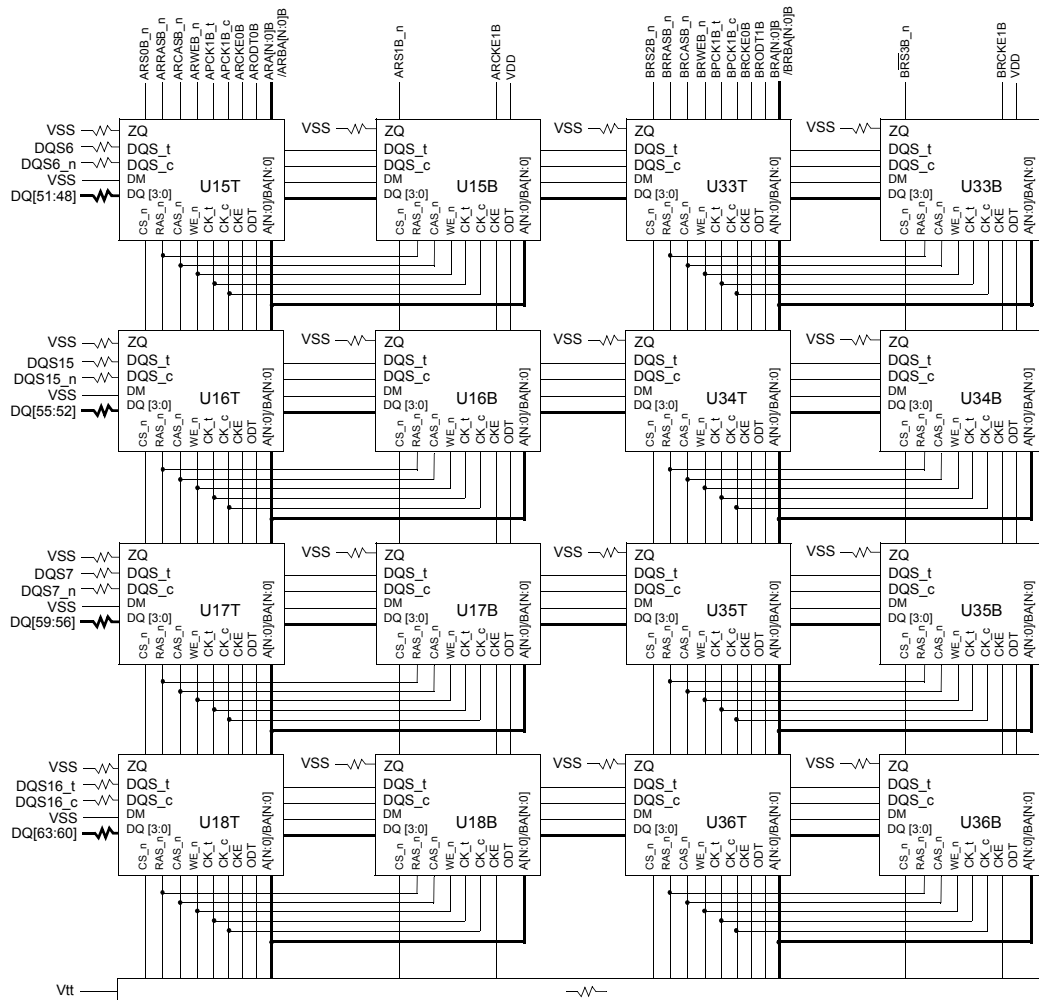
Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 4 of 5)



Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 5 of 5)



Notes:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 15 Ohms $\pm$ 5%.
3. See the wiring diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are 240 Ohms $\pm$ 1%. For all other resistor values refer to the appropriate wiring diagram.

