

4.20.21 - 204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM
72b-S0-DIMM Design Specification

DDR3 SDRAM 72b-SO-DIMM Design Specification

Revision 1.0

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1 Product Description

This specification defines the electrical and mechanical requirements for 204-pin, EP3(1.5 Volt) EP3L(1.35 Volt) EP3U(1.25 Volt), 72 bit-wide, Double Data Rate Synchronous DRAM Small Outline Dual In-Line Memory Modules (DDR3 SDRAM 72b-SO-DIMMs). These 72b-SO-DIMMs are intended for use as main memory when installed in embedded systems such as telecommunications I/O cards. EP3x-6400/EP3x-8500/EP3x-10600/EP3x-12800/EP3x-14900/EP3x-17000 refers to the JEDEC standard DIMM naming convention in which EP3x-6400/EP3x-8500/EP3x-10600/EP3x-12800/EP3x-14900/EP3x-17000 indicates a 204-pin DIMM running at 400/533/666/800/931/1063 MHz clock speed and offering 6400/8500/10600/12800/14900/17000 MB/s bandwidth on the primary data bus.

Reference design examples are included which provide an initial basis for 72b-SO-DIMM designs which may be unbuffered (72b-SO-DIMM), registered (72b-SO-RDIMM), or clocked (72b-SO-CDIMM). Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for EP3x-6400/EP3x-8500/EP3x-10600/EP3x-12800/EP3x-14900/EP3x-17000 support. All DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Table 1 — Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width (nom.) x thickness (max.) / MO-number,	30.0 mm x 67.6 mm x Max3.80 mm / MO-268
Pin count	204
SDRAMs supported	512 Mb, 1 Gb, 2 Gb, 4 Gb, 8 Gb
Ranks supported per DIMM	1, 2, 4
Capacity	256 MB, 512 MB, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, 32 GB
Serial PD	Consistent with JC 45
Voltage options	1.5/1.35/1.25 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.5/1.35/1.25 volt signal switching based on reference voltage at $V_{DD}/2$. See DRAM specification for more detail.

2 Environmental Requirements

DDR3 SDRAM 72b-SO-DIMMs are intended for use in telecommunications environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating temperature	See Note		3
H _{OPR}	Operating humidity (relative)	10 to 90	%	Note
T _{STG}	Storage temperature	-50 to +100	°C	Note
H _{STG}	Storage humidity (without condensation)	5 to 95	%	Note
P _{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	Note, Note
Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.				
Note 2 Up to 9850 ft.				
Note 3 The designer must meet the case temperature specifications for individual module components.				

3 Pinout and Description

Table 3 — Pin Description

Pin Name	Description	Num-ber	Pin Name	Description	Num-ber
CK0_t	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
CK0_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CK1_t	Clock Input, positive line	1	CB[7:0]	Data check bits Input/Output	8
CK1_c	Clock Input, negative line	1	DQS_t[8:0]	Data strobes	9
CKE[1:0]	Clock Enables	2	DQS_c[8:0]	Data strobes, negative line	9
RAS_n	Row Address Strobe	1	DM[8:0]	Data Masks / Data strobes, Termination data strobes	9
CAS_n	Column Address Strobe	1			
WE_n	Write Enable	1			
S_n[3:0]	Chip Selects	4	EVENT_n	Reserved for optional hardware temperature sensing	1
A[9:0],A11, A[15:13]	Address Inputs	14			
A10/AP	Address Input/Autoprecharge	1	RESET_n	Register and SDRAM control pin	1
A12/BC_n	Address Input/Burst chop	1	V _{DD}	Power Supply	xx
BA[2:0]	SDRAM Bank Addresses	3	V _{SS}	Ground	xx
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFDQ}	Reference Voltage for DQ	1
SDA	SPD Data Input/Output	1	V _{REFCA}	Reference Voltage for CA	1
SA[1:0]	SPD Address Inputs	2	V _{TT}	Termination Voltage	2
Par_In	Parity bit for the Address and Control bus	1	V _{DDSPD}	SPD Power	1
Err_Out_n	Parity error found on the Address and Control bus	1	Total		204

Table 4 — Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAMs on rank 0 (72b-SO-DIMM).
CK0_c	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAMs on rank 0 (72b-SO-DIMM).
CK1_t	IN	Positive Edge	Positive line of a secondary differential pair of system clock inputs. Terminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 of 72b-SO-DIMMs.
CK1_c	IN	Negative Edge	Negative line of a secondary differential pair of system clock inputs. Terminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 of 72b-SO-DIMMs.

Table 4 — Registered DIMM Input/Output Functional Description (Cont'd)

Symbol	Type	Polarity	Function
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). Connected to the registering clock driver on 72b-SO-RDIMMs, connected to DRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs.
S_n[3:0]	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs. For 72b-SO-RDIMMs, other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2] operate similarly to S[1:0] for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V _{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
A[15:13, 12/BC_n, 11, 10/AP, 9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS command. The address inputs also provide the op-code during Mode Register Set commands. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS_t[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS_c[17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[1:0]	IN	—	These signals are tied at the system planar to either V _{SS} or V _{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V _{DDSPD} on the system planar to act as a pullup.

Table 4 — Registered DIMM Input/Output Functional Description (Cont'd)

Symbol	Type	Polarity	Function
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part.
V _{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN		The RESET_n pin is connected to the RESET_n pin on the register (72b-SO-RDIMM) and to the RESET_n pin on the SDRAMs (all modules). When low, all register outputs will be driven low and the Clock Driver clocks to the DRAMs and register(s) will be set to low level (the Clock Driver will remain synchronized with the input clock).
Par_In	IN		Parity bit for the Address and Control bus. ("1 ": Odd, "0 ": Even). Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.
Err_Out_n	OUT (open drain)		Parity error detected on the Address and Control bus. A resistor may be connected from Err_Out_n bus line to V _{DD} on the system planar to act as a pull up. Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.

Table 5 — DDR3 204-pin 72b-SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREFDQ	2	VSS	53	VSS	54	DQ28	103	A3	104	A4	155	VSS	156	DQS5_t
3	VSS	4	DQ4	55	DQ24	56	DQ29	105	A1	106	A2	157	DM5	158	VSS
5	DQ0	6	DQ5	57	DQ25	58	VSS	107	A0	108	BA1	159	DQ42	160	DQ46
7	DQ1	8	VSS	59	DM3	60	DQS3_c	109	VDD	110	VDD	161	DQ43	162	DQ47
9	VSS	10	DQS0_c	61	VSS	62	DQS3_t	111	CK0_t	112	Par_In, NC, CK1_t	163	VSS	164	VSS
11	DM0	12	DQS0_t	63	DQ26	64	VSS	113	CK0_c	114	Err_Out_n, NC, CK1_c	165	DQ48	166	DQ52
13	DQ2	14	VSS	65	DQ27	66	DQ30	115	VDD	116	VDD	167	DQ49	168	DQ53
15	DQ3	16	DQ6	67	VSS	68	DQ31	117	A10/AP	118	S3_n	169	VSS	170	VSS
17	VSS	18	DQ7	69	CB0	70	VSS	119	BA0	120	S2_n	171	DQS6_c	172	DM6
19	DQ8	20	VSS	71	CB1	72	CB4	121	WE_n	122	RAS_n	173	DQS6_t	174	DQ54
21	DQ9	22	DQ12	Key				123	VDD	124	VDD	175	VSS	176	DQ55
23	VSS	24	DQ13	73	VSS	74	CB5	125	CAS_n	126	ODT0	177	DQ50	178	VSS
25	DQS1_c	26	VSS	75	DQS8_c	76	DM8	127	S0_n	128	ODT1	179	DQ51	180	DQ60
27	DQS1_t	28	DM1	77	DQS8_t	78	VSS	129	S1_n	130	A13	181	VSS	182	DQ61
29	VSS	30	RESET_n	79	VSS	80	CB6	131	VDD	132	VDD	183	DQ56	184	VSS
31	DQ10	32	VSS	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	DQS7_c
33	DQ11	34	DQ14	83	CB3	84	VREFCA	135	DQ33	136	DQ37	187	VSS	188	DQS7_t
35	VSS	36	DQ15	85	VDD	86	VDD	137	VSS	138	VSS	189	DM7	190	VSS
37	DQ16	38	VSS	87	CKE0	88	A15	139	DQS4_c	140	DM4	191	DQ58	192	DQ62
39	DQ17	40	DQ20	89	CKE1	90	A14	141	DQS4_t	142	DQ38	193	DQ59	194	DQ63
41	VSS	42	DQ21	91	BA2	92	A9	143	VSS	144	DQ39	195	VSS	196	VSS
43	DQS2_c	44	DM2	93	VDD	94	VDD	145	DQ34	146	VSS	197	SA0	198	EVENT_n
45	DQS2_t	46	VSS	95	A12/BC_n	96	A11	147	DQ35	148	DQ44	199	VDDSPD	200	SDA
47	VSS	48	DQ22	97	A8	98	A7	149	VSS	150	DQ45	201	SA1	202	SCL
49	DQ18	50	DQ23	99	A5	100	A6	151	DQ40	152	VSS	203	VTT	204	VTT
51	DQ19	52	VSS	101	VDD	102	VDD	153	DQ41	154	DQS5_c				

Terminology:

- * Active low signals are indicated by the suffix "_n"
- * Positive line of differential pairs are indicated by the suffix "_t"
- * Complementary inputs of differential pairs are indicated by the suffix "_c"

See Notes on following page for differences of 72b-SO-RDIMMs, 72b-SO-CDIMMs, and 72b-SO-DIMMs

Table 6 — Pinout Comparison Based on Module Type

Pin #	72b-SO-RDIMM		72B-SO-CDIMM		72B-SO-DIMM	
	Signal	Notes	Signal	Notes	Signal	Notes
89	CK0_c	Connected to CK_t and CK_c inputs on registering clock driver	CK0_c	Connected to CK_t and CK_c inputs on PLL	CK0_c	Connected to rank 0 SDRAMs
87	CK0_t		CK0_t		CK0_t	
88	Par_In	Connected to the registering clock driver	CK1_c	CK1_t and CK1_c are terminated but not used	CK1_c	Connected to rank 1 SDRAMs on 2 rank DIMMs, terminated but not used on 1 rank DIMMs
90	ErrOut_n		CK1_t		CK1_t	
121	S1_n	Connected to the registering clock driver	S1_n	Used for dual-rank 72b-SO-CDIMMs, not connected on single-rank 72b-SO-CDIMMs	S1_n	Used for 2 rank DIMMs, not connected on 1 rank DIMMs
114	ODT1, NC	Connected to the registering clock driver on dual- and quad- rank DIMMs; NC on single-rank DIMMs	ODT1, NC	Used for dual-rank DIMMs, not connected on single-rank DIMMs	ODT1, NC	Used for dual-rank DIMMs, not connected on single-rank DIMMs
126	S2_n, NC	Connected to the register on 4 rank DIMMs, not connected on 1 or 2 rank DIMMs	NC	Not used	NC	Not used
119	CKE1	Connected to the register on 2 and 4 rank DIMMs; NC on 1 rank DIMMs	CKE1, NC	Used for 2 rank DIMMs, not connected on 1 rank DIMMs	CKE1, NC	Used for 2 rank DIMMs, not connected on 1 rank DIMMs
117	A15	Connected to the registering clock driver	A15, NC	Depending on device density, may not be connected to SDRAMs. However, these signals are terminated. A15 not routed on some Raw Cards	A15, NC	Depending on device density, may not be connected to SDRAMs. However, these signals are terminated. A15 not routed on some Raw Cards
130	A14		A14		A14	
101	A13		A13		A13	
125	S3_n, NC	Connected to the register on 4 rank DIMMs, not connected on 1 or 2 rank DIMMs	NC	Not used	NC	Not used
NC = no internal connection						

4 Component Details

Table 7 — Supported SDRAM Components Maximum size for 512Mb to 8Gb; DDR3 SDRAM

This table is for reference only. Please see appropriate raw card annex for more information.

[illegible]