

Annex B - Raw Card B

DDR3 SO-RDIMM Design File

RC	Applicable Design File	Applicable BOM
B0	EP3-72b-SO-RDIMM_V051_RC_B0_20110405.brd	EP3-72b-SO-RDIMM_V051_RC_B0_20110120_BOM.txt
Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.		

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Column/Bank	MO-268 Variation
Capacity	Organization	Density	Organization				
1GB	128Mx72	512Mbit	64Mx8	18	2	13/10/3	CA
2GB	256Mx72	1Gbit	128Mx8	18	2	14/10/3	CA
4GB	512Mx72	2Gbit	256Mx8	18	2	15/10/3	CA
8GB	1Gx72	4Gbit	512Mx8	18	2	16/10/3	CA
16GB	2Gx72	8Gbit	1Gx8	18	2	16/11/3	CA

Note: Some heat spreaders may not be covered within these variations.

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 Variation
11.5 x 20 mm	8	106 Ball FBGA	Stacked	DW-z

Supported Speeds

Note: X will reflect passed committee ballot at the time when specification is issued at BOD ballot

Voltage	EP3-6400	EP3-8500	EP3-10600	EP3-12800	EP3-14900	EP3-17000	Notes
DDR3	X	X	X				
DDR3L	X	X	X				

Note: X will reflect passed committee ballot at the time when the specification is issued at BOD ballot

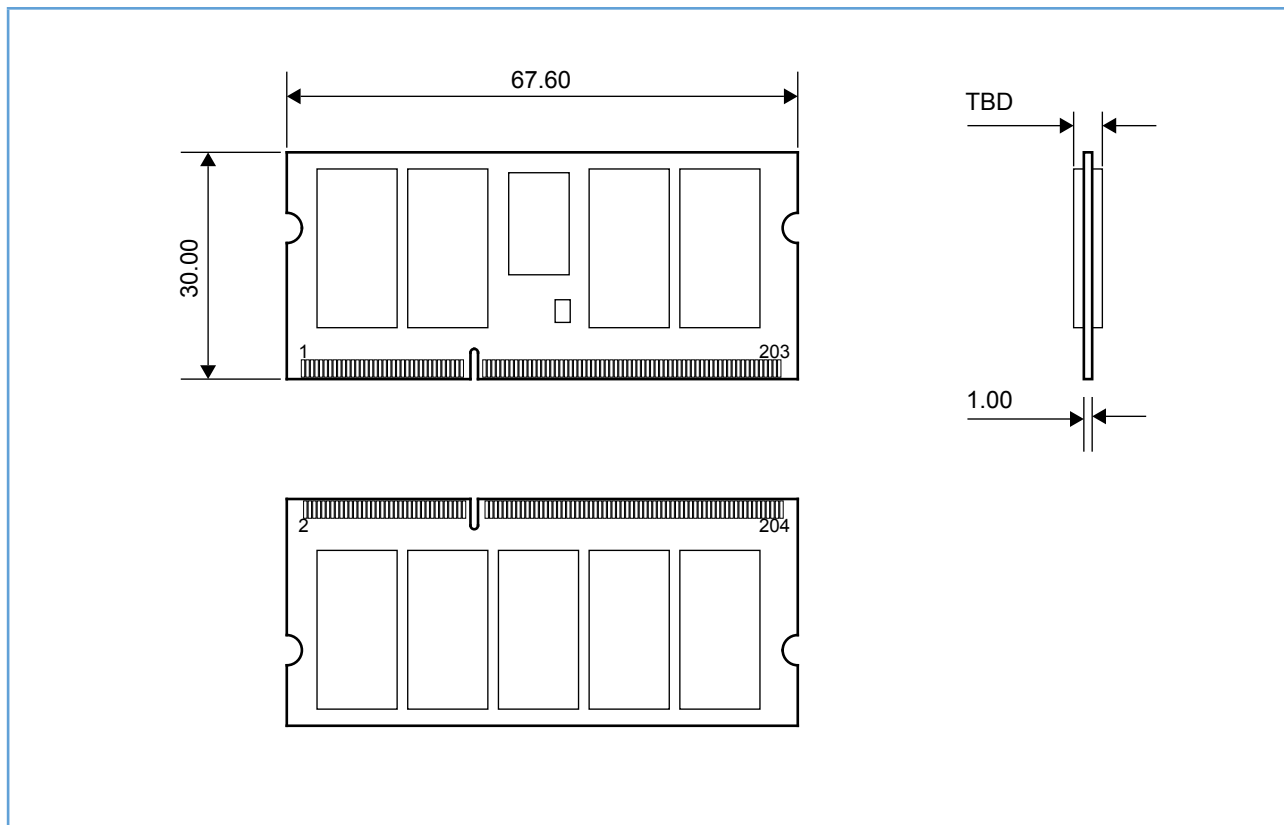
Note: P means proposed speed for committee ballot.

Design Rules and Deviations

None

General Layout

x72 SO-RDIMM, populated as two physical ranks of x8 DDR3 SDRAMs



Note 1: All dimension are typical unless otherwise stated. (Millimeters)

Note 2: Thermal sensor is placed within the Thermal Sensor Placement Area as defined in MO-268.

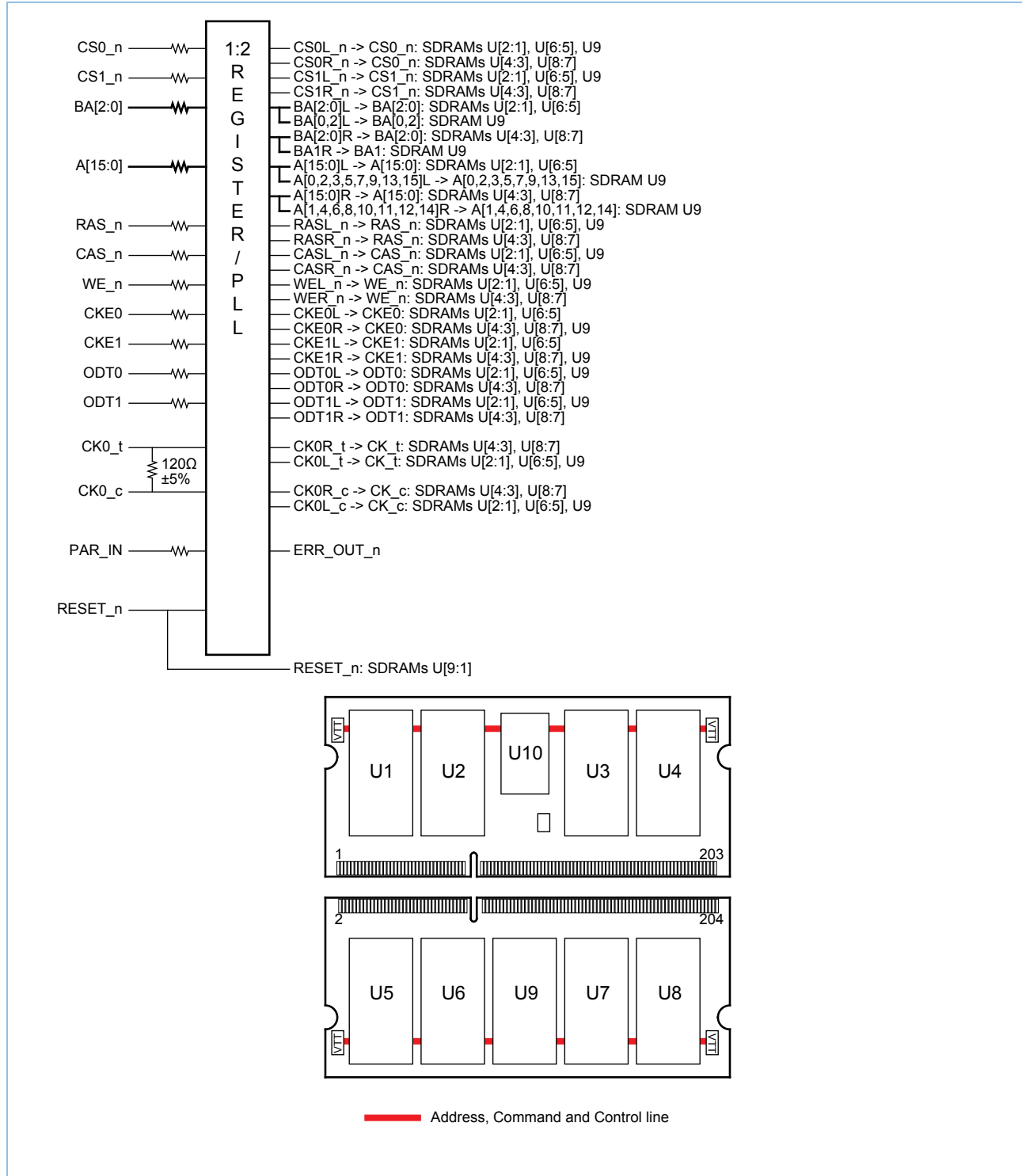
Note 3: Registering clock driver is placed within the Register Placement Area as defined in MO-268.

Note 4: Implementation and dimensions shown without heat spreader.

Note 5: In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-268 for dimensions of specific variations with heat spreader attached.

Block Diagram

x72 SO-RDIMM, populated as two physical ranks of x8 DDR3 SDRAMs (Part 1 of 2)



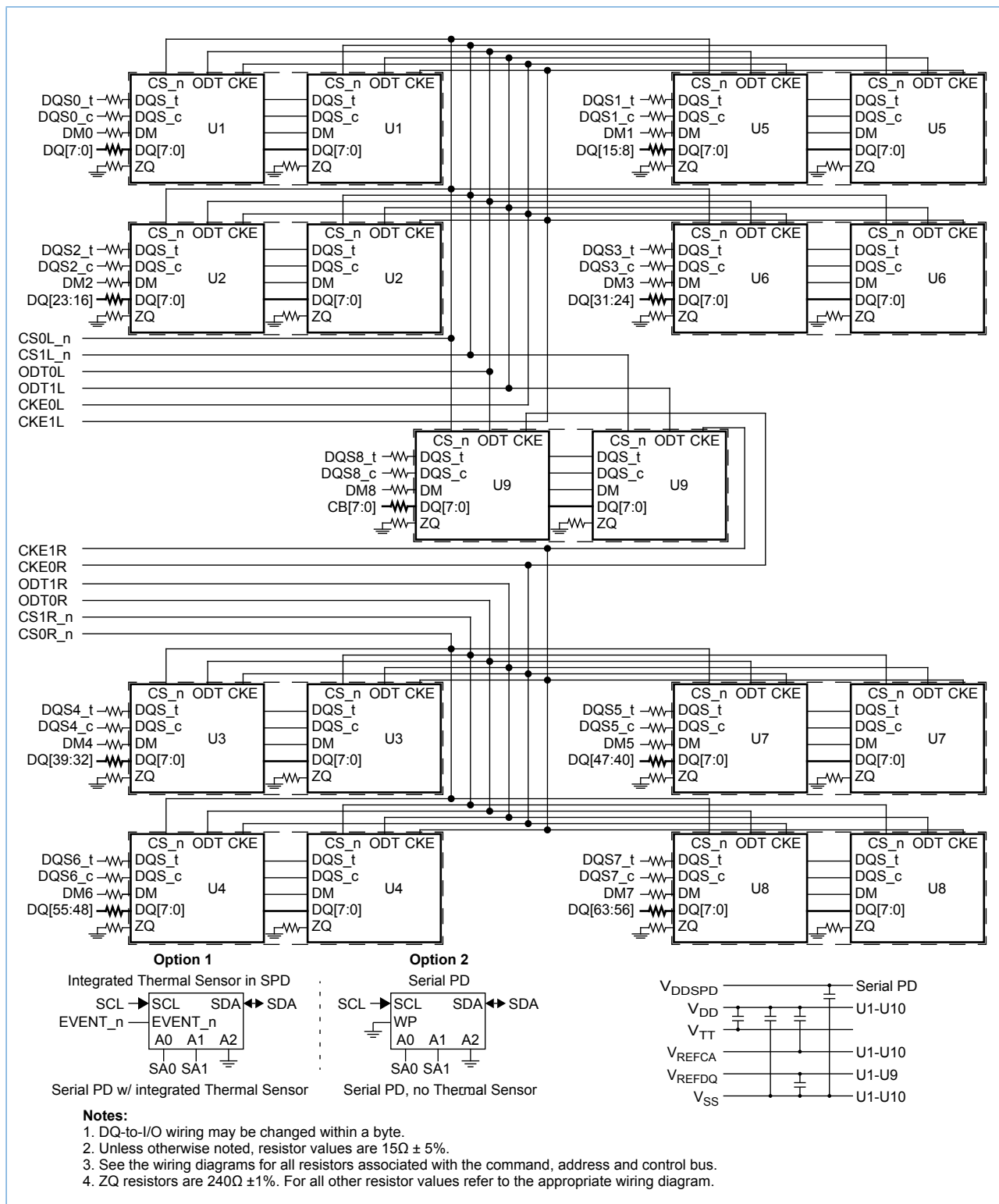
Note 1: Unless otherwise specified, all resistor values are 22ohms.

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Functional Block Diagram

x72 SO-RDIMM, populated as two physical ranks of x8 DDR3 SDRAMs (Part 2 of 2)



Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specifications

DRAMs per output	Register Type	Register Speed Grade PC3-6400	Register Speed Grade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
5 / 4	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only.

They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match module implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.