

Annex D - Raw Card D

DDR3 72b-SO-DIMM Design File

Specification Revision	Applicable Design File	Applicable BOM
1.00	EP3-72b-SO-DIMM_V070_RC_D0_20101215.brd	EP3-72b-SO-DIMM_V070_RC_D0_20101215_BOM.xlsx
1.30	EP3-72b-SO-DIMM_V130_RC_D1_20130215.brd	EP3-72b-SO-DIMM_V130_RC_D1_20130215_BOM.xlsx

Note: "Reference" design file updates will be released as needed. This 72b-SO-DIMM specification will reflect the most recent files, design but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Col/Bank	MO-268 variation
Capacity	Organization	Density	Organization				
1GB	128M x 72	512Mbit	64M x 8	18	2	13/10/3	CA
2GB	256M x 72	1Gbit	128M x 8	18	2	14/10/3	CA
4GB	512M x 72	2Gbit	256M x 8	18	2	15/10/3	CA
8GB	1G x 72	4Gbit	512M x 8	18	2	16/10/3	CA
16GB	2G x 72	8Gbit	1G x 8	18	2	16/11/3	CA

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
10.5 mm x 12.5 mm	8	78 Ball FBGA	Planar	DT-z

Supported Speeds

Raw Card	Config	EP3-6400	EP3-8500	EP3-10600	EP3-12800	EP3-14900	Notes
D0	DDR3	X	X	X			1
D1	DDR3	P	P	P	P		1
	DDR3L	P	P	P	P		1

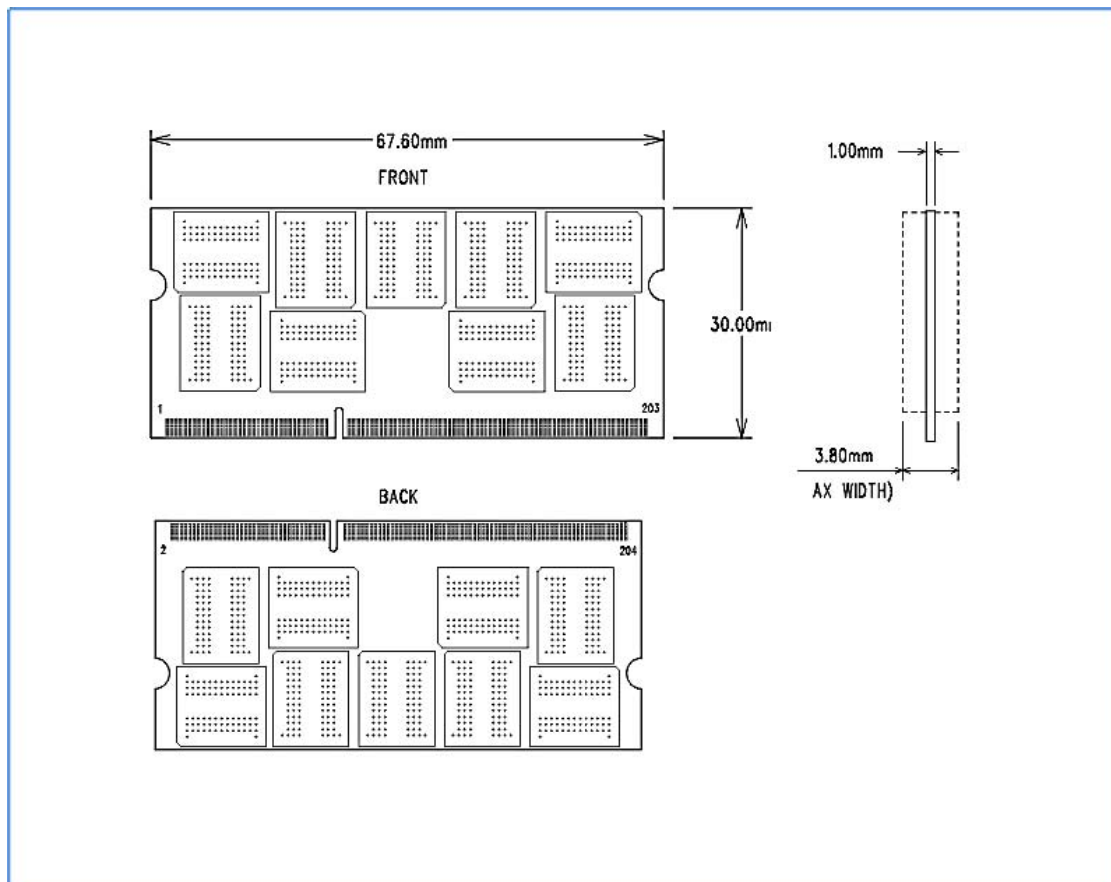
Note 1: "X" reflects speed grades approved from previous ballots. "P" reflects speed grades for this ballot. JEDEC office to replace "P" with "X" before publication.

Design Rules and Deviations

None

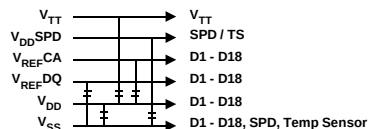
General Layout

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



Note All dimensions are typical unless otherwise stated. (Millimeters)

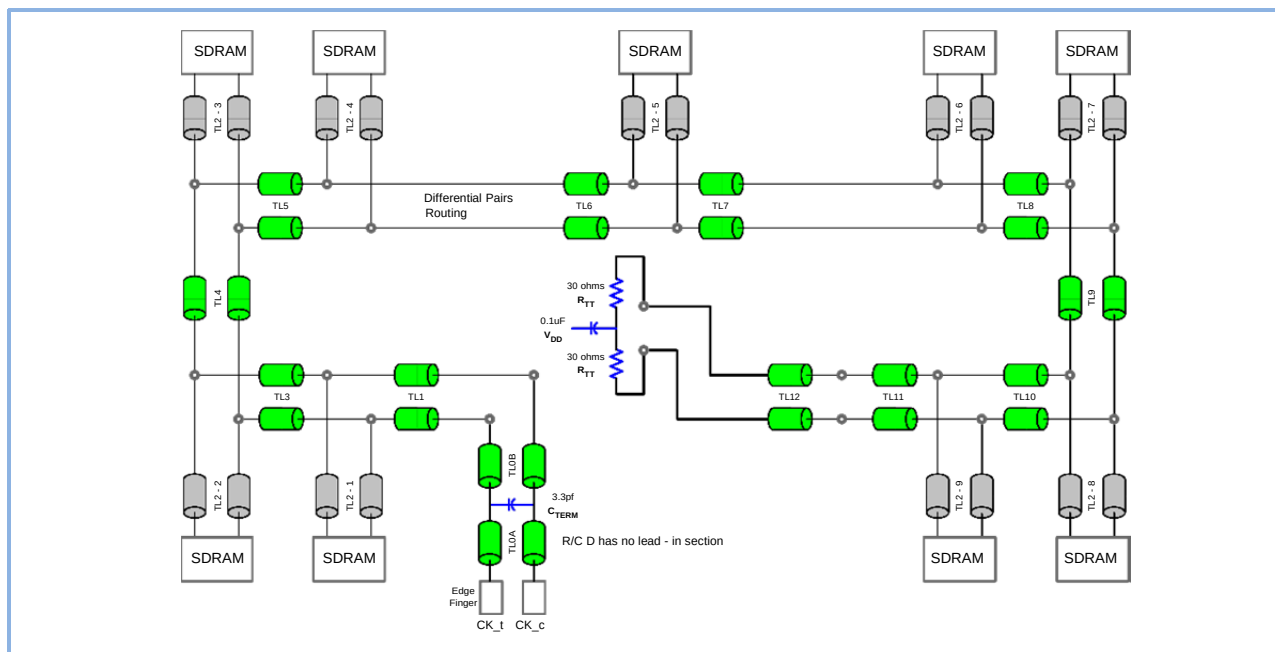
x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



Input Loading Matrix

Signal Names	Input Device	Loads
CK0_t, CK0_c, CK1_t, CK1_c	SDRAM	9
RESET_n	SDRAM	18
CKE0, ODT0, S0_n, CKE1, ODT1, S1_n	SDRAM	9
Addr, BA, RAS_n, CAS_n, WE_n	SDRAM	18
DQ, CB, DQS_t, DQS_c	SDRAM	2
DM, TDQS_t, TDQS_c	SDRAM	2
SCL, SDA, SA	EEPROM	1
EVENT_n	Thermal sensor	1*
*Integrated thermal sensor optional.		

Clock Net Wiring CK [1:0] _t, CK [1:0] _c (Raw Card D0)



Clock Routing Trace Lengths Raw Card D0

Type	TL0A Micro Strip		TL0B Micro Strip		TL1 Strip		TL2 Micro Strip		TL3 Strip		TL4 Strip	
CK_T,CK_C	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	4.0	4.0	0.8	0.9	32.1	32.5	3.7	4.0	22.9	23.0	21.6	21.7

TL5 Strip		TL6 Strip		TL7 Strip		TL8 Strip		TL9 Strip		TL10 Strip	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
20.8	20.9	13.5	13.6	13.6	13.7	18.9	19.0	21.9	22.0	24.1	24.2

TL11 Strip		TL12 Micro Strip		Compensated TL0+TL1 +TL2-1		Compensated TL0+TL1+ TL3+TL2-2		Compensated TL0+TL1+TL3 +TL4+TL2-3		Compensated TL0+TL1+TL3+ TL4+TL5+TL2-4	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
7.5	7.5	0.9	1.1	34.9	35.0	57.8	57.9	79.7	79.8	100.4	100.5

Compensated TL0+TL1+TL3+TL4+ TL5+TL6+TL2-5		Compensated TL0+TL1+TL3+TL4+ TL5+TL6+TL7+TL2-6		Compensated TL0+TL1+TL3+TL4+ TL5+TL6+TL7+TL8+TL2-7		Compensated TL0+TL1+TL3+TL4+TL5+ TL6+TL7+TL8+TL9+TL2-8		Compensated TL0+TL1+TL3+TL4+TL5+ TL6+TL7+TL8+TL9+TL10+TL2-9		Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
114.0	114.1	127.6	127.7	146.5	146.6	168.5	168.6	192.9	193.0	

NOTE 1. All distances are given in millimeters.

NOTE 2. Recommended spacing from Differential pair to other Nets: CK_T, CK_C and other spacing: minimum 0.15

NOTE 3. In the column of compensated length, Micro-strip line length is compensated as Equivalent Strip line Length (= Micro strip Length / 1.1),
e.g.: (compensated TL0+TL1+TL2-1) = TL0A/1.1 + TL0B/1.1 + TL1 + TL2-1/1.1