

**4.20.22 144-Pin DDR3 SDRAM Unbuffered 32b-SO-DIMM Design
Specification**

**EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-
DIMM Design Specification**

Revision 0.31

February 2012

Contents

1. Product Description	3
Product Family Attributes	3
2. Environmental Requirements	4
3. Pinout and Description	5
Pin Description	5
Input/Output Functional Description	6
DDR3 Unbuffered 32b-SO-DIMM Pinout	8
Address Mirroring Feature	9
SPD and Thermal Sensor	10
4. Component Details	11
SO-DIMM landing pattern for x8	12
SO-DIMM landing pattern for x16	13
x8 Ball pattern	14
x16 Ball pattern	15
5. DDR3 Unbuffered 32b-SO-DIMM Wiring Details	16
Signal Groups	16
General Net Structure Routing Rules.....	16
Explanation of Net Structure Diagrams.....	19
6. Serial Presence Detect Definition	20
7. DDR3 “Embedded Product” DIMM Label Format	22
8. DIMM Mechanical Specifications	24
Annex A - Raw Card A(x8 1R)	
Annex B - Raw Card B(x8 2R)	
Annex C - Raw Card C(x16 1R).....	
Annex D - Raw Card D(x16 2R)	

1. Product Description

This specification defines the electrical and mechanical requirements for 144-pin, EP3-3200/EP3-4200/EP3-5300/EP3-6400, 32 bit-wide, Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM Unbuffered 32b-SO-DIMMs). These DDR3 32b-SO-DIMMs are intended for use in cost sensitive, low pin count applications such as peripheral devices. EP3-3200/EP3-4200/EP3-5300/EP3-6400 refers to the JEDEC standard DIMM naming convention in which EP3-3200/EP3-4200/EP3-5300/EP3-6400 indicates a 32bits DIMM running at 400/533/666/800 MHz clock speed and offering 3200/4200/5300/6400 MB/s bandwidth. As a variation, EP3L 1.35V version is defined.

Reference design examples are included which provide an initial basis for DDR3 Unbuffered 32b-SO-DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for EP3-3200/EP3-4200/EP3-5300/EP3-6400 support. All DDR3 Unbuffered 32b-SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

DIMM organization	x32 NO-ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.0 mm x 67.6 mm x 3.80 mm / MO-274, Variation TBD
Pin count	144
SDRAMs supported	512 Mb, 1 Gb, 2 Gb, 4 Gb, 8Gb
Capacity	128MB, 256 MB, 512 MB, 1 GB, 2 GB, 4 GB, 8 GB
Serial PD	Consistent with JC 45
Voltage options	1.5 volt (DDR3/V _{DD}), 1.35 volt (DDR3L/V _{DD}), 3.3 volt (V _{DDSPD})
Interface	1.5/1.35 volt signal switching based on reference voltage at VDD/2. See DRAM specification for more detail.

2. Environmental Requirements

DDR3 SDRAM Unbuffered 32b-SO-DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating temperature	See Note		3
H _{OPR}	Operating humidity (relative)	10 to 90	%	1
T _{STG}	Storage temperature	-50 to +100	°C	1
H _{STG}	Storage humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft. 3. The designer must meet the case temperature specifications for individual module components.				

3. Pinout and Description

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]_t	Clock Input, positive line	2	ODT[1:0]	On Die Termination Inputs	2
CK[1:0]_c	Clock Input, negative line	2	DQ[31:0]	Data Input/Output	32
			DQS[3:0]_t	Data strobes, positive line	4
CKE[1:0]	Clock Enables	2	DQS[3:0]_c	Data strobes, negative line	4
RAS_n	Row Address Strobe	1	DM[3:0]	Data Masks	4
CAS_n	Column Address Strobe	1	NC	No connect. May be used for future use	12
WE_n	Write Enable	1			
S[1:0]_n	Chip Selects	2	EVENT_n	Reserved for optional hardware temperature sensing	1
A[9:0],A11, A[15:13]	Address Inputs	14	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
A10/AP	Address Input/Autoprecharge	1	RESET_n	SDRAM control pin	1
A12/BC_n	Address Input/Burst chop	1	V _{DD}	Power Supply	18
BA[2:0]	SDRAM Bank Addresses	3	V _{SS}	Ground	26
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFDQ}	Reference Voltage for DQ	1
SDA	SPD Data Input/Output	1	V _{REFCA}	Reference Voltage for CA	1
SA[2:0]	SPD Address Inputs	3	V _{TT}	Termination Voltage	1
			V _{DDSPD}	SPD Power	1

DDR3 Unbuffered 32b-SO-DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK[1:0]_t	IN	Positive Edge	Positive line of the differential pair of system clock inputs.
CK[1:0]_c	IN	Negative Edge	Negative line of the differential pair of system clock inputs.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[1:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ31.
V _{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, CKE0, CKE1, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[15:13, 12/BC_n,11, 10/AP,9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[31:0]	I/O	—	Data Bit Input/Output pins
DM[3:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR3/DDR3L SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[3:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[3:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[2:0]	IN	—	These signals are tied at the system planar to either V _{SS} or V _{DD} SPD to configure the serial SPD EEPROM and Temp sensor address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V _{DD} SPD on the system planar to act as a pull-up.
SCL	IN	—	This pin is used to clock data into and out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SCL bus line to V _{DD} SPD on the system planar to act as a pull up.

DDR3 Unbuffered 32b-SO-DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part.
V _{DD} SPD	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN		This pin is connected to the RESET_n pin on the DRAM.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)