

Appendix B - Raw Card B(x8 2R)

DDR3 Unbuffered 32b-SO-DIMM Design File

Rev	Applicable Design File	Applicable BOM
0.51	EP3-32b-SO-DIMM-V051_RC_B0_20111028.brd	EP3-32b-SO-DIMM-V051_RC_B0_20111028_BOM.xls
1.0	EP3-32b-SO-DIMM-V100_RC_B1_20130108.brd	EP3-32b-SO-DIMM-V100_RC_B1_20130108_BOM.xlsx

Note 1 "Reference" design file updates will be released as needed. This 32b-SO-DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Col/Bank
Capacity	Organization	Density	Organization			
512MB	128M x 32	512Mbit	64M x 8	8	2	13/10/3
1GB	256M x 32	1Gbit	128M x 8	8	2	14/10/3
2GB	512M x 32	2Gbit	256M x 8	8	2	15/10/3
4GB	1G x 32	4Gbit	512M x 8	8	2	16/10/3
8GB	2G x 32	8Gbit	1G x 8	8	2	16/11/3

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
11.0 mm x 16.0 mm	8	82 Ball FBGA	Planar	DW-z

Supported Speeds

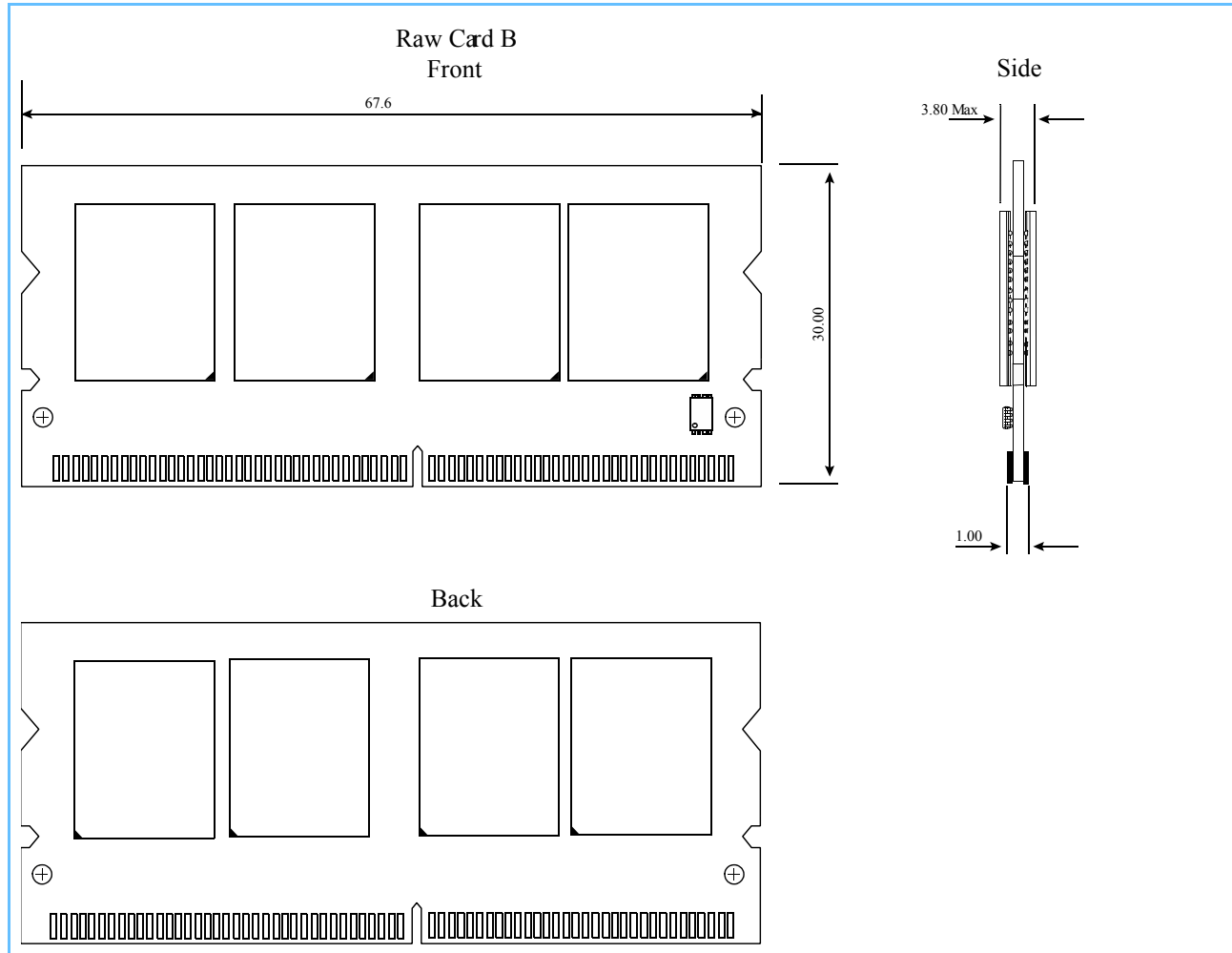
EP3-3200 (DDR3-800)	EP3-4200 (DDR3-1066)	EP3-5300 (DDR3-1333)	EP3-6400 (DDR3-1600)	Notes
X	X	X		
EP3L-3200 (DDR3L-800)	EP3L-4200 (DDR3L-1066)	EP3L-5300 (DDR3L-1333)	EP3L-6400 (DDR3L-1600)	Notes
X	X	X		

Design Rules and Deviations

DQ Fanouts from DRAM on the bottom side are referenced to full VDD shape on Layer-5 to avoid VDD current block caused by small segmentalized VSS shapes.

General Layout

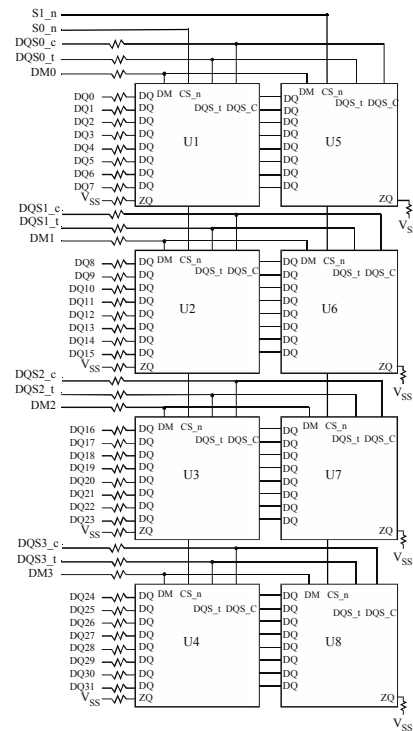
32b-SO-DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



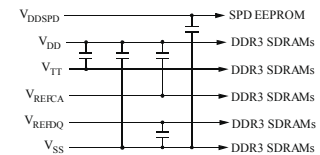
Note 1 All dimensions are typical unless otherwise stated. (Millimeters)

Functional Block Diagram

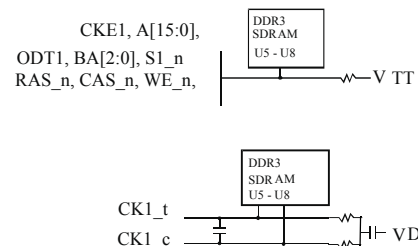
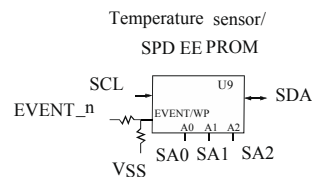
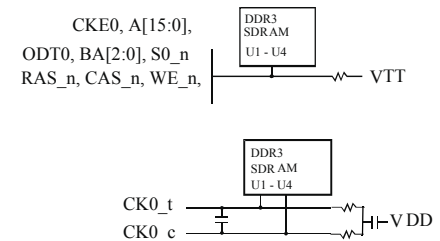
DDR3 32b-SO-DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



BA[2:0] → BA[2:0]: DDR3 SDRAMs
A[N:0] → A[N:0]: DDR3 SDRAMs
RAS_n → RAS_n: DDR3 SDRAMs
CAS_n → CAS_n: DDR3 SDRAMs
WE_n → WE_n: DDR3 SDRAMs
CKE[1:0] → CKE[1:0]: DDR3 SDRAMs
ODT[1:0] → ODT[1:0]: DDR3 SDRAMs
RESET_n → RESET_n: DDR3 SDRAMs



Clock, control, command, and address line terminations:



Notes:

1. ZQ resistors are 240 ohms +/- 1%.
For all other resistor values refer to the appropriate wiring diagram.
2. A set of DQ/DQS pair/DM group can be swapped between DRAMs.
3. Either SPD or "SPD with temp sensor" can be implemented with 0ohm register option.